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A New Hybrid Multilevel Inverter Using "U" Shape Packed Cell

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ABSTRACT: In this paper, structure for a new hybrid multilevel inverter using 'u' shape packed cell is presented, in which a series connection of the H bridge is used to increase the output voltage level.It has two different algorithms to determine the magnitude of the dc voltage sources is proposed.Reduction the number of switches,driver circuits and dc voltage sources of other recent topologies are compared and discussed. In addition to this, the proposed topology has features such as redundant state, less switching pattern and low standing voltages. The operation and performance of the proposed multilevel inverter has been verified by the simulation and experimental results of a single phase multilevel inverter.The validity of the proposed multilevel inverter is verified with both computer simulation using software (MATLAB /Simulink) and laboratory based prototype verified the results.

KEYWORDS: Symmetric Multilevel Inverter, Hybrid Inverter, CHB Multilevel Inverter, Reduced Switches

I. INTRODUCTION

The multilevel inverter was introduced in 1975.A multilevel inverter is a power electronic system that synthesize a desired stepped output voltage from several magnitude dc voltages as inputs. Multilevel power conversion has become increasingly popular in recent years due to advantages of high power quality waveforms, low electromagnetic compatibility (EMC) concerns,low switching losses and high voltage compatibility[1], low total harmonic distortion [2], redundant path.It has been extended for medium and high power applications suchas industrial electric vehicle applications,renewable energy system,motor drives,facts and so on. Generally,multilevel converters are classified into three classic structures: Neutral pointclamped(NPC)converter, flying capacitor(FC)converter,cascaded H bridge(CHB) converter[3].The unequal voltage sharing among series connected capacitors are the main drawback of NPC converter[4][5].FC converter requires a great number of storage capacitors for higher output voltage levels and the capacitor voltage balancing is difficult[3].The CHB converter is the most important structure among classical multilevel converters,because this structure needs to fewer number of power electronic components[3][4][5].Two different algorithms have been presented that lead to symmetric and asymmetric topologies.In symmetric topology all the dc voltage magnitudes are equal.In asymmetric topology all the dc voltage magnitudes are non-equal.The number of switches,insulated gate bipolar transistor (IGBT) drivers and independent dc sources, power losses,complexity of control algorithm,number of levels and total harmonic distortion for output voltage waveform,voltage stress on semiconductor devices,and the rate of standing voltage for switches are the optimization subjects in new topologies[6].It is also unable to exactly manipulate the magnitude of the output voltage due to adopted pulse width modulation (PWM) method [7].

Unfortunately,multilevel inverters do have some disadvantages.One particular disadvantage is the need for large number of power semiconductor switches.In the proposed algorithm,generate the maximum number of voltage levels at the output with the minimum number of dc voltage sources and switches,two algorithm are proposed for determination of dc voltage sources.Finally,the paper includes the simulation and experimental results of a single phase n level multilevel inverter to prove the feasibility of the proposed multilevel inverter.

II. PROPOSED TOPOLOGY

The topology recommended in [8] is uses fewer number of switches in symmetric configuration compared to CHB multilevel inverter topology. But the main drawback of the topology is increasing the voltage stress across the full bridge inverter part. In order to minimize the voltage stress the recommended topology is hybrid with

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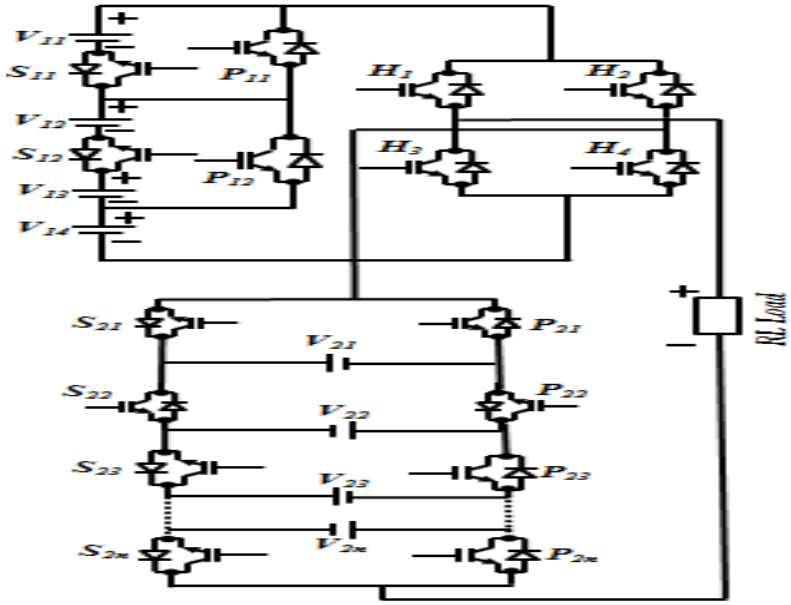
packed U cell topology. The maximum blocking voltage of Packed U cell topology is 2Vdc, whereas the recommended topology is n Vdc. To avoid the maximum blocking voltage the basic unit of [8] is selected, the basic unit consist of 4 dc voltage source with equal magnitude, 8 switches with maximum blocking voltage of 4Vdc. The new proposed basic unit is shown in fig. (1).It consists of two dc voltage sources. S_{11}, S_{12}, P_{11}, P_{12}, H_1, H_2, H_3, H_4 are the switches.In each switch consists of an IGBT with an antiparallel power diode. The number of driver circuits for the bidirectional switches are the same as the unidirectional switches in the proposed basic unit.According to fig (1), S_{11}, S_{12}, P_{11}, P_{12} should not be turned on simultaneously, because a short circuit across the dc voltage sources will be produced.



The generalized structure of proposed hybrid symmetric topology

Table1: Various Switching Pattern

State	Switching State														Output Voltage
	S_1	S_2	P_1	P_2	H_1	H_2	H_3	H_4	S_3	S_4	S_5	P_3	P_4	P_5	
0V	0	0	0	0	1	0	0	1	0	0	0	1	1	1	
±1V	0	0	1	1	1	**0**	**0**	**1**	**0**	0	0	0	0	0	Vdc
	0	0	1	1	0	1	1	0	0	0	0	1	1	1	-Vdc
±2V	1	0	0	1	1	0	0	0	0	0	0	0	0	0	$2V_{dc}$
	1	0	0	1	0	1	0	0	0	0	0	1	1	1	$-2V_{dc}$
±3V	0	1	1	0	1	0	1	1	0	0	0	0	0	0	$3V_{dc}$
	0	1	1	0	0	1	1	0	0	0	0	1	1	1	$-3V_{dc}$
±4V	1	1	0	0	1	0	0	1	0	0	0	0	0	0	$4V_{dc}$
	1	1	0	0	0	1	1	0	0	0	0	1	1	1	$-4V_{dc}$
±5V	1	1	0	0	1	0	0	1	1	0	0	0	1	1	$5V_{dc}$
	1	1	0	1	0	1	1	0	0	1	1	1	0	0	$-5V_{dc}$
±6V	1	1	0	0	1	0	0	1	1	0	1	0	1	0	$6V_{dc}$
	1	1	0	1	0	1	1	0	0	1	0	1	0	1	$-6V_{dc}$
±nV	1	1	0	0	1	0	0	1	0	0	0	1	0	1	nV_{dc}
	1	1	0	0	1	0	0	1	1	0	1	0	1	0	$-nV_{dc}$

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The proposed hybrid multilevel inverter can generate zero and positive and negative voltage levels. The zero output voltage is obtained when the switches H_1,H_4,U_{11},U_{13} are turned ON simultaneously. The other voltage levels are generated by proper switching between the switches. Table 1 shows the states of the switches for each output voltage value. In this table 1 means the corresponding switch is turned ON and 0 indicates the OFF state.
Table1 shows the output voltage levels of the proposed unit based on different switching patterns.In this table 0 and 1 indicate off and on states of the switches,respectively.As shown in table1,the basic unit is able to generate 2n+1 voltage levels at the output.In this basic unit is able to generate all of the positive and negative voltage levels at the output.

The new presented structures in three different configurations are introduced consists of symmetric method.

METHOD 1:
The structure of proposed symmetric method is shown in fig(2).
In this structure,the values of the dc voltage sources are equal.So, it is called as symmetric method.Table 1 shows the values of the output voltage.The output voltage of the proposed inverter is equal to adding the output voltage of each unit and it can be written as follows:

$V_1=V_2=V_3\ldots\ldots\ldots V_n=V_{dc}$ (1)

The number of output levels (N_{level}), $N_{switch}(N_{IGBT})$,$N_{Driver}(N_{Switches})$,V_{STV} is the proposed symmetric converter are obtained as follows,respectively

$N_{Level}=2n_L+9;n_L>=1$

$2n_U+1;n_L=0$ (2)

$N_{Switch}=10+n_L*2$ (3)

$N_{Driver}=N_{Switch}$ (4)

$V=22+4n_L$ (5)

Where n_L is the lower number of packed "U"cell dc source.
All possible states for a symmetric multilevel inverter are shown in table1.

III. COMPARISONS FOR THE NEW HYBRID MULTILEVEL INVERTER WITH OTHER TOPOLOGIES

This paper main objective is to reduce the number of power switches in multilevel inverter. The proposed symmetric multilevel inverter is compared with the other topologies. The cascaded H bridge which has the one source which carries the four switches. In each switch which consists of an IGBT with an antiparallel diode. The number of driver circuits for the bidirectional switches are the same as the unidirectional switches in the proposed basic unit. The proposed hybrid multilevel inverter can generate zero and positive and negative voltage levels. Table1 shows the output voltage levels of the proposed unit based on different switching pattern. As shown in table1, the basic unit is able to generate 2n+1 voltage levels at the output. In this basic unit is able to generate all of the positive and negative voltage levels at the output. In this basic unit is able to generate all of the positive and negative voltage levels at the output. The output voltage of the proposed inverter is equal to adding the output voltage of each unit and it can be written as follows:

$V_1=V_2=V_3\ldots\ldots\ldots V_n=V_{dc}$

The number of level, number of switches, Peak inverse voltage, blocking voltage are compared with other topologies. The voltage spike will occur at load side due to interloping in diode (Reverse recovery problem). To avoid this issue i)the load R value should be higher than L value and ii)should use LC filter at output side. So, this may not suitable for highly inductive load. The proposed novel symmetric multilevel inverter has significant improvements compared to conventional cascaded multilevel inverter.

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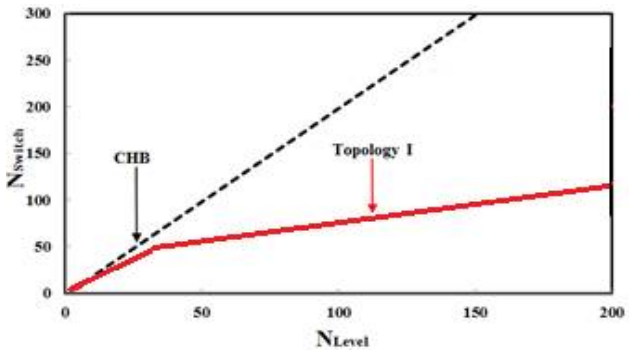

Fig.2 Comparison of Number of Level against Number of Switches

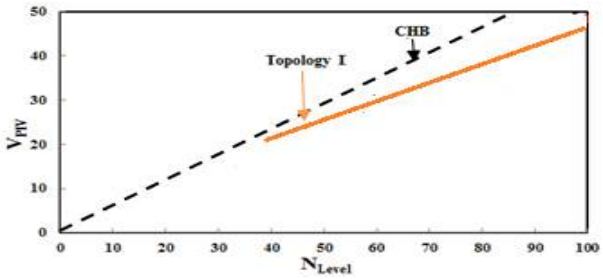

Fig.3 Comparison of Number of Level against Peak inverse voltage

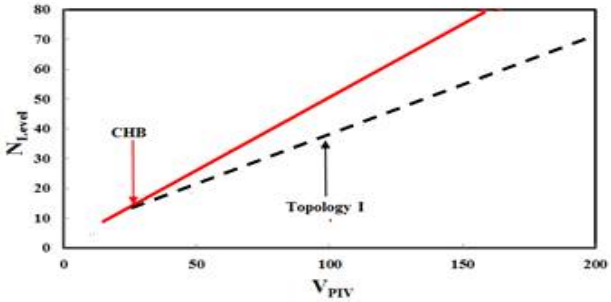

Fig.4 Comparison of Peak inverse voltage against Number of level

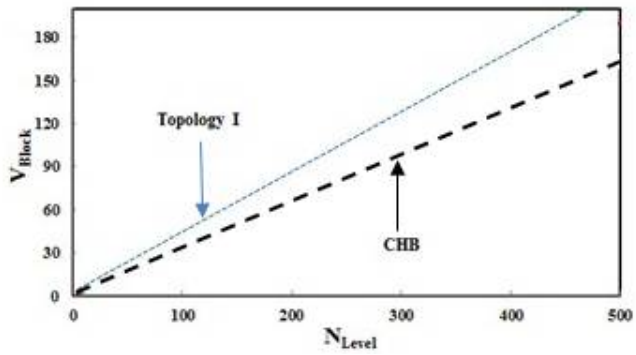

Fig.5 Comparison of Number of level against Blocking voltage

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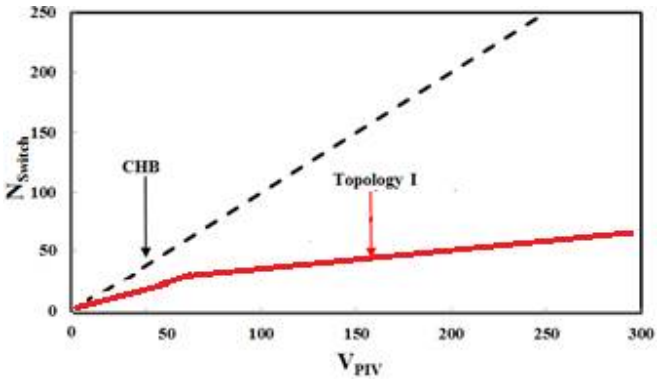

Fig.6 Comparison of Peak inverse voltage against Number of switches

IV. SIMULATION RESULT

To verify authority of proposed multilevel inverter is simulated using computer based simulation (MATLAB/SIMULINK). Each dc source of voltages $V_1=V_2=V_3=V_4=V_5=V_6=55V$. The sum of all magnitudes values 330V which produce rms voltage of 230V. Load parameters: R=20Ω, $L=100e^{-3}$. The value of output voltage frequency is50Hz.Modulation strategies are used in cascaded multilevel inverter to reduce the harmonic content.The pulse width modulation method is used in the proposed multilevel inverter because fixed dc input voltage, is supplied to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter power semiconductor devices. Fig.7 shows that the simulation circuit diagram

PULSE GENERATION:

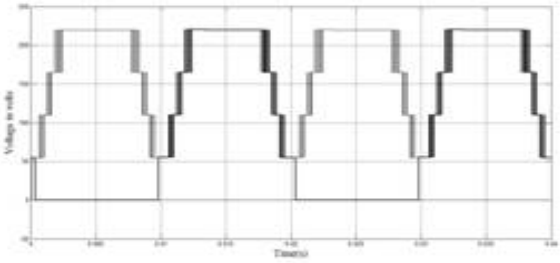

Fig.7 output pulse for DE- MUX

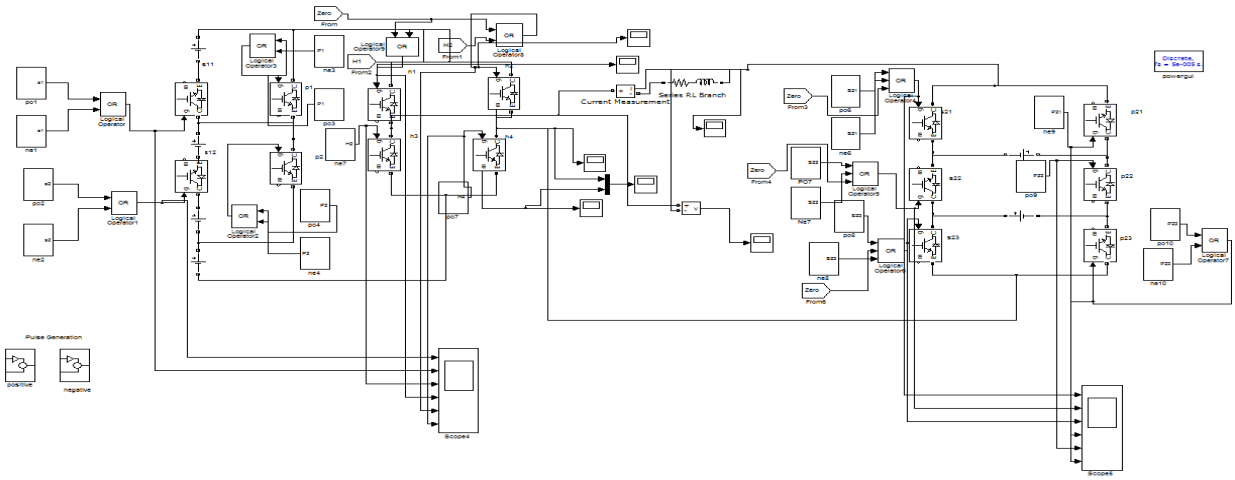

Fig.8 Simulation circuit

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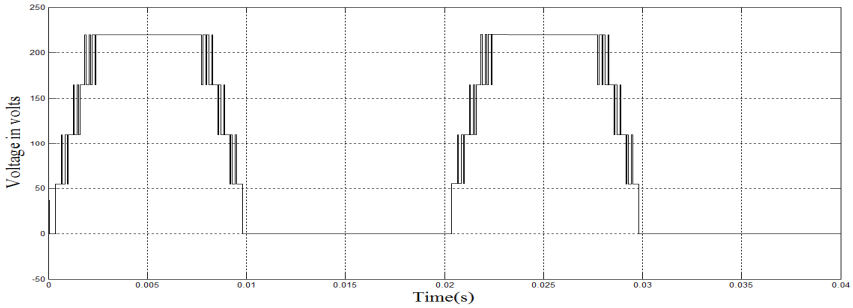

Fig. 9 V_{0max} of SDMLI

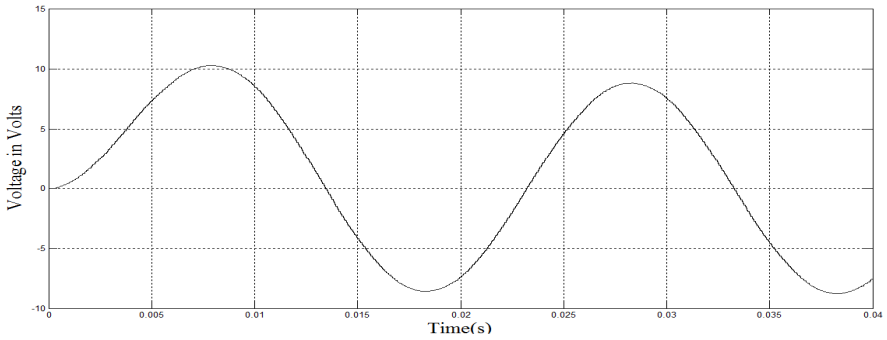

Fig. 10 Output pulse current given to switches

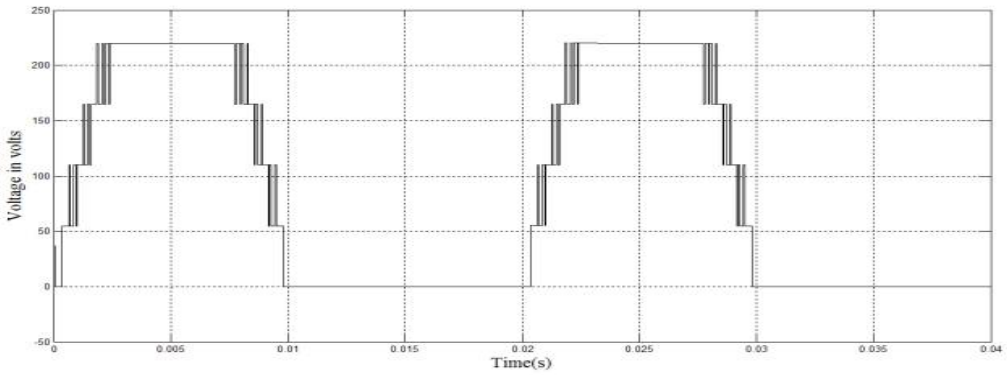

Fig. 11 $V_{0\ max}$ of Packed H Bridge

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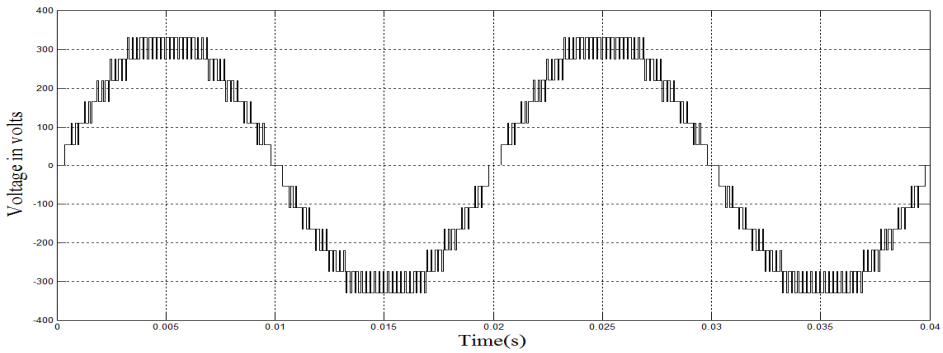

Fig. 12 simulated output waveforms for proposed multilevel inverter

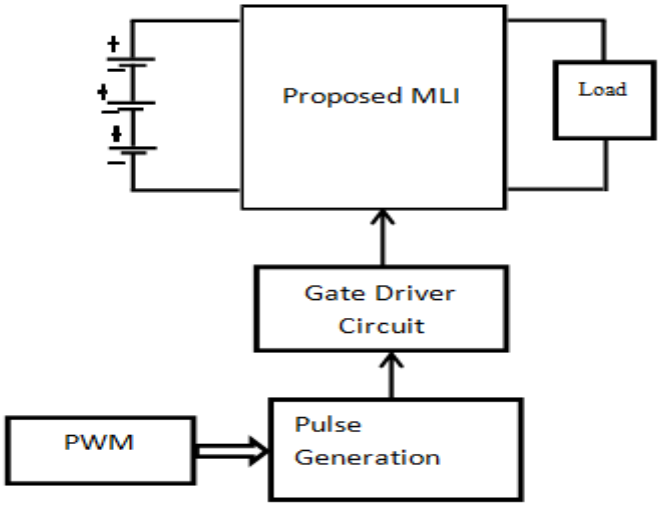

Fig. 13 Block diagram for proposed topology

The pulse width modulation which carries the signal to generate the pulses into the gate driver circuits to the proposed multilevel inverter. The load and dc voltage sources are connected to "U" shape packed cell and H-bridge. The PWM technique is mainly used for the output voltage control can be obtained without any additional components and also with this type of control, lower order harmonics can be eliminated or minimized along with its output voltage control. The filtering requirements are minimized as higher order harmonics can be filtered easily.

There will be six dc voltage sources are in new proposed topology. Each sources carries 55 volt. It is generated in a single phase magnitude of dc sources. The RL load is used in this new topology. Because in the RL circuit using inductive filter to reduce the harmonics so we get sinusoidal waveform. Current always depends upon load. The freewheeling diode which is connected across RL.

V. CONCLUSION

In this paper, the novel symmetric multilevel inverter is proposed. This multilevel inverter can be implemented in industrial where the minimum switches are required. The voltage output and current is verified to confirm the performance of proposed multilevel inverter. The nearest level modulation technique is implemented. Future work on this proposed topology considers: (i) High voltage applications by cascading the proposed topology. (ii) In practical applications such as, Induction motor drives and FACTS controllers.

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