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MAC Architectures Based on Modified Booth Algorithm

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ABSTRACT: Presently there is a requirement for high speed applications of digital signal processing which need high speed low power, compact circuits. Multiplication and addition are the major needed operations for digital signal processing and similar circuits. This need is fulfilled by using new architectures for Booth algorithm and modified Booth algorithm. Modified Booth algorithm increases the speed of multiplication by reducing the number of partial products and carry save adder performs the sum of partial products which further reduces the delay and power. New architectures are designed and simulated for increase in speed.

KEYWORDS: CSA carry save adder, CLA Carry Look ahead Adder , MAC Multiplier and accumulator.

I.INTRODUCTION

The demand for high speed and efficient processing has been mounting as a result of growing computer and signal processing applications.The core of every processing system is its data path. Available statistics [3] has given clear indications that more than 70% of the instructions usually perform arithmetical and logical operations mainly consist of addition and multiplication in the data path of RISC and CISC machines. Multiplication based computation, which involve operations like Multiply and Accumulate and inner product most intensive arithmetic functions, currently implemented in many signal processing applications such as convolution, fast Fourier transform, filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of most signal/ instruction processing algorithms, so there is a need of speed efficient multiplier.

Also, low power consumption and area efficiency are among the most important criteria for the fabrication of any processing and high performance systems. Optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually contradictory, so that improving speed results mostly in larger areas also.

In our study, we propose the best solution to this problem by introducing a new efficient VLSI architecture of parallel Multiplier-and Accumulator (MAC) using hybrid approach for high-speed arithmetic operations. Since the accumulator that has the largest delay in MAC, the Carry Save Adder (CSA) and compressor techniques are used as one of the processing element to improve the overall performance.

As per in the previous work, the general Booth algorithm and CLA's are used in MAC operation for getting the efficient output results through pipeline scheme. But the problem rises by the general booth algorithm and CLA's in previous work by that pipeline scheme performance will be decreased. To rectify these problems this proposed method has been introduced the modified booth algorithm and CSA.

This study presents an efficient implementation of high speed multiplier, Radix-8 modified Booth multiplier algorithm. The parallel multipliers like radix 2 and radix 4 modified booth multiplier does the computations using lesser adders and lesser iterative steps.

However, the fact remains that the area and speed are two conflicting performance constraints. Hence, innovating increased speed always results in larger area. In this, we arrive at a better trade-off between the two, by realizing a marginally increased speed performance

The proposed MAC will show the better properties to the existing standard design in many ways and performance twice as much as the previous research in the similar clock frequency.

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The power reduction techniques adopted in this work, and we expect that the proposed MAC can be adapted to various fields requiring high performance such as the signal processing areas.

II. RELATED WORK

In this paper[13], the asynchronous floating-point arithmetic units consisting of adders/subtractors and multipliers are designed and compared based on the Balsa synthesis system. For the critical mantissa multiplication in the multiplier, the modified Booth algorithm (radix 2, 4, and 8) is adopted. A pipelined design of the multiplier is also presented to increase performance.
Proposed MAC showed the superior properties to the standard design in many ways and performance twice as much as the previous research in the similar clock frequency[9].
In this paper[10] a new MAC architecture to execute the multiplication accumulation operation, for digital signal processing and multimedia information processing efficiently was proposed. By removing the independent accumulation process that has the largest delay and merging it to the compression process of the partial products, the overall MAC performance has been improved almost twice as that of the previous work.
Proposed both radix- 4 and Radix-8 Booth encodings new Radix- 5 kogge stone adder is developed to reduce the delay[11]. Also some measures should be taken which minimize the area consumption.
In this paper[12]study of various parallel MAC architecture and then implementation of design of parallel MAC based on some Booth encodings such as Radix -4 Booth encoder and some final adders. Such as CLA, Kogge stone adder is carried out.
Presented an efficient implementation of high speed multiplier using the shift and adds method, Radix-8 modified Booth multiplier algorithm[14]. The architecture includes a final adder with the size of 2 to perform a multiplication. It means that the operational bottle neck is induced in the final adder no matter how much delay.
Proposed for high speed and low power[15]. For improving the speed and to reduce the dynamic power there is a need to reduce the glitches 1-0 transition and spikes 0- 1 transition. Adder designed using spurious power suppression technique (SPST) which avoids the unwanted glitches and spikes.
A new MAC architecture to execute the multiplication - accumulation operation, which is the key operation, for digital signal processing and multimedia information processing efficiently, was proposed. By removing the independent accumulation process that has the largest delay and merging it to the compression process of the partial products[16], the overall MAC performance has been improved almost twice as much as in the previous work.
In this paper[17], a new architecture for a high speed MAC, in which computations of multiplication and accumulation are combined and hybrid type CSA structure is used to reduce the critical path and improve output rate is achieved
Present an efficient implementation of high speed multiplier using the shift and add modified Booth algorithm[18]. The adder used is look ahead carry adder. The compression tree along with the carry look ahead adder has reduced the hardware overhead and power consumption.
Proposed architectures of the high-speed low power and less area of modified Booth Wallace MAC. CSLA has comparatively low value of critical path length hence less combinational path delay but it has higher no. of leaf cell count and combinational path area[19]. It also has high dynamic power than CLA and CSKA. So CLA and CSKA architectures can be used for low power applications as it has low value of dynamic as well cell leakage power.
A new multiplier Accumulator architecture based on high accuracy modified Booth algorithm [19]. In this paper, a new MAC architecture is developed for high speed performance. The performance improvement is achieved by merging CSA and accumulator. MAC architecture is synthesized with 180 nm standard CMOS library using cadence SOC encounter.
Multipliers with high speed are essential of digital applications for example signal processing. A new architecture of multiplier-and-accumulator (MAC) was proposed for high-speed arithmetic. By combining multiplication with accumulation the performance was improved[20]. In Modified booth algorithm technique the modified booth encoder will reduce the number of partial products. Even in general purpose processors high speed multipliers are most required to provide a physically compact, good speed and low power consuming chip. To save significant power consumption of a VLSI design, it is a good direction to reduce its dynamic power. This paper proposes the spurious power suppression technique (SPST) in VLSI will reduce the power consumption of the system significantly.

In this paper[21], a new architecture of multiplier-and-accumulator (MAC) for high-speed arithmetic proposed. By combining multiplication with accumulation and devising a hybrid type of carry save adder (CSA), the performance

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was improved. The proposed CSA tree uses 1's-complement-based radix-2 modified Booth's algorithm (MBA) and has the modified array for the sign extension in order to increase the bit density of the operands. The CSA propagates the carries to the least significant bits of the partial products and generates the least significant bits in advance to decrease the number of the input bits of the final adder.

III.IMPORTANCE OF THE PROPOSED WORK

By showing the performance improvement of the Proposed MAC more than twice than the earlier research it can have the importance as below.

- It is expected that the proposed MAC can be adopted to various fields requiring high performance such as the signal processing areas.
- MAC unit designed can be used in efficient filter realization for high speed DSP applications.
- Efficient MAC can have extension to design floating point arithmetic, signed arithmetic and Decimal arithmetic.
- Multimedia processing is the one of the major area requires high speed multiplier.
- Further the designed MAC can be used in many areas like numerical coprocessors, calculators (Pocket and graphics etc.), filtering, modulation and demodulation etc.

In this work an efficient architecture is proposed for high speed arithmetic multiplication. Algorithm for MAC is Booths radix-8 algorithm, Modified Booths multiplier, 32 bit Wallace tree multiplier, which improves speed.
The Wallace tree basically multiplies two unsigned integers. The conventional Wallace tree multiplier architecture comprises of an AND array for computing the partial products, a carry save adder for adding the partial products so obtained and a carry propagate adder in the final stage of addition. In the proposed architecture, partial product generation and reduction is accomplished by the use of booth algorithm, 3:2, and 4:2, 5:2 compressor structures.

IV.PROPOSED IMPLEMENTATION

The proposed MAC is implemented and analyzed. Then it would be compared with some previous researchers. First the amount of used recourses in implementing the hardware is analyzed theoretically and experimentally then the delay of the hardware is analyzed. Finally the pipeline stage is defined and performance is analyzed based on the pipelining scheme. Implementation result from each section will be compared with standard design [4] and Equibaly's design [3], each of which has the most representative parallel MBA architecture.

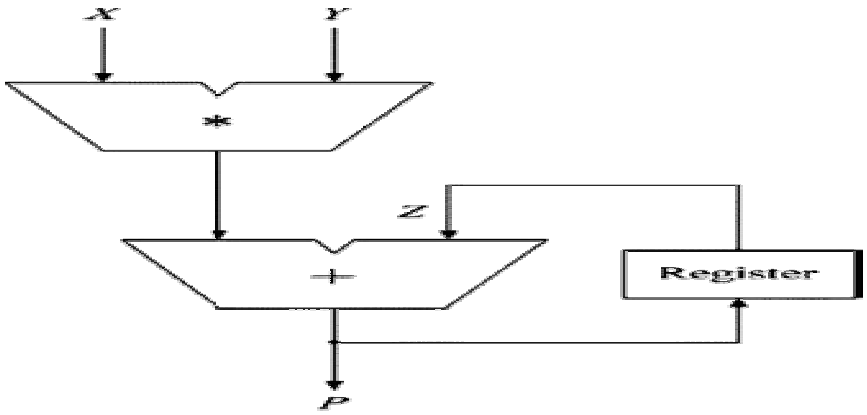

Fig.1 General Hardware architecture of MAC

Overview of MAC:
In this MAC operation a multiplier can be divided into 3 parts. The first is radix – 8 booth encoding in which the partial product is generated from the multiplicand (x) the multiplier (y).The second is adder array or partial product

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compression. The last is the final addition in which final multiplication result is produced by adding the sum & the carry.

General hardware architecture of this MAC is below in fig. -1

General hardware architecture of the MAC executes the multiplication operation by multiplying the input multiplicand X and multiplier Y. This is added to the previous multiplication result Z as the accumulation step if accumulation is needed.

The N-bit 2's complement binary number can be expressed as

$$X = -2^{N-1}x_{N-1} + \sum_{i=0}^{N-2} x_i 2^i, \qquad x_i \in 0,1.$$

……..(1)

If (1) is expressed in base-4 type redundant sign digit form in order to apply the radix-8 Booth's algorithm.

$$X = \sum_{i=0}^{N/2-1} d_i 4_i$$

……..(2)

Where

$$d_i = -2x_{2i+1} + x_{2i} + x_{2i-1}.$$

…… (3)

If (2) is used, multiplication can be expressed as

$$X \times Y = \sum_{i=0}^{N/2-1} d_i 2^{2i} Y.$$

…… (4)

The multiplication - accumulation result are then

$$P = X \times Y + Z = \sum_{i=0}^{N/2-1} d_i 2^i Y + \sum_{j=0}^{2N-1} z_i 2^i.$$

……. (5)

The MAC architecture implemented by (5) is called the standard design [4].

V. BOOTH ALGORITHM FOR PARTIAL PRODUCTS GENERATION

To generate and reduce the number of partial products of multiplier, proposed modified Booth Algorithm has been used, In the proposed modified Booth Algorithm, multiplier has been divided in groups of 4 bits and each groups of 4

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bits have been operation according to modified Booth Algorithm for generation of partial products 0, ±1A, ±2A, ±3A, ±4A, ±5A, ±6A, ±7A . These partial products are summed using compressors in structure of Wallace Tree.

In radix-8 Booth Algorithm, multiplier operand B is Partitioned into 11 groups having each group of 4 bits. In first group, first bit is taken zero and other bits are least Significant three bit of multiplier operand. In second group, first bit is most significant bit of first group and other bits are next three bit of multiplier operand. In third group, first bit is most significant bit of second group and other bits are next three bit of multiplier operand. This process is carried on. For each group, Partial product is generated using multiplicand operand A. For n bit multiplier there is n/3 or [n/3 + 1] groups and partial products in proposed modified Booth Algorithm radix-8.

VI. IMPLEMENTATION

A multiplier design consists of three operational steps. The first is Booth encoding in which a partial product is generated from the multiplicand X and the multiplier Y. The second is adder array or partial product compression to add all partial products and convert them into the form of sum and carry. The last is the final addition in which the final multiplication result is produced by adding the sum and the carry. When the multiplier results are to be accumulated, an additional step is needed, as shown in figure 2

In our design we are using more advanced features to enhance the parallelism. Block diagram of multiplier is shown in figure 3. Modified Booth encoder reduces partial products by half, so we are required to sum partial products. Here we are using compressors so it reduces the number of partial product sum stages.

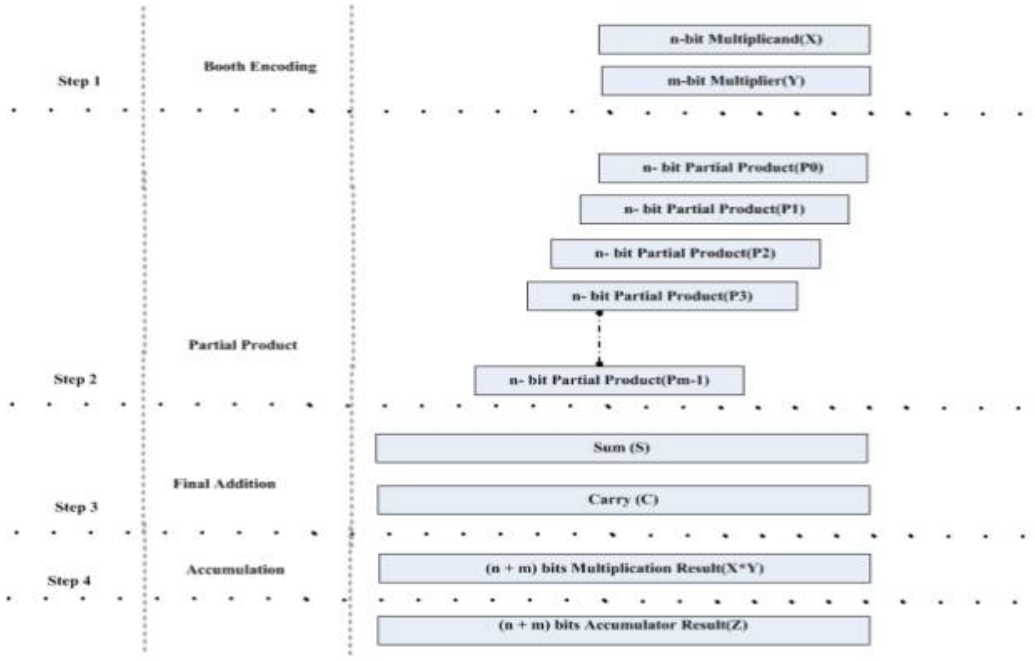

Fig.2.Booths's Multiplier steps

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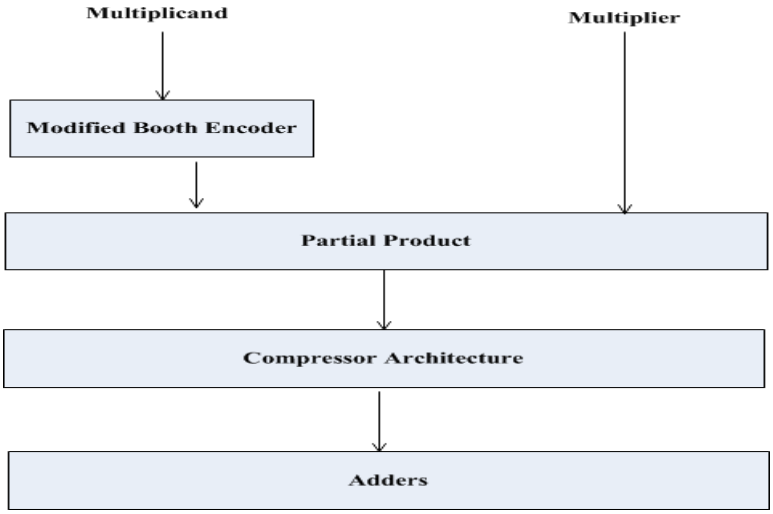

Fig.3.Block diagram of Booths Multiplication

VII.RESULTS

The simulation results are shown below with timing diagrams.
RTL Schematic:

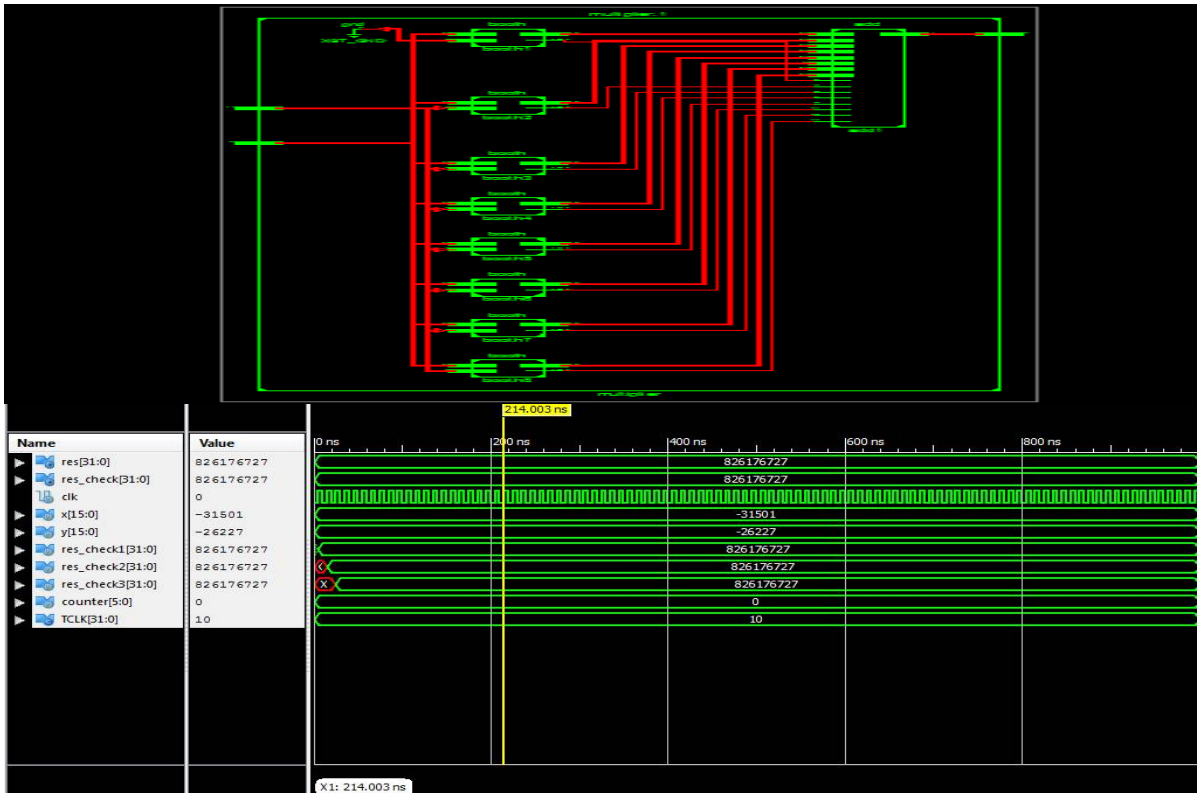

Fig. 4. Simulation waveforms

The multiplication between two 16 bit numbers is obtained by simulation is shown in above figure.4.

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VIII. CONCLUSION

In this paper, a new multiplier architecture is proposed, which is a most required for digital signal processing and multimedia communication applications. This models consist of modified booth algorithm shown in fig1.along with carry save adder and Wallace tree. The importance of the existing design shows the reduction of the partial products by using the modified booth algorithm for parallel processing.The simulation outcomes are shown in fig.4 where the 16 bit inputs are given and 32 bit output is obtained.This simulation shows that without any extra overhead positive and negative numbers can be treated equally.

REFERENCES

1. S. Waser and M.J. Flymn, "Introduction to arithmetic for Digital system designers," New York: Holt, Rinechart and Winston, 1982.
2. J J F Cavanagh, Digital computer arithmetic. New York: Mc GrawHill 1984.
3. F. Elguibaly, "A fast parallel multiplier–accumulator using the modified Booth algorithm," IEEE Trans. Circuits Syst., vol. 27, no. 9, pp. 902–908, Sep. 2000.
4. A.R. Omondi, Computer arithmetic systems, Eagle wood cliffs. NJ: Printice Hall. 1994.
5. J.Fadavi Ardekani, " Booth encoded multiplier generator using optimize Wallace tree," IEEE Transactions on VLSI Systems, vol.1, pp.120-125, 1993.
6. A. Fayed and M. Bayoumi, "A merged multiplier-accumulator for high speed signal processing applications," Proc. ICASSP, vol. 3, pp. 3212–3215, 2002.
7. P. Zicari, S. Perri, P. Corsonello, and G. Cocorullo, "An optimized adder accumulator for high speed MACs," Proc. ASICON 2005, vol. 2, pp. 757–760, 2005.
8. Young Ho seo, Dong wook kim, "A new VLSI Architecture of parallel multiplier Accumulator based on Radix 2 Modified Booth algorithm," IEEE transactions on very large scale integration (VLSI) systems, vol. 18, no.2, pp. 201-208 , Feb.2010.
9. M.V. Sathish, M. Sailaja, "Vlsi Architecture Of Parallel Multiplier– Accumulator Based On Radix-2 Modified Booth Algorithm," International Journal of Electrical and Electronics Engineering (IJEEE), vol.1, Issue-1, 2011
10. P. Sasi Bala, S. Raghuvendra, "A new VLSI architecture of parallel multiplier – Accumulator based on Radix – 2 modified Booth algorithm," International Journal of Instrumentation, control and Automation, vol.1, no.2, pp.91-97, 2011.
11. Sankey Goel, R.K. Sharma, "Parallel MAC based on Radix 4 & Radix 8 Booth encodings," International Journals of Engineering & Technology, vol.3, no.8, pp.6692-6697, 2011.
12. K. Hima Bindu, K. Bala Souri, K. V. Ramana Rao, " MAC architecture Accumulator based on Booth encoding parallel multipliers,"International journals of soft computing and Engineering,vol.1, no.5, pp. 385–388, Nov.2011.
13. Ren-Der Chen; Yu-Cheng Chou; Wan-Chen Liu, "Comparative design of floating-point arithmetic units using the Balsa synthesis system," Integrated Circuits (ISIC), 2011 13th International Symposium on , vol., no., pp.172,175, 12-14 Dec. 2011
14. Rashmi Ranjan et al., "A New Vlsi Architecture Of Parallel Multiplier Based On Radix-8 Modified Booth Algorithm Using Vhdl," International Journal of Computer Science & Engineering Technology (IJCSET), Vol. 3 No. 4 April,2012
15. Adalanki Purna Ramesh, Dr. A. V. N. Tilak, Dr. A. M. Prasad, "Efficient implementation of 16 bit multiplier, Accumulator using Radix – 2 modified Booth algorithm and SPST adder using Verilog," International journal of VLSI design and communication systems, vol. 3, no.3, pp.107-118, Jun. 2012.
16. S.Jagadish, S. Venkatachary, "Design of parallel multiplier Accumulator based on Radix-8 modified Booth algorithm with SPST," International journal of Engineering Research and application, vol.2, no.5, pp.425-435,Sept.Oct. 2012.
17. B.Jyothirmai, M. Premalatha, "Design and implementation of parallel MAC by Booth algorithm," International Journals of scientific Research,vol.1,no.6, pp.78-79,Nov.2012.
18. Harilal, Durga Prasad, "High speed arithmetic Architecture of parallel multiplier Accumulator based on Radix-2 modified Booth algorithm," International journals of computational Engineering research, vol.2, no.8, pp.28-38, Dec.2012.
19. Naveen Kumar, Manu Bansal, Amandeep kaur, "Speed Power and Area Efficient VLSI Architectures of Multiplier and Accumulator," nternational Journal of Scientific & Engineering Research,vol.4, Issue 1, Jan-2013.
20. J. Y. Yahwanth Babu, P. Dinesh Kumar, "A new multiplier Accumulator architecture based on high accuracy modified Booth algorithm,"International journal of advanced research in computer Engineering & Technology, vol.2,no.3,pp.1036-1040,Mar 2013.
21. Pratibhadevi Tapashetti, Dr.Rajkumar B Kulkarni, "Implementation of High Speed MAC VLSI Architectures, Based on High Radix Modified Booth Algorithm", International conference on advances in electronics ,computer and mathematical sciences(ICIREMPS-2016) Sagar Institute of Research and Technology(SIRT) Bhopal,MP,India,26 to 28 FEB *2016*.
22. Pratibhadevi Tapashetti, Dr.Rajkumar B Kulkarni, "Efficient And Compatible VLSI Architecture Of Parallel Mac Based On High Radix Modified Booth Algorithm", 3rd International Conference onIET-IEEE-Electrical, Electronics, Engineering Trends, Communication, Optimization and Sciences (EEECOS)-2016, SASI Institute of Technology and Engineering ,Tadepalligudem ,Andrapradesh,India, 2016/5