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# Multilevel Inverter Fed Permanent Magnet Synchronous Machine Performance Analysis at Different Modulation Frequencies

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**ABSTRACT**: Permanent magnet synchronous machine (PMSM) has over handiling capacity& good efficiency these motors eliminates the torque ripples caused by commutation and produce smooth torque. In normal PM motor drive fed with pulse width-modulated voltages which cause sharp voltage (dv/dt) appear across the motor terminals this may. cause the break down of motor insulation.

This problem can be resolute by applying changeble voltage with low dv/dt by using of multilevel inverter topology. Multilevel converters can operate at both fundamental and higher switching frequencies, low switching losses, improve power quality, higher voltage capability. In cascaded H- Bridge multilevel inverters individual H-bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower voltage higher-frequency.

Different PWM techniques like phase shifted carrier PWM (PSCPWM) and level shifted carrier PWM (LSCPWM) used for the switching control of multilevel converters. In level shifted carrier PWM, in phase disposition (IPD), alternative phase opposite disposition (APOD) and phase opposite disposition (POD) modulating techniques are analyzed the THD levels for different values of modulation index and switching frequency by using MATLAB/ SIMULINK. Finally better modulating technique is applied to drive the nine level cascaded-H Bridge fed Permanent Magnet Synchronous Motor drive.

**KEYWORDS**- Multilevel converter, permanent magnet synchronous motor, cascaded H-bridge inverter, nine level inverter, level shifted and phase shifted PWM technique.

### I. INTRODUCTION

PM synchronous motors are widely used in low and mid power applications robotics adjustable speed drives attractive solution for servo drive in k-w the range industrial applications. The high-quality permanent magnet materials have high flux density, high coercivity. Samarium - cobalt (SmCo), neodymium iron-boron (NdFeB) magnates used for their low cost. The concept of multilevel converters has been introduced since 1975. A multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. A multilevel inverter is a power-electronic system that generates a desired output voltage by several PWM techniques. Here we use phase shifted PWM, level shifted PWM. In level shifted PWM i) Phase disposition(PD), ii) Alternative Phase Opposition Disposition(APOD) iii) Phase Opposition Disposition(POD). The advancement in power electronics technology has made it possible to vary the frequency of the voltage. Thus, it made more extensive use in variable speed drive applications and the control of PM motor has become easier and cost effective, with the possibility of operating the motor over a wide range of speeds and still retains a good efficiency.



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### II. MATHEMATICAL MODELING OF PERMANENT MAGNET SYNCHRONOUS MOTOR

The following modeling equations are developing the modeling of a PMSM:



Fig1:Three-phase two-pole PMSM

$$\begin{array}{rcl} V_{qs} = & \mathsf{R}_q i_q + \rho \lambda_q + \omega_r \lambda_d(1) \\ V_{ds} = & \mathsf{R}_d i_d + \rho \lambda_d - \omega_r \lambda_q(2) \\ & \lambda_q = \mathsf{L}_q i_q(3) \\ \lambda_d = & \mathsf{L}_d i_d + \lambda_m \ (4) \\ \mathsf{T}_e = & (3/2) (\mathsf{P}/2) (\lambda_d i_q - \lambda_q i_d) (5) \\ \mathsf{P}_e = & \omega_{rm} \mathsf{T}_e = & (3/2) (\omega_r) (\lambda_d i_q - \lambda_q i_d) \ (6) \\ & \omega_{rm} = & (\omega_r) (\mathsf{P}/2) (7) \\ \mathsf{T}_e = & \mathsf{T}_l + \mathsf{T}_d + \mathsf{B} \omega_{rm} + \mathsf{J} \rho \omega_{rm} (8) \end{array}$$

#### **III. CASCADED H-BRIDGE INVERTER**

The single H-bridge is shown in Figure 2. A single H-bridge is a three-level inverter. Each single-phase full-bridge inverter generates three voltages at the output0,  $+V_{dc}$  and  $-V_{dc...}$  A two level inverter generates an output voltage with two values ( $+V_{dc}$  &  $-V_{dc}$ ) with respect to the negative terminal of capacitor.the different level H-bridge cells are connected in series.The cascaded voltage waveform is the sum of the inverter outputs.

Cascaded H-Bridge inverters have less number of switches to made multilevel inverter compared to other topologies used. The switches used in different topologies are shown in Table.1. The three level inverter generates three voltages, the word multilevel inverters starts with the three level inverter.



Fig 2: Single H-Bridge Topology

Increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform. This has reduced harmonic distortion.



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Inverter toplogy	Diode clamped MLI	Flying capacitor MLI	Cascaded H-bridge		
	L		MLI		
Main switchingdevices	2(m-1)	2(m-1)	2(m-1)		
MainDiodes	2(m-1)	2(m-1)	2(m-1)		
ClampingDiodes	(m-1)(m-2)	0	0		
DC busCapacitors	(m-1)	(m-1)	(m-1)/2		
Balancing capacitors	0	(m-1)(m-2)/2	0		
Here m is level of inverter					

Table1.Comparison of Components required in Multilevel Inverter configuration

Fig3. Shows the nine level cascaded H-Bridge multilevel inverter. The cascaded bridge multilevel inverter uses separate DC input source for the synthesize of desired voltage from several independent dc voltage sources, which may be obtained from batteries, fuel cells, or solar cells. This topology avoids use of extra clamping diodes or balancing capacitors.

#### IV MULTILEVEL INVERTER

The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. For 9-level inverter cascade H-bridge Inverter 4 separated DC sources with 4 full bridge shown in fig 3. The phase voltage is

$$van = v_{a1} + v_{a2} + v_{a3} + v_{a4}$$

$$V_{dc1} = \begin{bmatrix} S_{1} & S_{2} & S_{4} \\ S_{2} & S_{4} & S_{4} \\ S_{3} & S_{4} & S_{4} \\ S_{4} & S_{4} & S_{4} \\ S_{5} & S_{6} & S_{4} \\ S_{5} & S_{6} & S_{6} \\ S_{7} & S_{8} & S_{4} \\ S_{7} & S_{8} &$$

Fig 3.nine level inverter



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we observe the nine level inverter switching operation and with respective voltages from Table 2.

	Table2: shows the switching states of nine level inverter					
.NO.	SWITCHES OFF	SWITCHES ON	OUTPUT			
1	$S_2S_4S_5S_7$	$S_1S_3S_6S_8$	$4V_s$			
2	$S_1S_2S_4S_7$	$S_3S_4S_6S_7$	3V <sub>s</sub>			
3	$S_4S_5S_6S_7$	$S_1S_2S_3S_8$	$2V_s$			
4	$S_2S_3S_4S_5$	$\mathbf{S}_1 \mathbf{S}_6 \mathbf{S}_7 \mathbf{S}_8$	Vs			
5	$S_1S_2S_3S_4$	$S_5S_6S_7 S_8$	0			
6	$S_5S_6S_7 S_8$	$S_1S_2S_3S_4$	0			
7	$S_1S_6S_7S_8$	$S_2S_3S_4S_5$	-V <sub>s</sub>			
8	$S_1S_2S_3S_8$	$S_4S_5S_6S_7$	-2V <sub>s</sub>			
9	$S_3S_4S_6S_7$	$S_1S_2S_4S_7$	-3V <sub>s</sub>			
10	$S_1S_3S_6S_8$	$S_2S_4S_5S_7$	$-4V_s$			

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#### V. SINUOIDAL PWM TECHINIQUES USED IN MULTI LEVEL INVERTER

In this sinusoidal PWM techniques have various strategies using more than one triangular wave as carrier and the reference wave is sinusoidal as shown fig 4.



#### A. PHASE SHIFTED PWM (PSPWM)

A multilevel inverter with m voltage levels requires (m-1) triangular carriers. In the PSPWM, all the triangular carrier waves have same frequency and the same peak to peak amplitude, but there is phase shift between any two adjacent carrier waves, given  $\phi_{cr} = 360^{\circ}/(m-1)$  the gate signals generated by comparing the modulating wave with the carrier waves.





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For nine level inverter 8 triangular carriers are needed with a 45<sup>o</sup> phase displacement between two adjacent carriers. In this case the phase displacement for  $V_{cr1} = 45^{\circ}$ ,  $V_{cr2} = 90^{\circ}$ ,  $V_{cr3} = 135^{\circ}$ ,  $V_{cr4} = 180^{\circ}$ ,  $V_{cr5} = 225^{\circ}$ ,  $V_{cr6} = 270^{\circ}$ ,  $V_{cr7} = 315^{\circ}$ ,  $V_{cr8} = 360^{\circ}$ . Fig 5 show phase shift PWM.

### B. LEVEL SHIFTED PWM(LSPWM)

a. Phase disposition (PD) where all the carrier signals are in phasecarrier signal frequency is 4 times greater than sinusoidal frequency as shown in fig: 5.



b. Phase Opposition Disposition (POD) where the carrier signals above the zero line of sinusoidal modulating waveform are 180 out of phase with those below the zero line as shown in figure: 6



c. Alternative Phase Opposition Disposition (APOD), where each carrier signal is phase shifted by 180 from its adjacent carriers as shown in figure: 7



Fig 7: Alternative Phase Opposition Disposition

#### VI. RESULTS AND DISCUSSION

In fig 8 shows the speed difference of Permanent magnet synchronous machine fed with the five level inverter using phase shifted PWM technique and nine level inverter using phase shifted PWM technique.



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Fig8: Speed comparison with conventional and PSCPWM

In fig 9 shows the speed difference of Permanent magnet synchronous machine fed with the five level inverter using level shifted(APOD) PWM technique and nine level inverter using level shifted(APOD) PWM technique .



The Permanent magnet synchronous machine get supply from three phase nine level inverter output voltage shown in fig 10.



Fig 10.3-phase nine level inverter output waveform

The Total Harmonic Distortion(THD) of output voltage from nine level inverter is from fig 11



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Fig 11.Nine level Phase shift carrier PWM THD

The Total Harmonic Distortion (THD) of output voltage from five level inverter is shown in fig 12.



Fig 12. Fivelevel Phase shift carrier PWM THD

due to the reduction of Total Harmonic Distortion (THD) in supply voltage Permanent magnet synchronous machine performance is improved. We observe output voltage Total Harmonic Distortion (THD) difference for 9-level inverter and 5-level inverter at different modulation techniques from table 3.

Name of PWM	Output voltage THD	
technique	9-level	5-level
PSCPWM	12.15%	23.77%
PDPWM	12.65%	22.71%
APODPWM	12.18%	23.92%
PODPWM	14.71%	22.23%

Table 3.output voltage THD at different modulation techniques

### **VII. CONCLUSION**

In this paper simulation results shows that comparison of five level and nine level inverter fed permanent magnet synchronous Machines different modulation techniques. This is done by proper switching frequency. i.e. phase shifted carrier PWM (PSCPWM) and level shifted carrier PWM (LSCPWM) are implemented and analyzed the THD values. In level shifted carrier PWM (a) in phase disposition (IPD), (b) alternative phase opposite disposition (APOD) and (c)



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phase opposite disposition (POD) modulating technique is applied. Compared to five level permanent magnet synchronous Machines performance of 9-level H-bridge fed permanent magnet synchronous Machines.

#### REFFERENCES

- [1]L. Carrillo Arroyo "Modeling And Simulation Of Permanent Magnet Synchronous motor drive system "University Of Puerto Rico Mayaguez Campus 2006
- [2]Ebrahim Babaei "A Cascaded Multilevel converter Topology with Reduced Number of switches", IEEE Trans. Power Electron vol.23,no.6, Nov 2008
- [3] P. Satheesh Kumar, S.P. Natarajan, Alamelu Nachiappan, and B. Shanthi, "Performance evaluation of Nine Level Modified CHB Multilevel Inverter for Various PWM Strategies," IJMER. Vol. 3, no. 1, pp. 2758–2766, Sep - Oct. 2013.
- [4] M. Kavitha, A. Arunkumar, N. Gokulnathand S.Arun "New Cascaded H-Bridge Multilevel inverter Topology with Reduced Number of Switches and Sources" IOSR Journal of lectrical and Electronics Engineering (IOSR-JEEE) ISSN: 2278-1676 Volume 2, Issue 6 PP 26-36, (Sep-Oct. 2012).
- [5] Hemish R. Choksi, and Hiren Brahmbatt "Analysis AndSimulation Of Cascaded H-Bridge 9-Level inverter using Phase-Shifted PWM Technique For Induction Motor Drive"international Journal For Technological Research In Engineering Volume 3, Issue 4, december-2015.
- [6] B. P. Ganthia, P. K. Sahu, and A. Mohanty, "Minimization of Total Harmonic DistortionUsing Pulse Width Modulation Technique" IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) Volume 10, Issue 3 Ver. IV (May–Jun.2015), PP01-12.
- [7] Vijayalakshmi, and M. Vijaykumar, "Development of multi carrier PWM technique for five level voltage source inverter", G. Received 07 January 2015; accepted 20 January 2015
- [8] Mahajan Sagar Bhaskar Ranjana, Pandav Kiran Maroti, RuchitaMaheshwari, and Pachagade Ruchi M"Multilevel inverter with level shifting SPWM Technikque using Fewer number of switches for solar applications" Volume: 04 Issue: 10 | Oct-2015
- [9]Pablo Cossutta, Miguel Pablo Aguirre, Andrés Cao, Santiago Raffo and María Inés Valla, "Single-Stage Fuel Cell to Grid Interface With multilevel Current-Source Inverters"IEEE transactions on industrial electronics, vol. 62, no. 8, august 2015
- [10] Divyesh J Vaghela and Himanshu N Chaudhari, "Investigation of design, analysis and performance of hysteresis current control PMSM drive"International Conference on Electrical, Electronics, Signals, Communication and Optimization (EESCO) – 2015
- [11]J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, control and applications," IEEE Trans. Power Elec1rrn., vol. 49, no. 4, pp. 724-738, Aug, 2002.
- [12] M.D. Manjrekar, P.Steimer, and T.A. Lipo. "Hybrid multilevel power conversion system: A competitive solution for high power applications". IEEE Transations on Industry Applications, vol.3 pp834-841, May/June 2000.