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High Speed DAC with Resampling Architecture

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ABSTRACT: This paper describes a high speed DAC with a resolution of 12 bit. It operates at a speed of 2 GSPS. It uses current steering segmented architecture with an R-2R ladder network for 6 LSB's and 6 MSB bits are thermometer decoded. It uses distributed resampling for all the current sources which improve performance of DAC by suppressing the non-linear glitches that occur at the time of transitions. The DAC achieves a SFDR of 53.45 dB at Nyquist. The DAC is designed such that it's INL and DNL are within 1 LSB. The DAC is designed using CMOS 65nm technology. The design is implemented using Cadence 6.1.4 Virtuoso tool.

KEYWORDS: DAC, GSPS, thermometer decoder, glitches, INL, DNL, SFDR, CMOS.

I. INTRODUCTION

The high resolution and high speed DAC's are important in generation of RF signal in wireless networking, mobile communication, radar and instrumentation application. By increasing the sampling rate and bandwidth of DAC, the design allows the system to be built with lesser RF mixing, filtering and switching components after DAC. If speed of DAC is large, then no further frequency translation is necessary which results in a simpler system with performance limited only by the DAC.

In this paper, a 12 bit high speed DAC is presented. In the next section, basics of current steering DAC and its topologies are discussed. In section III, the different blocks of high speed DAC such as thermometer decoder, latch and current cell are described. In section IV, simulation results is presented. Finally a conclusion and future scope is presented.

II. CURRENT STEERING DAC

Current steering architecture is most commonly used in high speed DAC design. This current steering DAC's has an array of current sources which steer the current to the output. There are three different topologies generally used in current steering architecture like binary weighted, unary weighted and segmented architecture.

A. BINARY WEIGHTED ARCHITECTURE:

An N-bit binary weighted converter has only N current mirrored sources with sizes of transistors varying from one unit to 2*N* units corresponding to one LSB current to 2*N* times the LSB current. This kind of design of current source array leads to the use of transistors with very large sizes in case of high resolution DACs. The disadvantage with this architecture is that the circuit is sensitive to matching errors and glitches this causes large DNL error at mid code transition. The advantage of using binary-weighted DAC is that the number of reference elements and switches are kept at the minimum value, thus saving the chip area.

B. UNARY WEIGHTED ARCHITECTURE:

In unary weighted converter, the digital input code is converted to thermometer code which controls the switches. Thermometer code has 2^N-1 bits for N bit digital code. Since elements are of equal size the matching becomes much simpler than a binary DAC. Thus, the advantage of using thermometer code is that the disturbance from glitches is minimized and so it can be used for high speed operation. Monotonicity is also guaranteed because we always add a reference source when ramping the output. This is the fastest and highest precision DAC architecture but at the expense of high cost, due to additional chip area and encoding circuits needed. This is used for low resolution otherwise the encoding circuits become too large.

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C. SEGMENTED ARCHITECTURE:

The Segmented DAC, which combines the thermometer coded principle for the most significant bits and the binary weighted principle for the least significant bits, is a popular architecture. In this way, a compromise is obtained between precision (by the use of the thermometer coded principle) and chip area with less number of resistors or current sources (by the use of the binary weighted principle). In this paper a 12-bit segmented DAC is implemented with 6 LSB's for binary and 6 MSB's thermometer decoded.

III. DAC DESIGN

The block of proposed 12-bit high speed DAC is shown in Fig 1. It consists of three main blocks namely 6 bit thermometer decoder, latch and current cell. The brief discussion regarding each block is presented in following section.

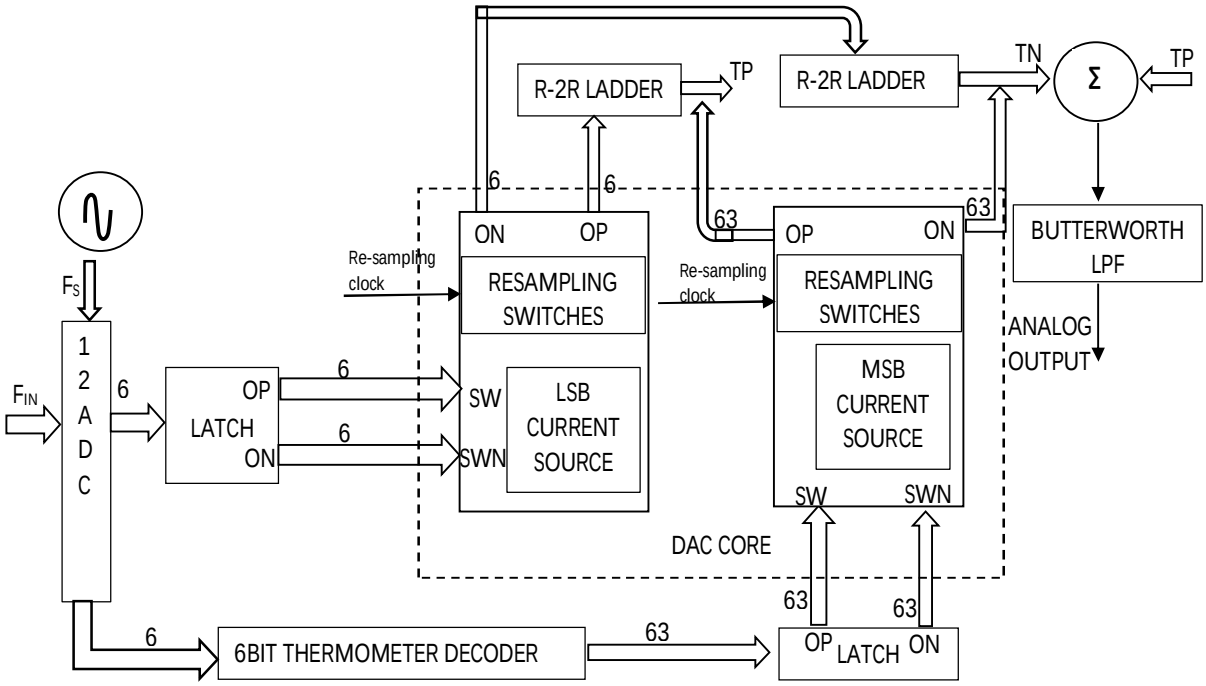

Fig. 1: Proposed DAC architecture.

The input analog signal is converted into digital by 12 bit ADC which has a sampling frequency of 2 GHz. The 6 MSB's are applied to thermometer decoder with generates 63 bit thermometer code. The proposed design uses distributed resampling which uses one switch for one current source all are driven by common clock. The resampling is done before currents are applied to R-2R ladder network so that each resampling operate on same unit current [1].

A. THERMOMETER DECODER:

By designing a thermometer decoder using standard cell library will have a disadvantage on operating speed which is limited by the timing constraints of the used cell [3]. Hence to obtain higher operating speed, the decoder is designed manually at the transistor level. The 6 bit thermometer decoder will generates 63 bit code. The decoder can be easily designed by using NAND and NOR gates itself. The design of CMOS 4 bit thermometer decoder is shown in Fig. 2. The 4 bit thermometer decoder is further used for designing 6 bit decoder using multipliers. The decoder has the supply voltage of 1.2V. Further to increase the INL and DNL dynamic element matching of thermometer decoded 63 MSB current sources can be used. The analog mismatch at the output is randomized by switching ON and OFF current source that depends on the input digital code in a sequence by which harmonic coherence is reduced and make signal independent of noise, by which the SFDR of the analog output is improved [4].

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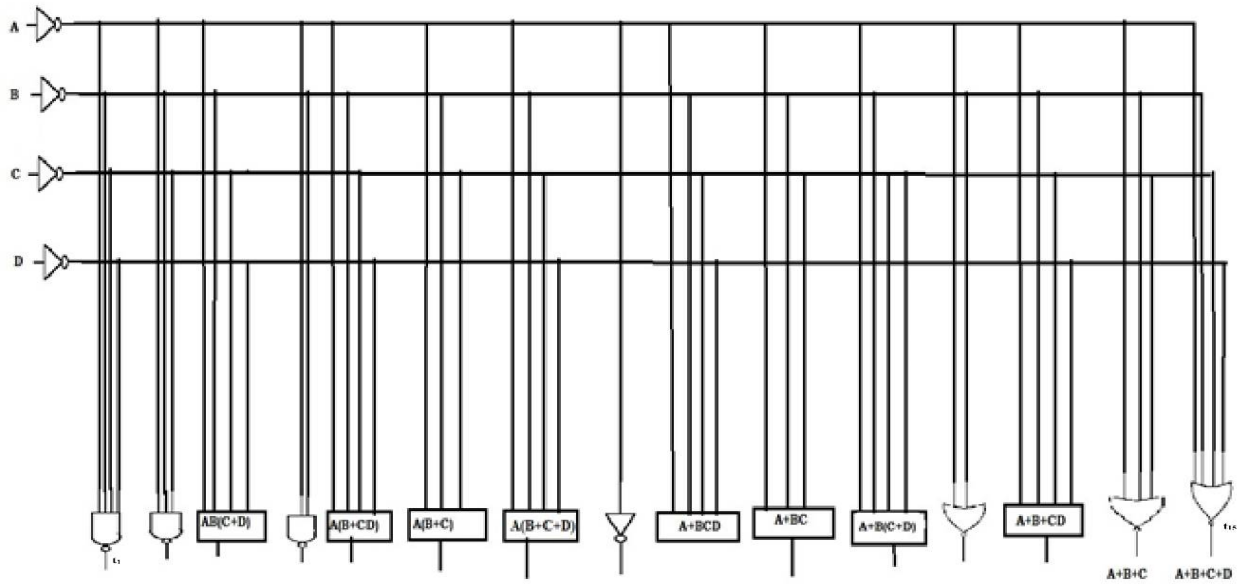

Fig. 2: 4 bit thermometer decoder.

B. LATCH:

The problem that commonly arises while operating the DAC is appearance of glitch in the output as an error which are mainly caused mistiming in the current signals at output of DAC. This glitches appear only during the transitions. The spectral content of the output signal will get corrupted because of this glitches. The one source of mistiming is difference in the arrival of digital bits at the input of encoder. Another source is differential logic delay between input and output of the encoder. This source of mistiming can be minimized by using latches.

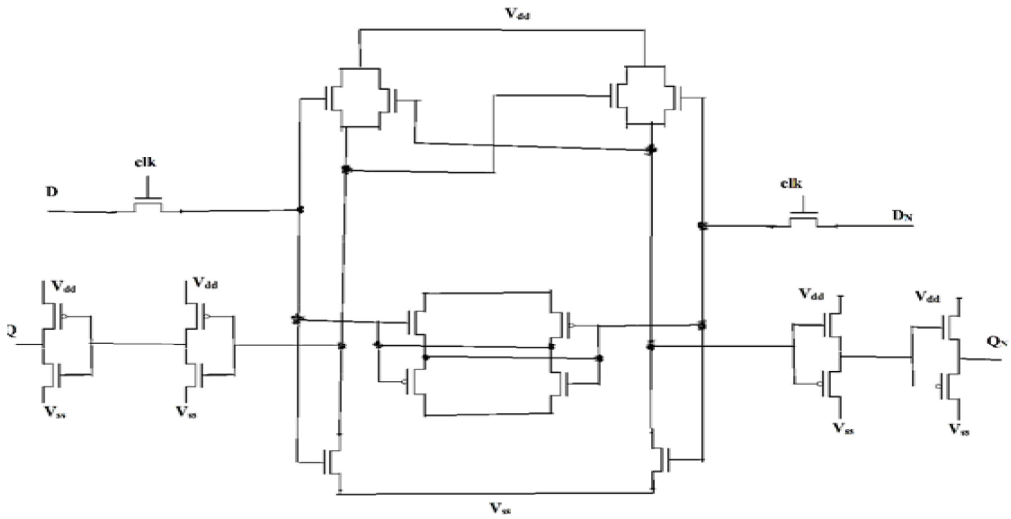

Fig. 3: D latch

C. CURRENT CELL:

The Fig. 4 shows the schematic of current cell with resampling architecture. Differential pair is used so that noise cancellation can be obtained. By the use of differential current cell even harmonics will reduced. In the Fig. 4 MOSFET M1 generates the required one LSB current. This MOSFET is regarded as current transistor. The size of transistor is determined in the following equation by considering the process variation.

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$$wl = \left(A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)^2}\right)/2\left(\frac{\sigma_I}{I}\right)^2 \quad (1)$$

Where $\left(\frac{\sigma_I}{I}\right)$ = standard deviation of unit current source,

A_β / A_{VT} = technology constants defined in foundry,

V_{GS}- V_T = gate overdrive voltage.

The area of current transistor M1 is fixed based on above considerations. The area of cascode transistor and switches must be minimized to reduce high frequency distortion. The cascode transistor is used to improve the impedance of current cell. It also isolates current transistor from the switches. Two additional current paths are added at source of M10 and M12 so that both transistors will not be switched off completely which means change in voltage at drain of M9 is not much observed [5]. So parasitic capacitance C_{gs} of M10 or M12 and C_{gd} of M6-M9 is not observed from the output node, hence this capacitances will not contribute to degradation due to distortion.

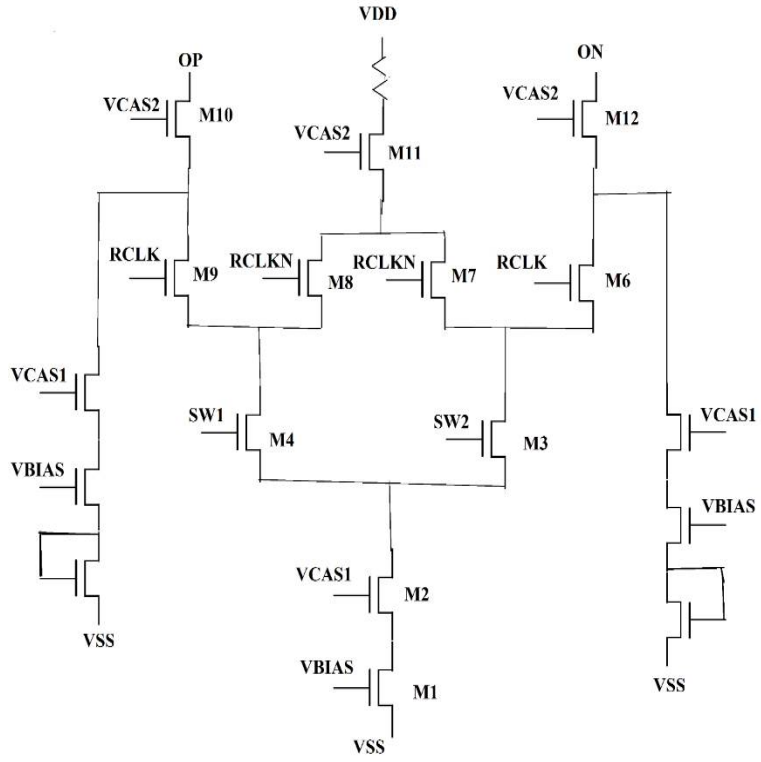

Fig. 4: Current cell

The resampling switch is used to pass the analog signal to the output only after the signal has settled to a final value [6]. Thus, the portion of the analog signal with glitches can be blocked by to the use of the switch. The resampling creates an RZ output waveform, so two DAC cores are used, clocked half a clock cycle apart. This recreates an NRZ waveform. Note that these two cores use the same data, so, unlike many DACs over 2 GSPS, this DAC acts as a single NRZ DAC clocked at the full sample rate and there are no interleaving spurs.

IV. SIMULATION RESULTS

The simulation of the entire design is carried out in Cadence Specter. The analog block has a supply voltage of 3.3V whereas the digital section is supplied with voltage of 1.2V. The DAC consumes a power of 42.37mW. The Monte Carlo simulation is performed on a single current source which shows the current deviation is within 1 LSB which means that INL and DNL are within 1 LSB. The Fig. 5 shows the Monte Carlo simulation of current source. The DAC has the digital input which 2 GSPS. The Fig. 7 shows the SFDR plot, which shows that DAC achieves a SFDR of 53.45 dB at Nyquist i.e. 667.48 MHz. The current cell has the output impedance of 1.518 MΩ at 2 GHz

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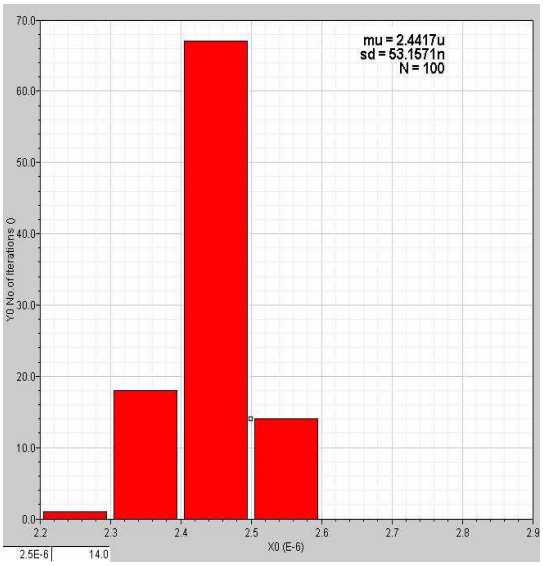

Fig. 5: Current source mismatch histogram

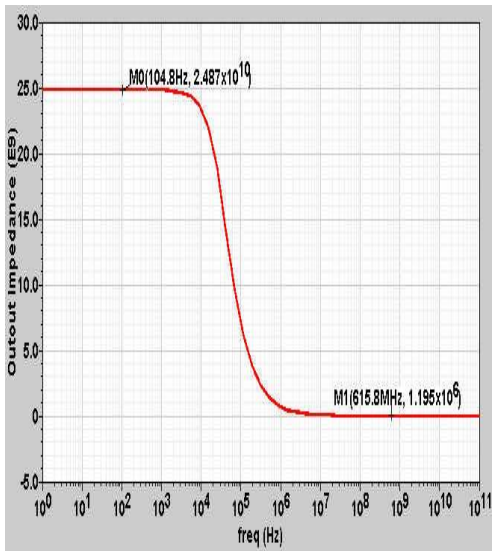

Fig. 6: Output impedance curve of current source

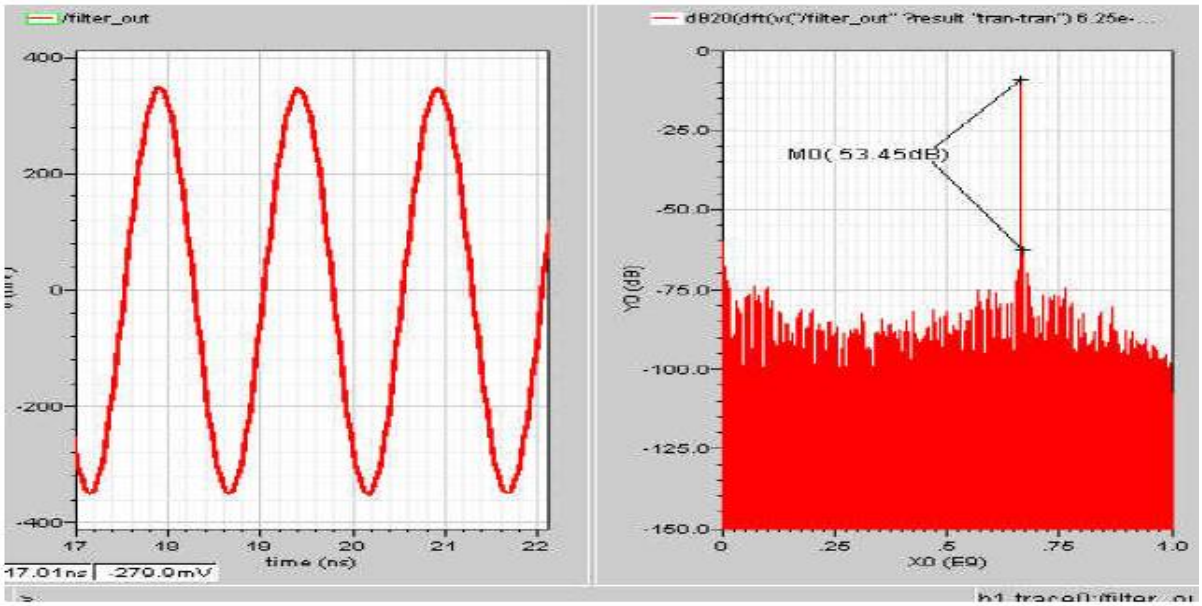

Fig. 7: Output of DAC and its SFDR

V. CONCLUSION & FUTURE SCOPE

In this paper, a 12 bit current steering high speed DAC with resampling architecture is presented. The proposed design achieves a SFDR of 53.45 dB at Nyquist. The design uses distributed resampling architecture to improve performance by suppressing non-linear glitches. The DAC is designed such that it's INL and DNL error are within 1 LSB. The output impedance of the current cell is calculated to be 1.518 MΩ at 2 GHz.

Further in order to improve INL and DNL dynamic element matching (DEM) for thermometer decoded MSB bits can be used. Calibration techniques can be used for compensating mismatch errors in the current cell. Further in order to increase the speed of DAC, Bi-CMOS technology can be used.

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