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An Efficient Design of Constant Delay Logic

M.Sankararao[1], R.Lalitha[2]

PG Student [VLSI], Dept. of ECE, Swamy Vivekananda Engineering College, Bobbili, A.P, India [1]

Assistant Professor, Dept. of ECE, Swamy Vivekananda Engineering College, Bobbili, A.P, India [2]

ABSTRACT*:* Static logic circuits allow versatile implementation of logic functions based on static, or steady-state, behavior of simple NMOS or CMOS structures [5]. This approach, however, may require a large number of transistors to implement a function, and may cause a considerable time delay. Dynamic CMOS circuit technique is introduced which allows us to significantly reduce the number of transistors used to implement any logic function. Feed through Logic (FTL) overcomes the drawback of using more transistors in domino logic, this logic can be implemented with same number of transistors used in dynamic logic.

To mitigate these problems, a new high-performance logic is proposed, which is called the "constant delay" (CD) logic. In this paper two methods are proposed to overcome the drawbacks. They are reducing the charging current with help of Leakage current replica circuit. For all circuits implementing by using back end tools 130 nm technology.

KEYWORDS: CD logic, FTL Transistor, power dissipation, power consumption, Domino logic

I. INTRODUCTION

CONSTANT DELAY LOGIC CONCEPT: To mitigate the above-mentioned problems, CD logic [1] is proposed with a schematic shown in Fig. 1(a). Timing block (TB) creates an adjustable window period to reduce the static power dissipation. Logic Block (LB) helps to reduce the unwanted glitch and also makes cascading CD logic feasible. A buffer implemented in CD logic with schematics of TB and LB is shown in Fig. 1. (b).

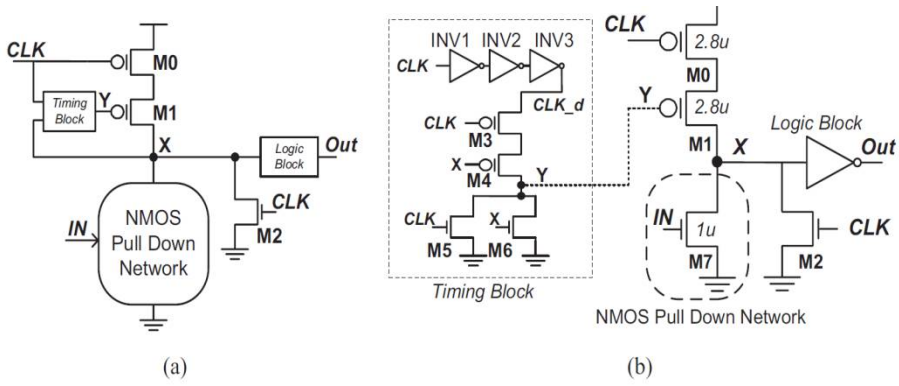

Fig. 1 CD logic (a) Block diagram (b) Buffer

1. CD Logic Operation*:* Fig. 2 depicts the corresponding CD logic timing diagram and flowchart. For simplicity, it is assumed that IN come from dynamic domino logic gates. When CLK is high, CD logic pre-discharges both X and Y to GND. When CLK is low, CD logic enters the evaluation period and three scenarios can take place: namely, the contention, C–Q delay, and D–Q delay modes. The contention mode happens when CLK is low while IN remains at logic "1." In this case, *X* is at a nonzero voltage level which causes Out to experience a temporary glitch. The duration of this glitch is determined by the local window width, which is determined by the delay between CLK and CLK_d. When CLK_d becomes high, and if *X* remains low, then *Y* rises to logic "1," and turns off *M1*.Thus the contention period is over, and the temporary glitch at Out is eliminated. C–Q delay mode takes places when IN make a transition from high to low before CLK becomes low.

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When CLK becomes low, *X* rises to logic "1" and *Y* remains at logic"0" for the entire evaluation cycle. The delay is measured by the falling edge of both CLK and Out: hence the name C–Q delay. D–Q delay mode utilizes the pre-evaluated characteristic of CD logic to enable high-performance operations. In this mode, CLK falls from high to low before IN transit, hence *X* initially rises to a nonzero voltage level. As soon as IN become logic "0," while *Y* is still low, then *X* quickly rises to logic "1." A race condition exists in this case between *X* and *Y*. If CLK_d rises much earlier than *X* and *Y* will go to logic "1," turn off *M1*, and result in a false logic evaluation. If CLK_d rises slightly slower than *X*, then *Y* will initially rise (thus slightly turns off *M1*) but eventually settle back to logic"0." CD logic can still perform the correct logic operation in this case; however, its performance is degraded because ofM1's reduced current drivability. Therefore, it is important to maintain a sufficient window width under process–voltage–temperature (PVT) variations. Compared to FTL, where the contention lasts for the entire evaluation period, TB effectively reduces CD logic's power consumption during the contention mode. The local window technique in the proposed CD gate allows designers to customize the window width for different logic expressions to achieve minimal power dissipation while not sacrificing the performance. For instance, a multiple input NAND gate will require a longer window width than a NOR gate because of the larger internal capacitance due to the stacked nMOS transistors.

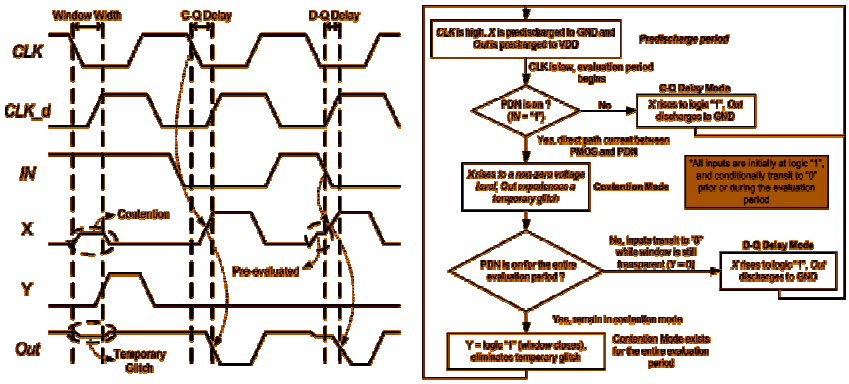

Figure 2 Timing diagram and flowchart of the proposed CD logic.

Drawbacks of CD logic are due to its bulky design and more power consumption compared to Domino logic. Each CD logic circuit consists of 11 more transistors than Domino logic and 13 more transistors than FTL. Due to those extra transistors area and power dissipation also slightly increases. In this paper two methods are proposed to overcome the drawbacks. They are Reducing the charging current with help of Leakage current replica circuit and Reducing the power consumption by minimizing the timing block.

II. EXISTING DESIGN FOR TIMING DIAGRAM

LEAKAGE CURRENT REPLICA TECHNIQUE**:** The leakage current replica (LCR) keeper (Fig. 3), which is a circuit that addresses the shortcomings of the conventional keeper and previously proposed enhancements [2]. The LCR keeper uses a conventional analog current mirror that tracks any process corner as well as voltage and temperature. The only variation that the LCR keeper cannot track is random on-die variation, which still must be addressed using conventional margining. A single current mirror structure can be shared among more than one dynamic gates. The LCR keeper overhead is one pFET per dynamic gate plus a portion of the shared current mirror circuit. There are other techniques circuit techniques which change the controlling circuit of the gate voltage of the keeper such as conditional-keeper domino (CKD), high speed domino (HSD), and controlled keeper by current-comparison domino (CKCCD) [3]. As LCR occupies less area among the above mentioned techniques it is chosen in this project.
Leakage current replica setup is shown in fig. 4. In this method a leakage current replica circuit is inserted between the power supply and transistor M13, which provides a constant current source. The current provided is the leakage current of the NMOS transistor M3. The leakage current changes from logic to logic. The w/l ratio of transistor M3 is set to the equivalent w/l ratio of the NMOS logic network. Transistor M1 and M2 mirrors the leakage current of M3.

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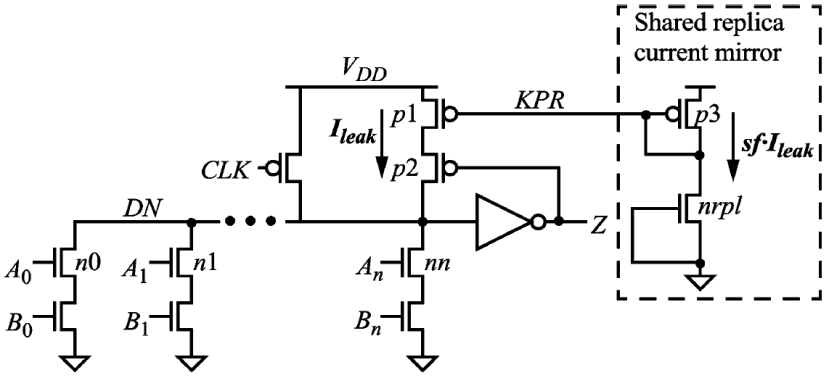

Figure 3 LCR keeper dynamic gate topology

In evaluation phase node 'X' is charged with the leakage current of M3. As the leakage current is less the power consumption in modified CD logic reduces, but there are two problems associated with Leakage current replica circuit addition.

First problem is it requires three more transistors than the original CD logic, which is an area overhead. Second one is, the leakage current may not be sufficient to charge the node 'X' to V_{DD} in the given window width. To solve this the window width should be increased or leakage current should be increased, even if the problem of charging is solved the delay problem arises, where the delay increases due to slow rising of voltage at node 'X' due to leakage(less) current.

So the usage of leakage current replica method increases the area overhead and increases the delay. This leakage current replica method is best suited for FTL which gives improved power performance compared to CD logic, but here also the delay is reduced.

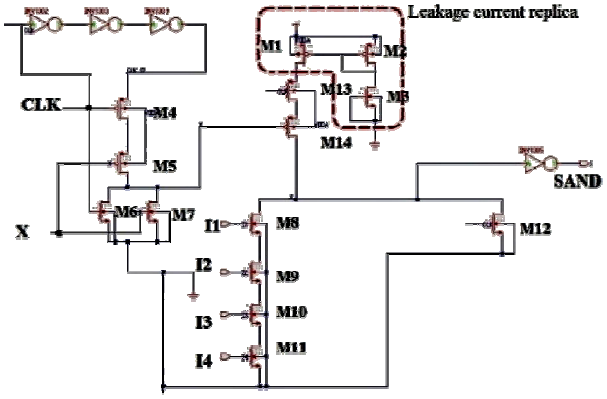

Figure 4 Leakage current replica method

TIMING BLOCK MINIMIZATION TECHNIQUE: In CD logic(fig 5.) the extra number of transistors is mainly due to timing block, so optimizing the timing block reduces the area overhead and power consumption. The timing block should be optimized in such a way that the delay should not be increased.

Three optimized designs of timing blocks were proposed in this paper which performs the same logical function of the original timing block.

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Table I. Truth table of timing block- II

CLK_D	SOUT	TOUT
0	0	0
0	1	1
1	0	0
1	1	0

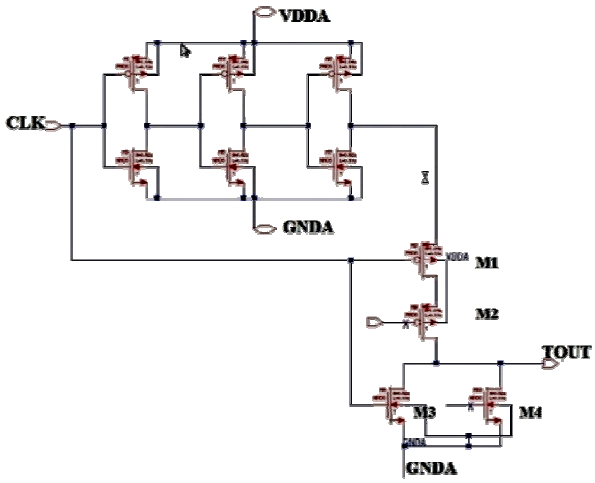

Figure 5 Timing Block of CD logic

8-T TIMING BLOCK: In first design the number of transistors in the timing block is reduced by two. Fig. 6 shows the original timing block from where the transistors M1 and M3 are removed to get the same operation performed. Fig. 4.4 shows the first modification in timing block i.e., 8-T timing block. The delay gets increased if this timing block is used because transistor M3 has clock as an input i.e., if CLK='1' then TOUT should be pulled to zero. As M3 is absent in this circuit TOUT is made zero through M2 using delay inverted clock signal. So TOUT is inverted version of clock, i.e., when CLK='1' TOUT='0', but with some delay. This delay makes the pre-charging slower, which increases the delay. To reduce the delay, the W/L ratio of pre-charge transistors should be increased. To avoid this 9-T timing block is developed.

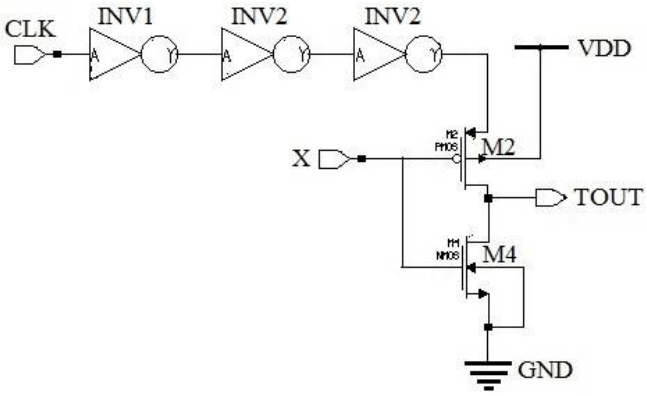

Figure 6 8-T timing block

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9-T TIMING BLOCK: In the second design one transistor is reduced as shown in fig. 7, but the 8-T timing block has some limitations for low leakage paths, and 9-T timing works well with the low leakage paths but dissipates more power at high leakage paths. The drawback in 8-T timing block is overcome by adding transistor M3. So now, charging the TOUT node is faster compared to that in 8-T timing block. But here the disadvantage is more power dissipation.

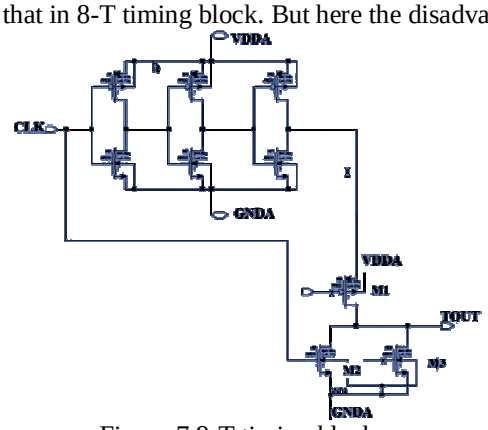

Figure 7 9-T timing block

III. PROPOSED TECHNIQUES TO IMPROVE CD-LOGIC

6-T TIMING BLOCK (PROPOSED TECHNIC):Fig. 8 Shows the 6-T timing block. Truth table of 6-T timing block is shown in table 1. 6-T timing block even though performs the same operation of original timing block and 8-T timing block its design is different from both above. First two timing blocks takes the node 'X' as feedback, but 6-T timing block takes the inverted output of 'X' i.e., 'SOUT' as the feedback.

The operation of 6-T timing block can be understood from the table 4.1, in evaluation mode when node 'X' is low 'SOUT' is high, the power supply should be cutoff so that TOUT is '1'. When 'SOUT' is low then power should be supplied to node 'X' so that the charge leakage can be eliminated, but taking 'SOUT' as a feedback leads to a drawback. In the CD logic with original timing block node 'X' can be connected to any static block, but in CD logic with 6-T timing block node 'X' should be connected to only an inverter. Static gates cannot be replaced with the inverter, because the truth table depends only on inverter output if a static gate replaces the inverter then the 6-T timing block cannot get the inverted feedback, then the truth table fails. As the timing block is reduced by four transistors adding two more transistors is not a big drawback, and that too the addition of two transistors is not required everywhere.

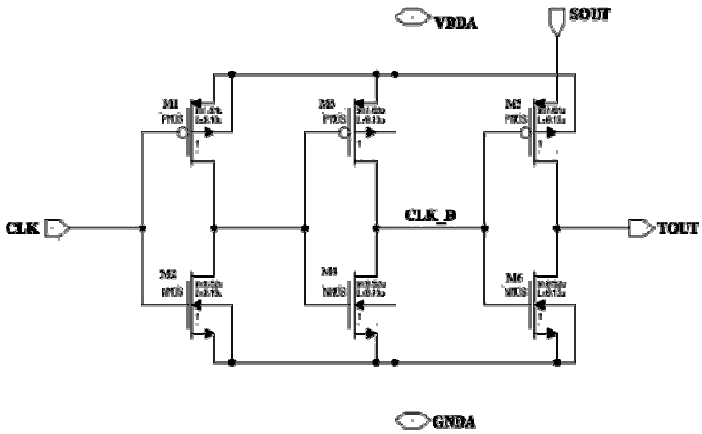

Figure 8 6-T timing block

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IV. RESULT AND DISCUSSION

The performance comparison between different types of designs is shown in table 2. Even though LCR addition reduces the charging current, due to the three more transistors the power dissipation increases. LCR addition for FTL decreases the power dissipation of FTL, but the decrement in power dissipation is negligible compared to the CD logic. CD logic is nothing but the addition of timing block and logic block to the FTL. Optimizing the timing block seems to be the best option to reduce the power dissipation without affecting the delay. Delay can be reduced by just slightly increasing the transistor widths of M3 and M4 without affecting the logic function. So the power dissipation, delay and area get reduced by replacing the 10-T timing block with modified 6-T timing block.

V.CONCLUSION

In this paper four different types of techniques are employed where, the leakage current replica failed in reducing the power dissipation, minimizing the area and reducing the delay, coming to 8-T timing block CD logic, it succeeded in minimizing the area and power dissipation but failed in reducing the delay. 9-T timing block CD logic has shown reduction in area but not more than that of the 8-T timing block CD logic, with same speed as that of the conventional logic. The drawback in 9-T timing block CD logic is that it dissipates more power than all the other proposed techniques. Finally the improved CD logic has overcome the drawbacks of CD logic by decreasing the logic area and Power dissipation with almost the same speed. This technique provided the least area, highest speed and lowest power dissipation among all the proposed techniques. By doing this Improved CD logic delivers better performance in speed, power consumption and area compared to CD logic.

TABLE II COMPARISON OF AND & OR GATES WITH DIFFERENT MODELS

Logic type	C-Q delay	D-Q delay	Power Dissipation
Constant delay logic 4-I/P AND gate	224.97 ps	221.81 ps	6.559 n Watts
Constant Delay logic 4- I/P OR gate	257.12 ps	226.16 ps	6.172 n Watts
LCR Constant delay 4-I/P AND gate	228.99 ps	223.50 ps	7.743 n Watts
LCR Constant delay 4-I/P OR gate	238.46 ps	214.42 ps	7.356 n Watts
8-T TB CD logic 4-I/P AND gate	321.98 ps	310.88 ps	4.567 n Watts
8-T TB CD logic 4-I/P OR gate	354.92 ps	324.34 ps	4.123 n Watts
9-T TB CD logic 4-I/P AND gate	245.77 ps	231.42 ps	7.658 n Watts
9-T TB CD logic 4-I/P OR gate	267.52 ps	235.21 ps	7.234 n Watts
6-T TB CD logic 4-I/P AND gate	145.21 ps	144.87 ps	2.791 n Watts
6-T TB CD logic 4-I/P OR gate	177.20 ps	134.24 ps	1.804 n Watts

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