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Design of ALU Based on Reversible Gates

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ABSTRACT: Programmable reversible logic is emerging as a prospective logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on circuit heat generation. Recent advances in reversible logic using and quantum computer algorithms allow for improved computer architecture and arithmetic logic unit designs. There are many reversible logic gates which can perform various logical and arithmetic operations. However, basic reversible logic gates have their own importance to perform various operations in different logic structures. In this paper a reversible ALU based on two basic reversible logic gates namely Fredkin & Feynman, is proposed. This reversible logic structure performs 12 operations with minimum number of garbage output and constant inputs. There are four control signals which are used to perform particular arithmetic and logical operations as well as to select suitable operation as an output.

KEYWORDS: Fredkin Gate, Feynman Gate, Quantum Cost, Reversible Adder

I. INTRODUCTION

According to the Landauer [1] if energy consumption in bit erase is considered, an n input and single output gate provides a loss of (n-1) information bit while going through the classical logic gate. For every bit of information loss, KT ln2 joules energy is dissipated where k is the Boltzmann constant and T is the absolute temperature. C.H. Bennett [2, 3] showed that dissipated energy is directly correlated with number of lost bits. AND gate can be considered as an example. It follows ordinary logic and can be said traditional or classical logic gate. Output of any AND gate comes to be logic 0 for three combinations of input bits. It appears logic 1 for only one combination of inputs. Thus it erases and overwrites 0 for three different combinations which is nothing but loss of energy. To resolve this problem, reversible logic gates can be used. It provides same number of input and output with unique input output combinations.

The key point of reversible computing is that the electric charge at output of any device should remain available for further calculations. It means charge on storage cell consisting of transistors is not permitted to flow away when the transistor is switched between on/off positions [4]. In this way output can be reused through reversible computation. When there is no information bit loss, system is reversible. To perform this type of computation, it is necessary to have some n × n logic devices which can substitute traditional or classical n × 1 logic devices.

II.LITERETURE SURVEY

Lihui Ni, Zhijin Guan, and Wenying Zhu described general approach to construct the Reversible full adder that can be extended to a variety of Reversible full adders with only two Reversible gates.Bruce, J.W et.al.used only Fredkin gates to construct full adder with gates cost equal to 4, 3 garbage outputs and 2 constant inputs. HimanshuThapliyal and A P. Vinod [6] presented design of reversible gates by using pass transistor logic and K. Prudhvi Raj and Y. Syamala [7] proposed reversible gates design using CMOS and pass transistor logic both.MathewMorrison &Nagrajan Rangnathan [14] showed a reversible ALU based on MRG gate, PAOG gate and UPG gate.One of the existing Design of ALU is shown in[15].This design is compared with traditional 4 –bit ALU specified as 74181ALU.Main logical operations are same therefore reversible ALU as described in (Zhijin Guan 2011) and 74181ALU are considered as logic devices which uses reversible and traditional logic gates to achieve same output.

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III. SOME REVERSIBLE LOGIC GATES

A reversible logic gate should follow property of bijection between input and output. It means number of inputs and number of outputs is equal and output can be uniquely generated for given input combinations. Similar to classical logic gate, reversible logic gate can be designed by using pass transistor as given in [6] or CMOS logic as given in [7]. Reversible logic gates used in proposed designs are Feynman [4] gate and Fredkin gate [8].

Feynman (F) / CNOT Gate:The Feynman gate as shown in Fig. 1 is also called CNOT gate, is the fundamental reversible logic gate as describe in [4] has mapping of input (X1, X0) to output (Y1, Y0) as shown in (2) and (3).

$$Y1 = X1 \quad (1)$$

$$Y0 = X0 \oplus X1 \quad (2)$$

According to quantum representation shown in Fig. 2, Quantum cost of Feynman gate is one and delay according to [5, 9] is 1Δ. It can also be used to generate fan out signals by keeping one input at ground according to Fig. 3.

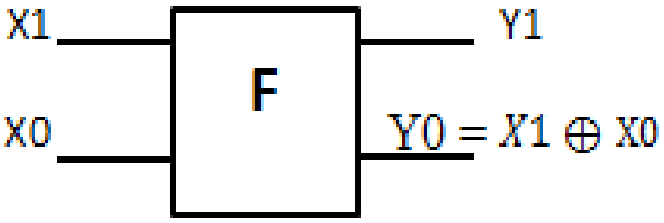

Fig.1. Feynman Gate

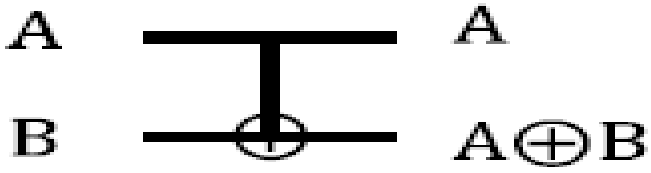

Fig.2. Quantum representation of Feynman Gate

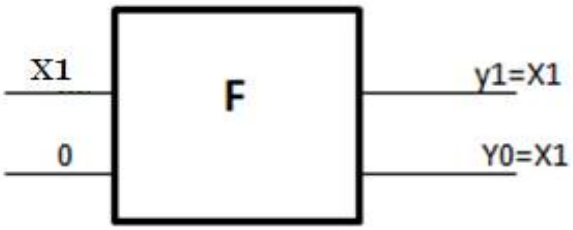

Fig.3. Fan-Out signal

FREDKIN GATE (FG): Fredkin gate as shown in Fig. 4 is a reversible 3×3 gate as proposed in [8]. Relation between inputs (X3, X2, X1) and outputs (Y3, Y2, Y1) of Fredkin gate is given by (3), (4) and (5).

$$Y3 = X3 \quad (3)$$

$$Y2 = \bar{X}3 \cdot X_2 + X3 \cdot X1 \quad (4)$$

$$Y1 = X3 \cdot X2 + \bar{X}3 \cdot X1 \quad (5)$$

Fredkin gate has the property to swap the inputs according to the value of control signal as given in (6) and (7). X_3 is control signal in this case.

$$Y_2 = X_2 \,\&\, Y_1 = X_1 \text{ when } X3 = 0 \quad (6)$$

$$Y_2 = X_1 \,\&\, Y_1 = X_2 \text{ when } X3 = 1 \quad (7)$$

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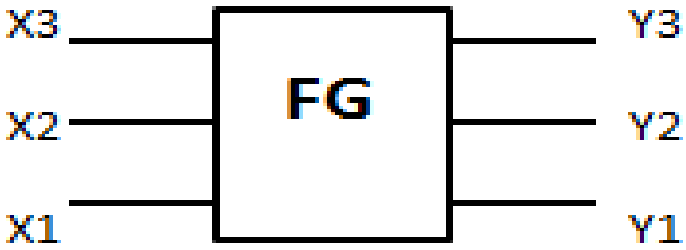

Fig.4. Fredkin Gate

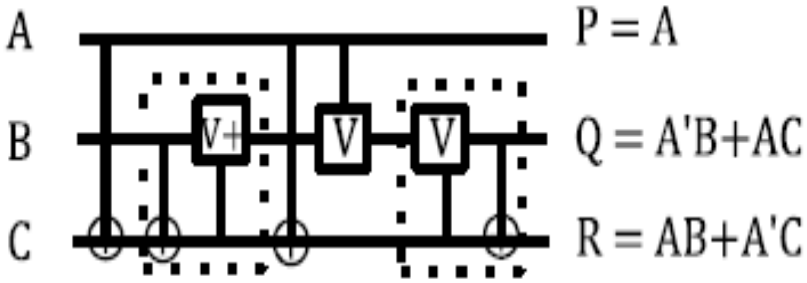

Fig.5. Quantum representation of Fredkin Gate

Quantum representation of FG is shown in Fig. 5. According to it, the quantum cost of FG is 5 and delay according to [5, 9] is 5Δ. This gate can also be used to create the inverse and fan out function as shown in Fig. 6. Two input AND gate can be generated by grounding one terminal as shown in Fig. 7. Two input OR gate can be generated by tying one terminal of FG to supply voltage as represented in Fig. 8. Higher order AND and OR logic can be realized by using FG arranged in binary tree. B bit AND gate requires B-1 FGs. In this type of structure input passes a maximum of $\log_2 N$ FGs [10].

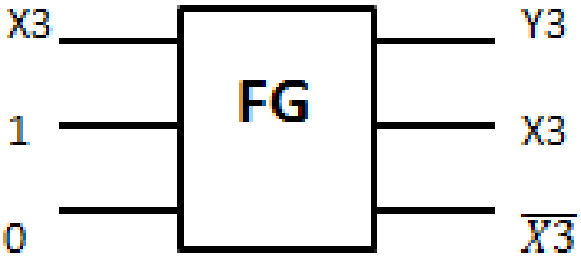

Fig.6. Fan-out signal

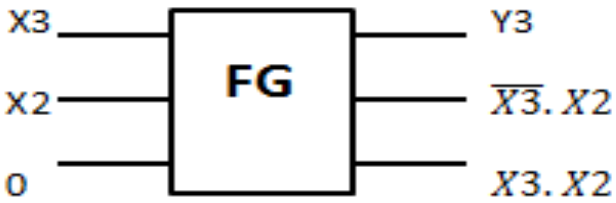

Fig.7. Logical 'AND ' operation

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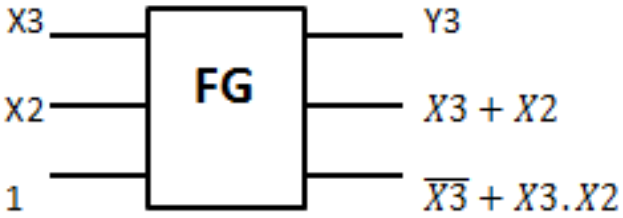

Fig.8. Logical 'OR' operation

IV. BASIC DEFINITIONS ABOUT REVERSIBLE LOGIC GATE

If matter of performance is discussed, reversible logic gates have some parameters namely quantum cost, constant input and garbage output. Also, delay in circuit and number of transistors used are important factors to consider while designing any reversible logic structure.

GARBAGE OUTPUTS:The number of outputs added to make an n-input-k-output function reversible is called garbage. Whenever it is necessary to make equal number of inputs and outputs, additional inputs or outputs can be added .Relation between the number of garbage outputs and constant inputs, can be given below in (8).

Input + constant input = output + garbage (8)

QUANTUM COST:The cost of the circuit in terms of the cost of a primitive gate is called Quantum cost. It is calculated knowing the number of primitive reversible logic gates (1×1 or 2×2) required to realize the circuit. Quantum cost of a 1×1 gate is 0 and 2×2 gate is 1.

DELAY:Delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. Definition is based on two assumptions first each gate performs computation in one unit time and second all inputs to the circuit are available before the computation begins. Logical depth can be considered as measure of the delay proposed by Mohammadi and Eshghi [5]. Each 1×1 gate and 2×2 reversible gates are taken as unit delay 1. Any 3×3 reversible gate can be designed from 1x1 reversible gates and 2×2 reversible gates, such as CNOT gate, Controlled-V and Controlled-V+ gates (V is a square-root-of NOT gate and V + is it's Hermitian). Thus, delay of a 3x3 reversible gate can be computed by calculating its logical depth when it is designed from smaller 1x1 and 2x2 reversible gates.

V. ARITHMETIC LOGIC UNIT (ALU) BASED ON REVERSIBLE LOGIC

ALU can perform various arithmatic and logic operation hence it can be considered as important part of any centre processing unit(CPU).Basicly an ALU should perfom Addition, subtraction as arithmatic operations and for logical operations, it should perform AND, OR, NOT, EXOR.Other operations can be derived on the basis of these operations.The ALU designs proposed in [10] can perform these baisc operations. It is designed in two part as revrsible function generartor and control unit.The proposed is also based on [10] and provides the idea of reversible function generator and a multiplexer to control the output for given control lines.

PROPOSED RVERSIBLE FUNCTION GENERATOR:The proposed reversible function generator consists of five Fredkin gates and seven Feynman gates in different ways to perform different functions such as fanout, decison making and other logical operations. In the structure shown in figure [9] there are three control signal AS_LI_D , A_S, AND_OR. Name of the lines can be given as S2,S1,S0 but the abreviated names are used to identify the operations.

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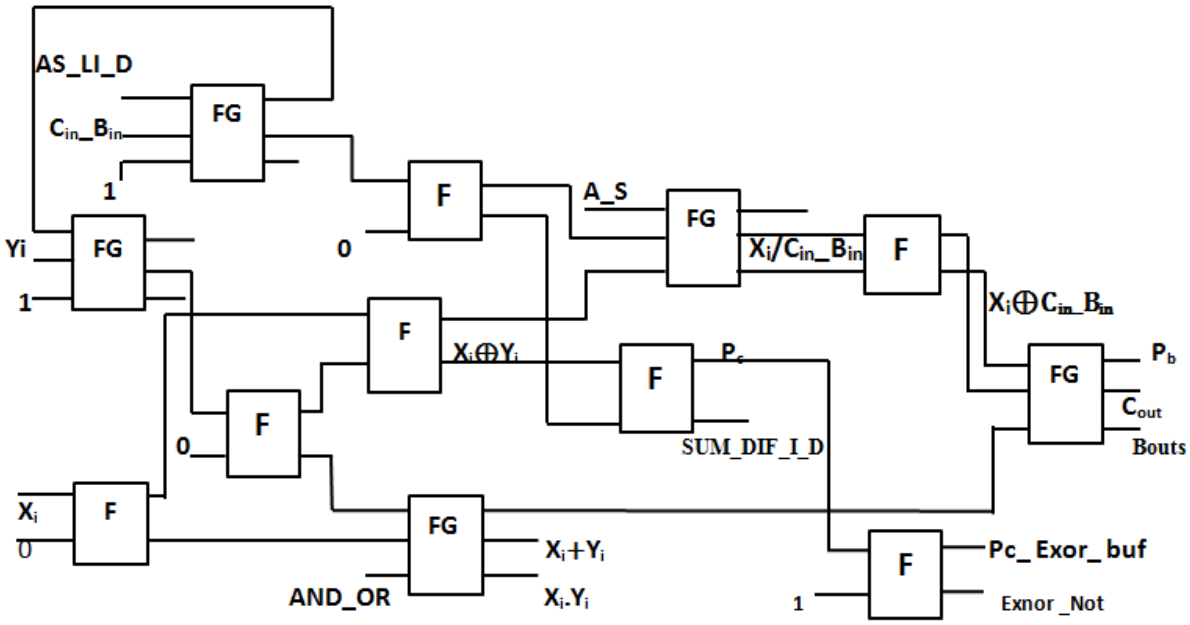

Fig.9. Proposed Reversible function Generator

such as AS_LI_D is used to identify selection between Arithmatic and logical opeartions of add, subtract, Increment and decrement, A_S is used to identify add and subtract operation under the control of AS_LI_D similiarly AND_OR is used to identify logical AND, Logical OR operations. These signals are further used in multiplexer to select any operation according to the code.

Table 1: Operation performed by reversible function generator

Sr. No.	AS_LI_D	A_S	AND_OR	Operation
1	0	0	0	A minus B, Borrow
2	0	0	1	A plus B , Carry
3	0	1	0	A.B, A⊕B,$\overline{A \oplus B}$, A⊕C,$\overline{A}B$
4	0	1	1	A+B, $\overline{B} + AB$
5	1	0	0	Decrement A
6	1	0	1	Increment A
7	1	1	0	A=A
8	1	1	1	$\bar{A}$

This function genretor has quantum cost of 32 with 6 constant input,4 gabage output and can perform 15 operations which are shown in Table 1.The delay in sum and difference signal generation is 1FG and three F , delay in carry and borrow signal propagation from input to output appears to be 3FG and 2F but since Carry in and borrow in signals are the control signal of two Feynman gates. Hence the worst case delay in carry and borrow propagation is 3FG and 1 F.
This function generator provides many outputs at same signal line. For example result of Add, Subtract, Decrement, increment appears on same signal line but for different control line status. Some signal such as logical AND, EXNOR, EXOR, $\overline{\boldsymbol{A}}\boldsymbol{B}$,$\overline{\boldsymbol{B}} + \boldsymbol{AB}$ appears simultaneously on different output lines. To resolve this problem a multiplexer based control unit is proposed.

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There exist a trade of between number of operations and number of gate used. So the quantum cost of this function generator can reduced to 20 and this structure will perform only 7 operations which will be comparable to [12]. In this case the worst case delay will reduced to 2FG and 1F.

PROPOSED CONTROL UNIT: The control unit based on reversible multiplexer consists of six Fredkin and one Feynman gate. It picks any one of the outputs from function generator according to the code received from control lines of function generator. It also generates carry &borrow signals for next stage. The quantum cost of this control unit is 31 with 9 garbage output and one constant input.

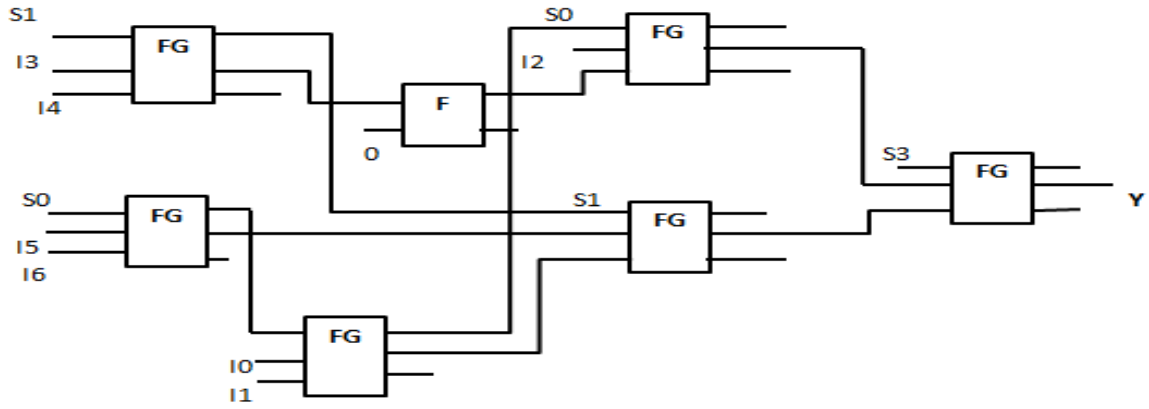

Fig.10. Proposed control unit

It has four control signal S3, S2, S1, S0 to select the desired output. Three signals S2, S1, S0 are received from function generator but one signal S3 is used for selection between arithmetic and logic operations.

PROPOSED N- BIT REVERSIBLE ALU: The proposed function generator and control unit can be combined to work as one bit ALU. This one bit ALU block can be combined with same type of blocks to perform ALU operations for more than one bit. Along with this there exist two advantages one Fredkin gate can be removed from each next stage of proposed function generator as only first stage needs it for increment and decrement operations. One Feynman gate can also be removed from very last stage of control unit as there is no need to add carry and borrow for further stage. Hence total quantum cost of n bit ALU with proposed design is

$$QC = 32n-5(n-1) + 31n -1 \quad (9)$$

$$QC = 32n-5n-5+31n-1 \quad (10)$$

$$QC = 58n-6 \quad (11)$$

The proposed function generator performs 15 operations but significant arithmetic and logical operations are accessed by control unit. This strategy reduces the size of control unit and avoids unnecessary outputs. Now total 12 useful operations are accessed as shown in Table 2.

Table 2 Proposed reversible ALU operations

Sr. No.	**S3**	**S2**	**S1**	**S0**	**Operation**
1	0	0	0	0	Subtract
2	0	0	0	1	Borrow Out
3	0	0	1	0	Add
4	0	0	1	1	Carry out
5	0	1	0	0	Decrement
6	0	1	1	0	Increment
7	1	0	0	0	AND
8	1	0	0	1	OR

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9	1	0	1	0	EXOR
10	1	1	1	1	NOT
11	1	0	1	0	Buffer
12	1	1	1	0	EXNOR

V. RESULT AND DISCUSSION

In order to verify the functional correctness of proposed ALU, Verilog code for four bit reversible ALU is written and design is simulated on Modelsim. Each output waveform corresponds to one or more operations performed by the Proposed ALU. Type of operation can be identified using four control signals namely S3, S2, S1, S0 according to table 2.Output is denoted by the signal Y and three input signals are Xi, Yi, Cin_Bin.

1. According to table 2 output of subtract operation can be obtained for a given code of S3, S1, S2, S0. Four bit numbers denoted by Xi and Yi (Fig.11) and subtracted output is denoted by Y.

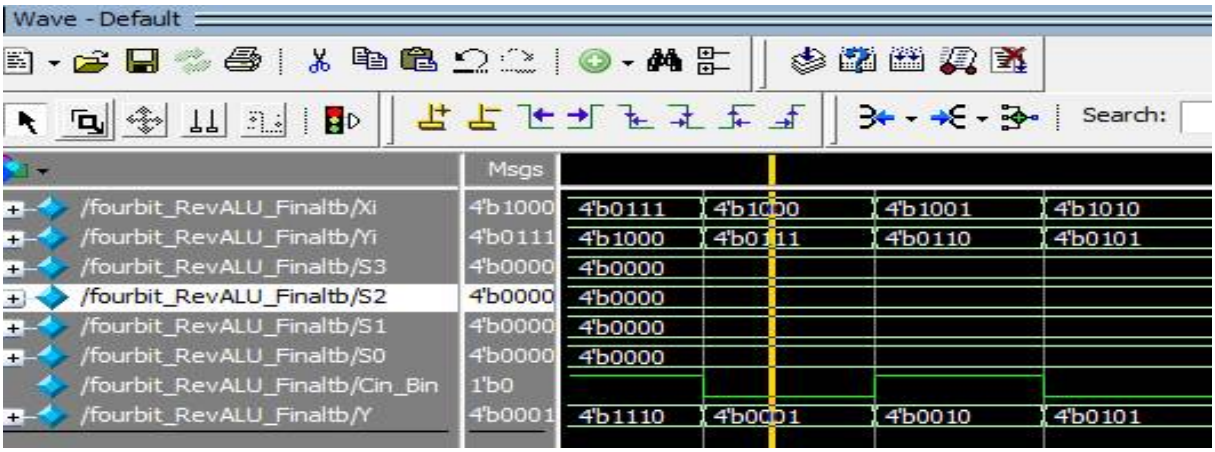

Fig.11. Output Waveform of four bit ALU (Subtract operation)

2. Fig. 12 shows two binary numbers denoted by Xi and Yi and output of add operation is denoted by Y. This figure contains four combinations of each four bit binary numbers along with addition operation associated with them.

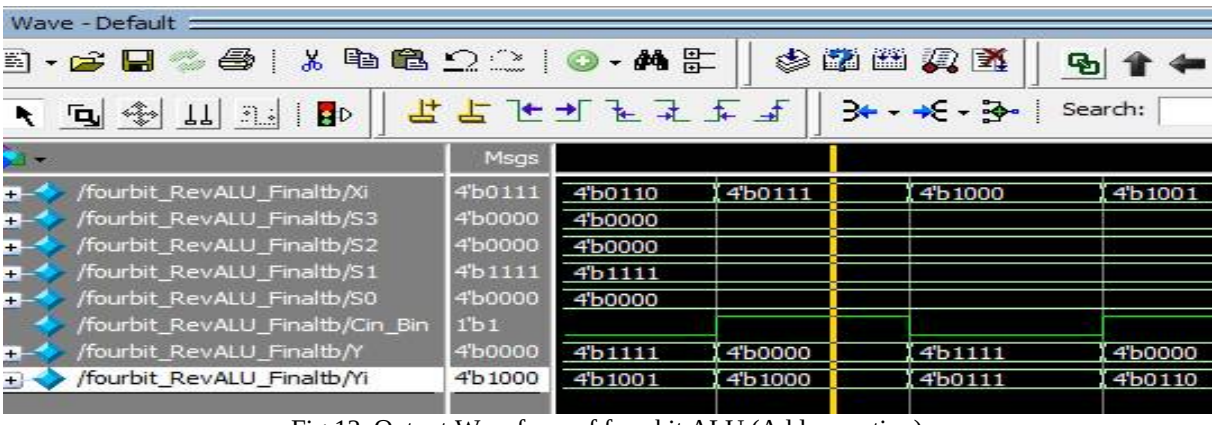

Fig.12. Output Waveform of four bit ALU (Add operation)

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3. Increment operation is shown by adding 1 to least significant bit of a given number. For easy observation Fig. 13 shows numbers in hexadecimal form along with output Y after incrementing the hexadecimal digit Xi.

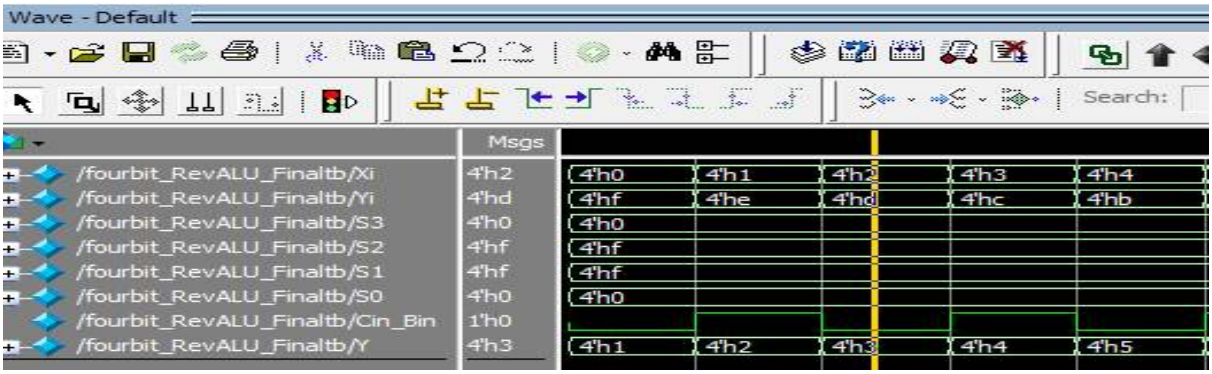

Fig.13. Output Waveform of four bit ALU (Increment operation)

4. Decrement operation is shown by subtracting 1 from least significant bit of a given number. For easy observation Fig. 14 shows numbers in hexadecimal form along with output Y after decrementing the hexadecimal digit Xi.
5.

Fig.14. Output Waveform of four bit ALU (Decrement operation)

6. This figure (Fig.15) contains two operations performed between Xi and Yi for two different values of S3, S2, S1, and S0.

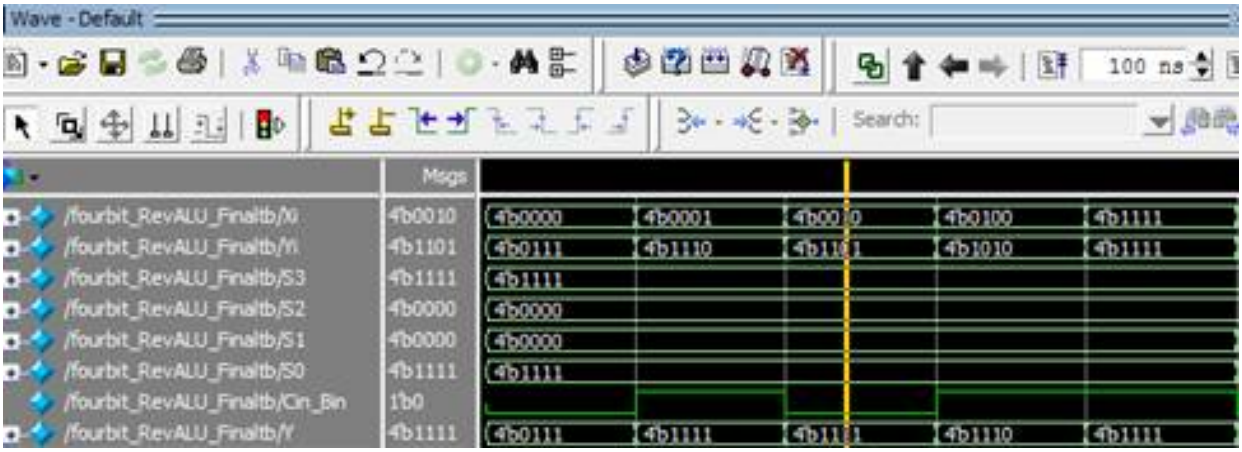

Fig.15. Output Waveform of four bit ALU (OR, EXOR operations)

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7. This figure (Fig.16) contains AND operation performed between Xi and Yi and NOT operation performed on Xi only. These operations are performed between each binary bit of both numbers it means each 1 bit ALU block performing the operation individually.

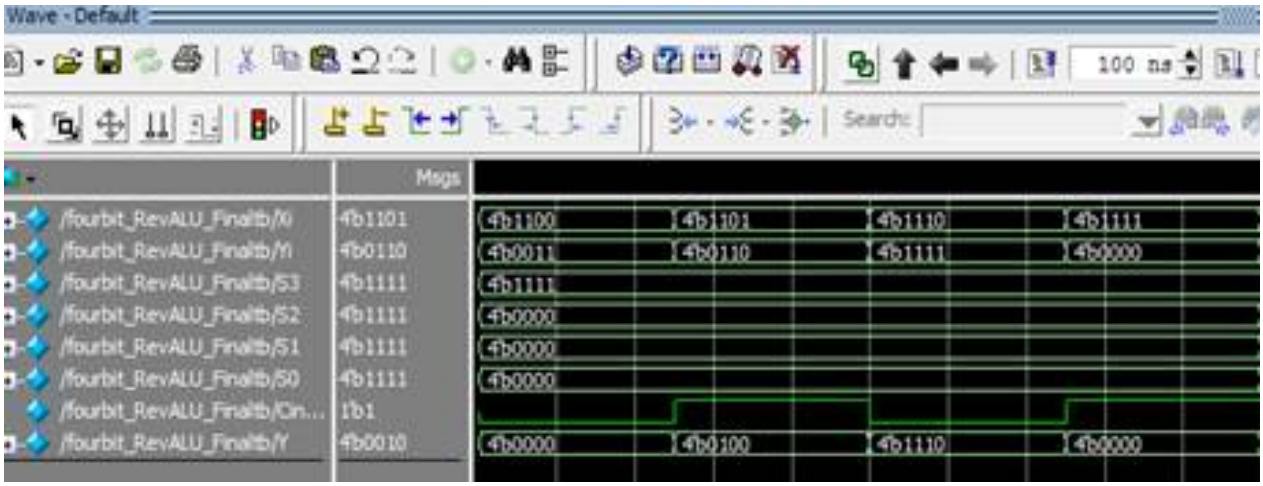

Fig.16. Output Waveform of four bit ALU (AND, NOT operations)

8. This figure (Fig.17) contains XNOR operation performed between Xi and Yi and buffer operation performed on Xi only. Binary numbers are shown to observe this operation between each bit of some possible combinations of the numbers.

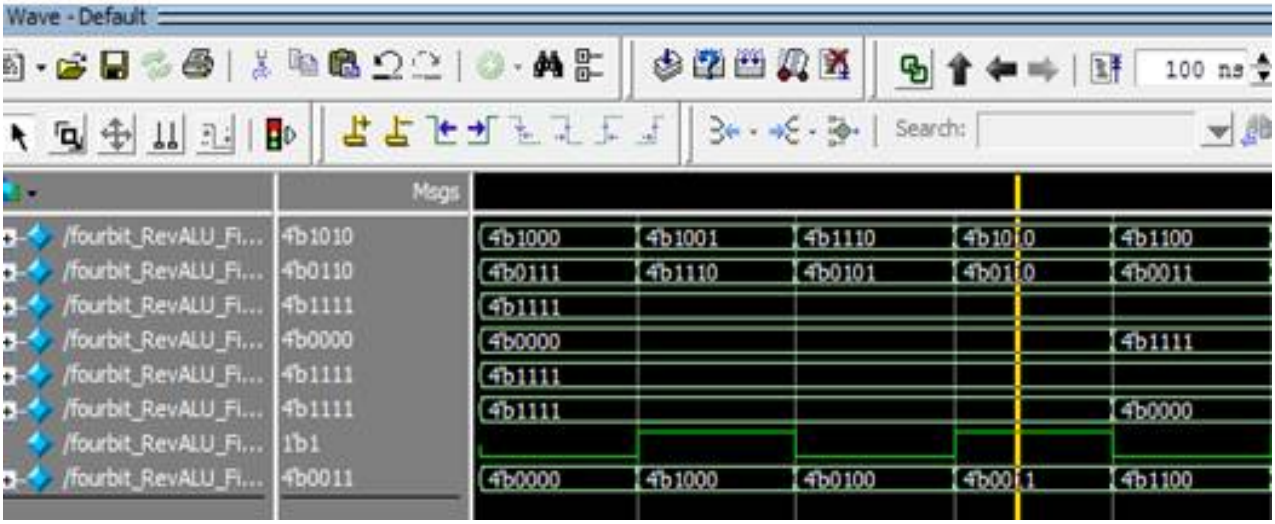

Fig.17. Output Waveform of four bit ALU (Buffer, XNOR operations)

VI. CONCLUSION

The proposed reversible logic unit has some advantages over previous design [15] as it consist of two type of basic reversible logic gates Feynman and Fredkin so less number of transistors are required as according to [6,7] minimum transistor required to design Feynman gate are eight and for Fredkin gates are six. This ALU performs more arithmetic and logic functions such as XNOR, Buffer, NOT. In case of quantum cost and delay it is not better than the design in [14] but if number of functions is considered this design performs twice the number of functions as well as proposed ALU has four control lines to generate opcode for various operations which are lesser in comparison to [14]. In

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comparison with ALU [15] as shown in table3, the proposed design is better in case of quantum cost and as far as delay is considered it provides delay of 5 FG in carry signal generation and 3FG and 2 F delays in sum or difference generation which is comparable with ALU [15].
One more advantage of proposed design is that it uses carry skip adder [11] and borrow skip Subtractor which can predict Carry out and Borrow out signal before it ripples in each adder Subtractor stage. This facility makes this design faster.

Table 3 Comparison of proposed ALU with existing design

Design	Quantum cost	Delay(worst)	Garbage output	Constant input
proposed	58n-6	27n	10n	7n
[15]	>60n	>30n	12n+1	8n

This reversible logic structure is a logic device which can perform as reversible ALU. By using reversible logic gates instead of traditional logic gates (AND, OR gates) agenda of power consumption can be taken into consideration. The flexibility of design is provided as basic reversible logic gates are used so enhancement of device for higher bit is possible. To improve delay facility of carry skip block [12] and borrow skip block design can be included. There are four control bits and only 12 operations are given. More operations corresponding to remaining combination of control bits can be included.

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