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# Design of Cascaded Asymmetric Multilevel Inverter 

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#### Abstract

Electricity can be generated using non conventional energy sources. Solar energy is one of the important non conventional energy. By using solar energy PV arrays produce electricity. The output obtained from PV arrays is given to DC to DC converter, which is used to step up the DC voltage. The output obtained from DC to DC converter is given to an inverter for AC applications. The problems with conventional inverter are the output produced will be non sinusoidal, total harmonic distortion (THD) will be high, and it require more number of switches. To overcome the issues of conventional inverters multilevel inverters (MLI) are used. The inverter proposed is cascaded multilevel inverter (CMLI). Cascaded multilevel inverter uses less number of switches for AC applications using solar energy. 101 output levels are obtained from the proposed 15 switches multilevel inverter. Symmetric multilevel inverter disadvantages can be overcome by using asymmetric multilevel inverter. The number of voltage sources used for symmetric multilevel inverter is more compared to asymmetric multilevel inverter to obtain same number of levels. The proposed cascaded MLI gives low voltage stress and THD is reduced. The proposed asymmetric multilevel inverter circuit produces THD of $3.78 \%$. Modeling and simulation of proposed topology is done using MATLAB/SIMULINK.


KEYWORDS: Non Conventional Energy, Multilevel Inverter, Total Harmonic Distortion, Cascaded Asymmetric.

## I. INTRODUCTION

Energy crisis is the major problem faced by all nations of the world. Energy crisis occurs when fossil fuels get depleted. Energy crisis can be overcome by using renewable energy sources. The combustion of fossil fuels produces environmental pollution. Renewable energy can be harvested by using different methods. The important renewable energy is solar energy. The important natural energy obtained from the sun is solar energy and it is widely available in nature.
The block diagram for the proposed topology is shown in figure 1.Solar energy is heat and light energy obtained from sun. Solar energy is trapped into PV Arrays. Solar energy is converted into electrical energy with help of PV arrays. PV Arrays produces output which is DC in nature. DC to DC converter is connected to the output of PV arrays. An electronic circuit which converts a source of direct current (DC) from one voltage level to another is called DC to DC converter. Now an inverter is connected to the DC to DC converter. Inverter converts DC into AC. The output obtained from inverter is AC. Cascaded asymmetric multilevel inverter is used for the proposed work. [1] The first inverter which was invented was 2 level inverters. Multilevel inverters were developed as technology got advanced and in recent times they have gained lot of interest in many applications. Diode clamped MLI, flying capacitor MLI and cascaded MLI are different classes of multilevel inverter. [2] By using MLI near sinusoidal output waveform and reduced THD can be obtained. The THD can be decreased when the number of output levels is increased. The main disadvantage of conventional MLI is to obtain more number of output levels the number of components used to design the circuit increases. Cascaded H-bridge and diode clamped are two most advanced type of MLI topologies for which hardware implementation is possible. [3] Asymmetric MLI is used to overcome the limitations of symmetric MLI. The proposed topology is cascaded asymmetric MLI which utilize minimum number of switches and obtain reduced total harmonic distortion (THD).

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering 

(An ISO 3297: 2007 Certified Organization)
Vol. 5, I ssue 12, December 2016


Figure 1: Block diagram of the proposed topology

## II. BASIC CELL OF MLI

The basic cell of MLI topology generates same number of output levels compared to conventional multilevel inverter with reduced number of switches. 5 output levels are obtained from basic cell. [4] The basic cell consists of 2 voltage sources and 5 switches with anti-parallel diodes. DC voltage is the voltage obtained from the PV arrays. Figure 2 shows the basic cell of MLI topology. Basic cell consists of 5 switches S11, S12, S13, S14 and S15. The switches S11, S12, S13, S14 are arranged same as conventional H-bridge and S15 is added to increase the output level by selecting a proper voltage source. The two voltage sources are V11 and V12. The maximum output voltage obtained is 48 V . V11 $=\mathrm{V} 12=24 \mathrm{~V}$


Figure 2: Basic Cell of MLI
The table 1 represents the switching states of five level basic cell of Multilevel Inverter (MLI) topology. Where logic ' 1 ' is used to represents 'ON' state and logic ' 0 ' is used to represent 'OFF' state of switch. Depending on the switching states of switches the output voltage is obtained. There are total 5 levels in which 2 are positive level, 2 are negative level and a zero level. In level1 the output voltage obtained is 0 V , the output voltage obtained in level 2 is 24 V , the output voltage obtained in level 3 is 48 V , the output voltage obtained in level 4 is -24 V and in level 5 the output voltage obtained is -48 V . There are two positive voltages 24 V and 48 V and two negative voltages -24 V and -48 V .

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering 

(An ISO 3297: 2007 Certified Organization)

Vol. 5, I ssue 12, December 2016

Table 1: Switching States of Basic Cell

| levels | S11 | S12 | S13 | S14 | S15 <br> output <br> v |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
|  | 1 | 0 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 | 1 | 24 |
| 3 | 1 | 1 | 0 | 0 | 0 | 48 |
| 4 | 0 | 0 | 1 | 0 | 1 | -24 |
| 5 | 0 | 0 | 1 | 1 | 0 | -48 |

Level 1: zero level, output voltage is 0 V .
Level 2, Level 3: Positive level, the output voltage obtained is 24 V and 48 V respectively.
Level 4, Level 5: negative level, the output voltage obtained is -24 V and -48 V respectively.

## III. MULTILEVE INVERTER WITH 10 SWITCHES

Multilevel inverter consists of two basic cells for 10 switches. [5] Figure 3 represents multilevel inverter with 10 switches. The total number of voltage sources used for 10 switches is four. S11, S12, S13, S14, S15, S21, S22, S23, S24 and S25 are different switches used. Switches S11, S12, S13, S14 and S15 are present in $1^{\text {st }}$ basic cell. The switches S21, S22, S23, S24 and S25 are present in the $2^{\text {nd }}$ basic cell. The voltage sources are V11, V12, V21 and V22. V11 and V12 are connected to $1^{\text {st }}$ basic cell and V21 and V22 are connected to $2^{\text {nd }}$ basic cell. By using 10 switches multilevel inverter total 25 levels can be obtained.
In which 12 are positive level, 12 are negative and a zero level is obtained. The output obtained is in stepped form with increase in voltage of 24 V for each level. 288 V is the maximum output voltage obtained. The input voltage given is DC in nature and the output obtained is AC. Two different voltages are used in the structure. The voltage sources used are $\mathrm{V} 11=\mathrm{V} 12=120 \mathrm{~V}$ and $\mathrm{V} 21=\mathrm{V} 22=24 \mathrm{~V}$.


Figure 3: Multilevel inverter with 10 switches

## IV. OPERATION OF 10 SWITCHES MLI

The 10 switches MLI switching states is illustrated in the below table. There are 25 levels in which 12 are positive levels, a zero level and 12 are negative levels is obtained. The output obtained from the inverter is in stepped form with increase in voltage of 24 V for each level. The maximum output voltage obtained is 288 V .

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering 

(An ISO 3297: 2007 Certified Organization)

## Vol. 5, I ssue 12, December 2016

The output voltage increase in steps from minimum of 0 V to maximum of 288 V , then it decreases in steps of 24 V and reaches 0 V . After the completion of positive levels the negative level starts. During negative level the voltage decreases in steps of -24 V and after reaching -244 V the voltage increases and reaches 0 V .

Table 2: Switching Operation of 10 Switches Multilevel Inverter

| levels | S11 | S12 | S13 | S14 | S15 | S21 | S22 | S23 | S24 | S25 | $0 / \mathrm{pV}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 2 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 24 |
| 3 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 48 |
| 4 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 72 |
| 5 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 96 |
| 6 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 120 |
| 7 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 144 |
| 8 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 168 |
| 9 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 192 |
| 10 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 216 |
| 11 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 240 |
| 12 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 264 |
| 13 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 288 |
| 14 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | -24 |
| 15 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | -48 |
| 16 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | -72 |
| 17 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | -96 |
| 18 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | -120 |
| 19 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | -144 |
| 20 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | -168 |
| 21 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | -192 |
| 22 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | -216 |
| 23 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | -240 |
| 24 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | -264 |
| 25 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | -288 |

## V. PROPOSED MULTILEVEL INVERTER WITH 15 SWITCHES

Three basic cells are present in the proposed multilevel inverter structure. Figure 4 represents proposed 15 switches multilevel inverter. Each basic cell consists of 5 switches hence a total of 15 switches are present in the structure. S11, S12, S13, S14, S15, S21, S22, S23, S24, S25, S31, S32, S33, S34 and S35 are different switches which are used in the proposed structure. The switches S11, S12, S13, S14 and S15 are present in $1^{\text {st }}$ basic cell. The switches S21, S22, S23, S24 and S25 are present in $2^{\text {nd }}$ basic cell. The switches S31, S32, S33, S34 and S35 are present in $3^{\text {rd }}$ basic cell. Total of six voltage source is connected, in which 2 voltage sources is connected in each basic cell.

The voltage sources connected are V11, V12, V21, V22, V31 and V32. The voltage in $1^{\text {st }}$ basic cell is V11 $=$ V12 $=$ 120 V . The voltage in $2^{\text {nd }}$ basic cell is $\mathrm{V} 21=\mathrm{V} 22=24 \mathrm{~V}$. The voltage in $3^{\text {rd }}$ basic cell is $\mathrm{V} 31=\mathrm{V} 32=6 \mathrm{~V}$. The input voltage given to the inverter is DC and the output voltage obtained is stepped AC. Three different voltage sources are used in the structure. By using 10 switches multilevel inverter total of 101 levels can be obtained in which 50 positive levels, a zero levels and 50 negative levels are obtained. 300 V is the maximum output voltage obtained at the output.

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering 

(An ISO 3297: 2007 Certified Organization)
Vol. 5, I ssue 12, December 2016


Figure 4: Proposed 15 switches multilevel inverter

## VI. OPERATION OF PROPOSED 15 SWITCHES MULTILEVEL INVERTER

The operation of proposed 15 switches multilevel inverter is shown in the switching states of the 15 switches multilevel inverter. The tables 3 and 4 represents positive levels of proposed 15 switches multilevel inverter and negative levels of proposed 15 switches multilevel inverter respectively. There are 101 levels in which 50 are positive levels, a zero level and 50 are negative levels is obtained. The output obtained is in stepped form with increase in voltage of 6 V for each level. The maximum output voltage obtained is 300 V . The output voltage increase in steps from minimum of 0 V to maximum of 300 V , then it decreases in steps of 6 V and reaches 0 V . After the completion of positive levels the negative level starts. During negative level the voltage decreases in steps of -6 V and after reaching 300 V the voltage increases and reaches 0 V .

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Table 3: Positive Levels of Proposed 15 Switches Multilevel Inverter


Table 4: Negative Levels of Proposed 15 Switches Multilevel Inverter


# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering 

(An ISO 3297: 2007 Certified Organization)
Vol. 5, I ssue 12, December 2016

## VII. SIMULATION RESULTS

The simulation for proposed basic cell of MLI topology is done using 5 switches. The SIMULINK model for basic cell is shown below. Harmonic spectrum analysis is done using FFT window for MATLAB/ SIMULINK. The parameters values used for the project work are voltage $\mathrm{V} 11=\mathrm{V} 12=12 \mathrm{~V}$, frequency $=50 \mathrm{~Hz}, \mathrm{R}=280 \Omega, \mathrm{~L}=35 \mathrm{mH}$.


Figure 5: SIMULINK Model of Basic Cell


Figure 6: Output Waveforms of Basic Cell MLI for RL Load


Figure 7: Switching States of Basic Cell of MLI

## International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

## Vol. 5, I ssue 12, December 2016



Figure 8: FFT Analysis of Basic Cell of MLI
Figure 5 represents the SIMULINK model of basic cell of multilevel inverter with 5 switches. Output waveforms of basic cell MLI for RL load, Switching States of basic cell of MLI, FFT Analysis of basic cell of MLI using 5 switches are shown in Figure 6, Figure 7, Figure 8 respectively. THD of basic cell of MLI with 5 switches is $5.57 \%$.

The simulation for 10 switches MLI topology results in 25 levels. In which 12 are positive, 12 are negative and zero level is obtained. The SIMULINK model for 10 switches MLI is shown blow. In MATLAB/ SIMULINK harmonic spectrum analysis is done using FFT window. The parameters used are voltage sources V11 $=\mathrm{V} 12=120 \mathrm{~V}, \mathrm{~V} 21=\mathrm{V} 22$ $=24 \mathrm{~V}, \mathrm{R}=280 \Omega, \mathrm{~L}=35 \mathrm{mH}$ and frequency $=50 \mathrm{~Hz}$.


Figure 9: SIMULINK Model for 25 Levels

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering 

(An ISO 3297: 2007 Certified Organization)
Vol. 5, I ssue 12, December 2016


Figure 10: Output Waveforms of 25 Level MLI Using 10 Switches for RL Load


Figure 11: Switching States of 25 Level MLI


Figure 12: FFT Analysis of 25 Level Inverter Using 10 Switches

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering 

(An ISO 3297: 2007 Certified Organization)

## Vol. 5, I ssue 12, December 2016

Figure 9 represents the SIMULINK Model for 25 levels topology. Output waveforms of 25 levels for 10 switches for RL load, Switching States of 25 levels MLI, FFT Analysis of 25 level 10 switches are shown in Figure 10, Figure 11, Figure 12 respectively. The THD of 25 level inverter using 10 switches is $4.71 \%$.

The proposed topology simulation is carried out using 15 switches. The number of output levels obtained is 101, in which 50 are positive, 50 are negative and a zero level is obtained. In MATLAB/ SIMULINK harmonic spectrum analysis is done using FFT window. The components used for proposed 15 switches MLI are voltage sources used are $\mathrm{V} 11=\mathrm{V} 12=120 \mathrm{~V}, \mathrm{~V} 21=\mathrm{V} 22=24 \mathrm{~V}, \mathrm{~V} 31=\mathrm{V} 32=6 \mathrm{~V}, \mathrm{R}=280 \Omega, \mathrm{~L}=35 \mathrm{mH}$ and frequency $=50 \mathrm{~Hz}$.


Figure 13: SIMULINK Model of Proposed MLI Using 15 Switches Topology


Figure 14: Output Waveforms of MLI Using 15 Switches for RL load

## International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

## (An ISO 3297: 2007 Certified Organization)

## Vol. 5, I ssue 12, December 2016



Figure 15: Switching States of MLI Using 15 Switches


Figure 16: FFT Analysis of MLI Using 15 Switches
Figure 13 represents the SIMULINK model of proposed 15 switches MLI, Output waveforms of MLI using 15 switches for RL load, Switching States of MLI using 15 switches, FFT Analysis of MLI using 15 switches are shown in Figure 14, Figure 15, Figure 16 respectively. THD of the proposed 15 switches is $3.73 \%$.

Comparison of THD of basic cell, MLI with 10 switches and MLI with 15 switches is shown in the below table
Table 5: Comparison of THD

| Switches | 5 | 10 | 15 |
| :---: | :---: | :---: | :---: |
| Levels | 5 | 25 | 101 |
| THD \% | 5.57 | 4.71 | 3.73 |

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering 

(An ISO 3297: 2007 Certified Organization)

Vol. 5, I ssue 12, December 2016

When basic cell of MLI is used, which produces total of 5 levels the THD obtained is $5.57 \% .10$ switches MLI is designed a total of 25 levels is obtained and the THD is $4.71 \%$. When 15 switches MLI is designed a total of 101 levels are obtained and the THD is reduced to $3.73 \%$. The above table concludes that when the number of output levels is increased THD is getting reduced. Further the output levels can be increased to reduce THD.

## VIII. CONCLUSION

The main objective of project work is to implement cascaded multilevel inverter for 5 switches, 10 switches and 15 switches to obtain different levels. The dissertation of the work has successfully designed cascaded multilevel inverter structure for solar applications. The design and development is carried out by using MATLAB and SIMULINK. MATLAB is used to write the codes for the structure. Synthesis and analysis is done using SIMULINK. The THD for 3 different levels are obtained such as 5 levels, 25 levels and 100 levels. The THD are tabulated and compared. The output which is obtained from the proposed method has low total harmonic distortion (THD) and the output quality is improved.

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