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Analysis, Design and Implementation of Snubberless Bidirectional Current Fed Full Bridge Voltage Doubler

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ABSTRACT: this paper describes the novel soft switching bidirectional snubberless current fed full bridge voltage doubler. A novel secondary modulation technique is used to clamp the voltage across the primary side switches naturally with zero current commutation (ZCC). It eliminates the necessity for active clamping or passive snubber to absorb the switch turn off voltage. A major challenge in current fed converters, zero current switching (ZCS) of primary side devices and zero voltage switching (ZVS) of secondary side devices are achieved, which significantly reduce switching losses. Primary device voltage is clamped at low voltage, which enables the use of low voltage devices with low on state resistance. Soft switching and voltage clamping is inherent and load independent.

KEYWORDS: snubberless, Bidirectional, zero current commutation (ZCC), zero current switching (ZCS), zero voltage switching (ZVS).

I.INTRODUCTION

Bidirectional dc/dc converter isolated with high frequency transformer has been widely used in motor drives in electrical vehicles (EVs), energy storage systems (ESS), dc/dc converting stage of solid state transformers (SSTs), and hybrid renewable energy generation with ESS due to its merits of low cost and high power density[1-5]. The proposed design DC-DC converter has the following features: number of active devices are low compared to the converters usually applied to reduce switching losses, DC-DC converter is essential equipment in the system of dc load which has step up and step down voltage. A DC-DC converter is required electrical couple to the dc load.
In the full bridge DC-AC-DC converter which allows energy transfer between the source and the load. The performance of the converter will be analyzed by comparing various modulation techniques like phase shift, triangular and trapezoidal methods. A high frequency transformer is used for isolation in DC-DC full bridge voltage doubler. Various modulation strategies have been discussed for the dual active bridge DC-DC converter [6]. The performance parameters have been analyzed in terms of output voltage ripple and switching losses. Simulation studies have been carried out using MATLAB & SIMULINK to verify the results.

Compared to voltage fed converters, current fed converters have lower input current ripple, lower HF transformer turns ratio, negligible diode ringing [8], and easier current control ability. Therefore current fed converters are meritorious for low voltage and high current application. The major limitations of current fed converters are hard switching and snubber requirements to absorb the switch turn off voltage spike.
A dual half bridge bidirectional DC-DC converter is proposed to minimize the number of switching devices. This converter topology requires four split capacitors to handle full load current and occupy a considerable volume of the converter. It may need an additional control to avoid the possibility of voltage imbalance across the capacitors. Also this topology is not modular in nature and so not easily scalable for higher power. Peak current through the primary switches are >2x the input current and top and bottom switches share unequal currents. In this paper, a novel secondary modulation based soft switching bidirectional snubberless current fed full bridge voltage doubler is proposed as shown in Fig.2. Voltage doubler or half bridge is selected to reduce number of switches.

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II.BLOCK DIAGRAM AND DESCRIPTION

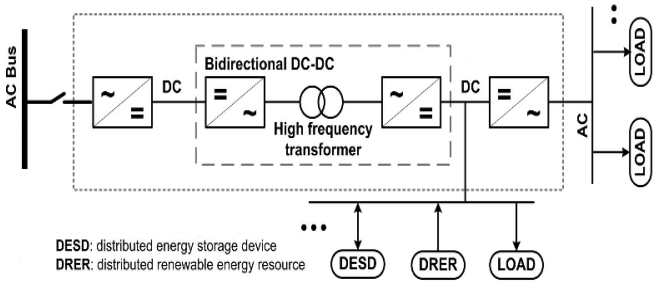

Fig.1 Block diagram

In this paper, a secondary modulation based soft switching bidirectional snubberless current fed full bridge voltage doubler is proposed as shown in Fig.2

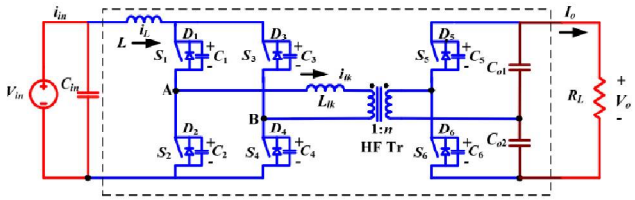

Fig.2 snubberless bidirectional full bridge voltage doubler

Voltage doubler or half bridge is selected to reduce number of switches; the transformer turns ratio. The proposed converter offers the following merits:

1) Switching losses are reduced due to ZCS of primary switches and ZVS of secondary switches. It permits high switching frequency operation to realize a compact and high power density system.

2) Voltage across primary devices is independent of duty cycle with varying input voltage and output power and naturally clamped. It avoids the need of passive snubber or active clamping circuit making it snubberless and enables the use of semiconductor devices of low voltage rating having low on state resistance. Therefore the conduction loss is significantly reduced and high frequency can be achieved.

III.SWITCHING OPERATION

In this section, steady state operation and analysis with zero current commutation (ZCC) natural voltage clamping (NVC) concept has been explained. Before turning off of a diagonal switch pair (S_1-S_4 or S_2-S_3) at primary side, the other pair of primary side switches turned on. The reflected output voltage $V_0/2n$ appears across the transformer primary. It diverts the current from one switch pair to other pair through transformer causing current through just triggered switch pair to raise and the current through conducting switch pair to fall to zero naturally resulting in ZCC. Later the body diodes across switch pair start conducting and their gating signals are removed leading to ZCS turnoff of devices. Then the device voltage raises and clamped at reflected output voltage. For the simplicity the study of operation and analysis, the following assumptions are made: A) boost inductor L is large enough to keep constant current. B) All active and passive components are assumed ideal. C) Series inductor L_{lk} includes the leakage inductance of HF transformer. With appropriate design of the HF transformer, external series inductor could be avoided. D) Magnetizing inductance is infinitely large.

Steady state operating waveforms are shown in Fig.3. the primary switch pairs S_1-S_4 and S_2-S_3 are operated with identical gating signals phase shifted with each other by 180^0. The duty cycle is kept higher than 50%. The operation during different intervals in one half cycle is explained with equivalent circuits shown in Fig.4.

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Interval 1 (Fig.4a; $t_0 < t < t_1$): In this interval, primary side H-bridge switches S_2 and S_3 anti-parallel body diode D_6 of secondary side switches are conducting. The current through series inductor L_{lk} is negative and constant. Power is transfer to the load through HF transformer.

Interval 2 (Fig.4b; $t_1 < t < t_2$): At $t = t_1$, primary switches S_1 and S_4 are turned on. The corresponding snubber capacitors C_1 and C_4 discharge fastly in a very short period.

Interval 3 (Fig.4c; $t_2 < t < t_3$): Now all four primary switches are conducting. Reflected output voltage $V_0/2n$ appears across series inductor L_{lk} and diverts the current through switches S_2 and S_3 into switches S_1 and S_4. Therefore, primary current starts increasing linearly. It causes currents through previously conducting devices S_2 and S_3 to reduce linearly while switches S_1 and S_4 start conducting with zero current which helps reducing associated turn-on loss. Since the anti-parallel body diode D_6 is conducting. S_6 can be gated on for ZVS turn on. At the end of this interval, D_6 commutates naturally. Primary current of transformer reaches zero and ready to change polarity.

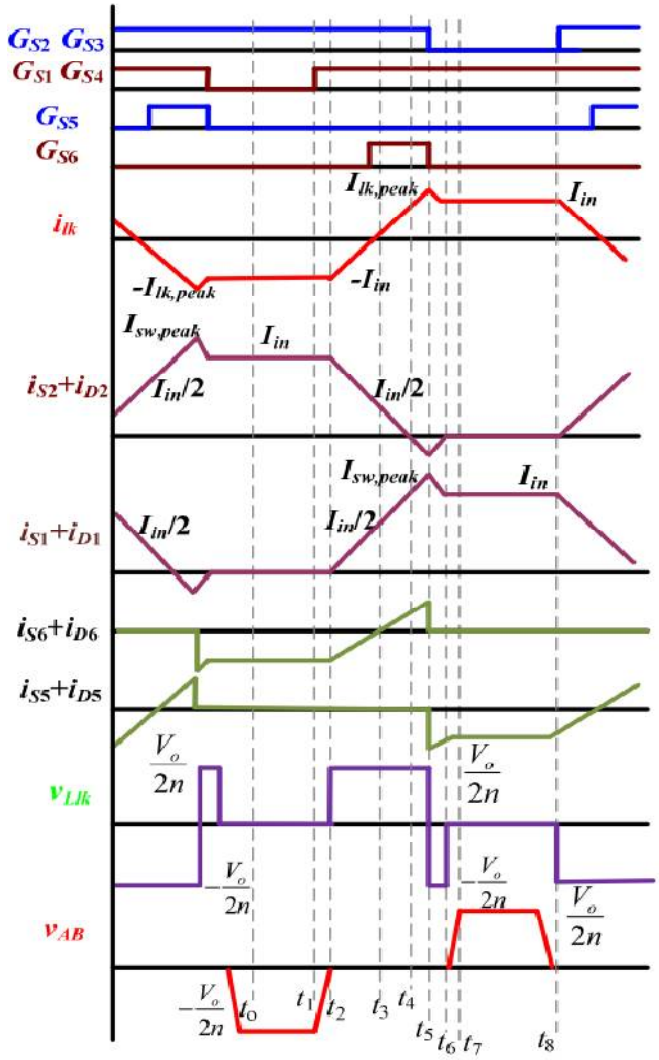

Fig.3 operating waveforms

Interval 4 (Fig.4d; $t_3 < t < t_4$): in this interval, secondary side swich S_6 is turned on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3. At the end of this interval, the primary devices S_2 and S_3 commutate naturally and their respective currents reach zero obtaining ZCS. The full current, i.e. input current is taken over by devices S_1 and S_4, and transformer.

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Interval 5 (Fig.4e; $t_4 < t < t_5$): In this interval, the primary or series inductor current increases further with the same slope and anti-parallel body diodes D_2 and D_3 are start conducting causing extended zero voltage to appear across the outgoing or commutated switches S_2 and S_3 to ensure ZCS turn off. Now the secondary device S_6 is turned off.
At the end of this interval, currents through transformer, switch S_1 and switch S_4 reach their peak value. This interval should be short to limit the peak current through the components reducing the current stress and kVA ratings.
Interval 6 (Fig.4f; $t_5 < t < t_6$): During this interval, switches S_2, S_3 and S_6 are turned off. Anti-parallel body diode of switch S_5 takes over the current immediately. Therefore, the voltage across the transformer primary reverses polarity and the current through it starts decreasing. The currents through the switches S_1 and S_4 and body diodes D_2 and D_3 also start decreasing.
At the end of this interval, currents through D_2 and D_3 reduce to zero and diodes are naturally commutated.
Interval 7 (Fig.4g; $t_6 < t < t_7$): In this interval, snubber capacitors C_2 and C_3 charge to $V_0/2n$. switches S_2 and S_3 gain forward blocking mode.
Interval 8 (Fig.4h; $t_7 < t < t_8$): In this interval, currents through S_1 and S_4, transformer are constant at input current I_{in} and current through anti-parallel body diode of the secondary switch D_5 is I_{in}/n.
For the rest of HF cycle, the intervals are repeated in the same manner with other symmetrical devices conducting to complete the full HF cycle.

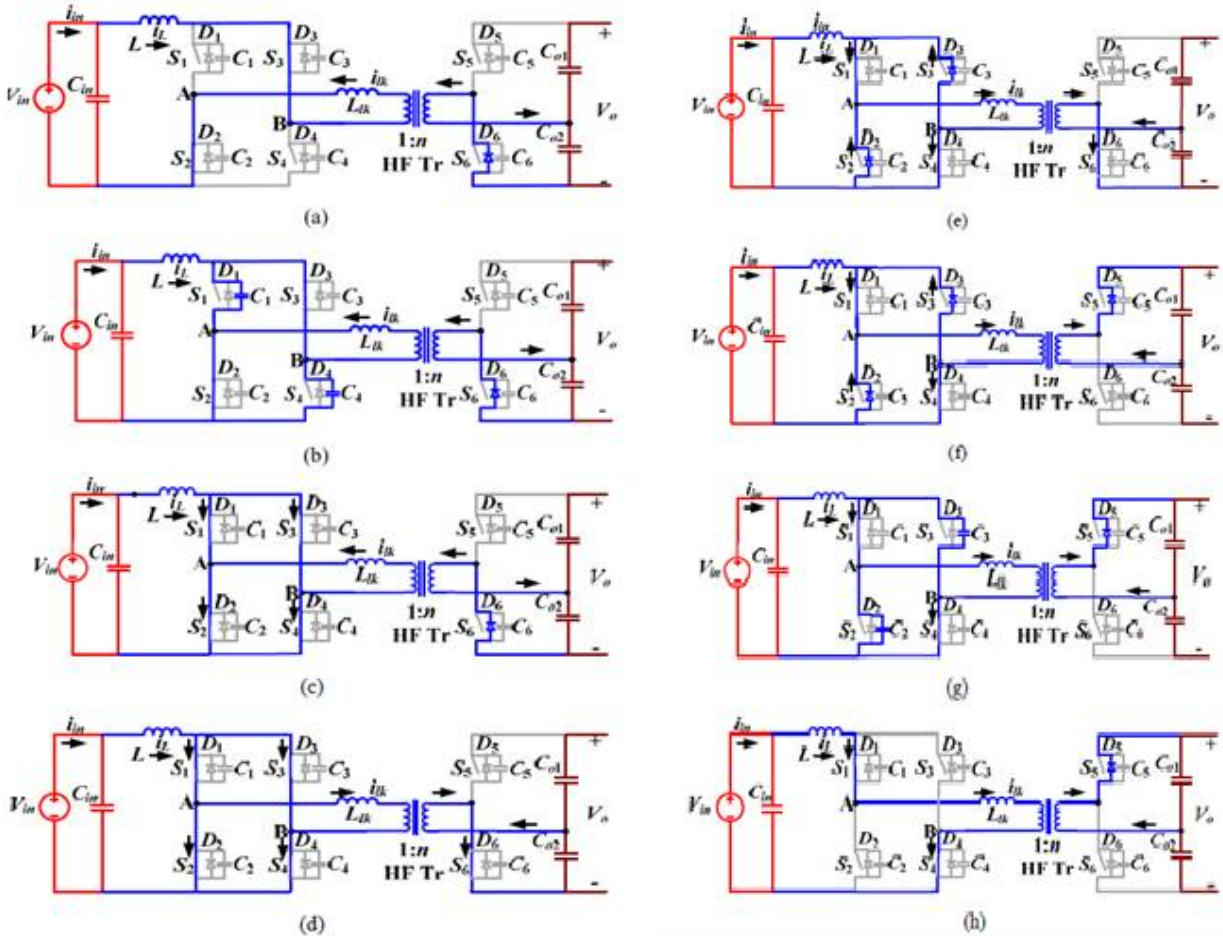

Fig.4. Equivalent circuits during different intervals of the operation of the converter.

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IV.DESIGN PROCEDURE

In this section, design procedure is illustrated by a design example considering the following specifications: *Po*=250W, *Vin*=12V, *Vo*=150 ~ 300V, *fs*=100kHz. The design equations are presented to calculate the components rating.

(1) Average input current is *Iin=Po/(ηVin).* Assuming an ideal efficiency η of 95%, *Iin*=21.9

(2) Maximum voltage across the primary switches is

$$V_{P,sw} = \frac{V_0}{2 \cdot n} \quad (1)$$

(3) Input and output voltages are related as

$$V_0 = \frac{n \cdot V_{in}}{1 - d} \quad (2)$$

Where *d* is the duty cycle of primary switching devices.. Equation (2) is derived by assuming body diode conducts for quite short time just to ensure ZCS of primary switches(interval 6) without significantly increasing the peak current. However, at light load, the diode conduction time is relatively large and (2) not valid any more. Due to the existence of longer body diode conduction period, the output voltage is boosted to higher value than that of nominal boost converter. For such cases, (2) is modified into following

$$V_0 = \frac{n \cdot V_{in}}{(1 - d - d')} \quad (3)$$

Where *d'* given by,

$$d' = d - 0.5 - \frac{4 \cdot n \cdot I_{in} \cdot L_{lk\_T} \cdot f_s}{2 \cdot V_0} \quad (4)$$

(4) Series inductance L_{lk} is calculated using

$$L_{lk} = \frac{V_0 \cdot (d - 0.5)}{4 \cdot n \cdot I_{in} \cdot f_s} \quad (5)$$

(5) The output power can be derived as

$$P = \frac{4n \cdot v_{in}^2 - v_0 \cdot v_{in} \cdot (3 - 4d)}{16 \cdot n \cdot L_{lk} \cdot f_s} \quad (6)$$

Turns ratio of HF transformer is selected based on conduction losses, which mainly consist of the conduction losses in the primary switches because they carry higher currents. Increasing the turns ratio may reduce the maximum voltage across the primary switches allowing low voltage switches with low on state resistance. but, higher turns ratio yields high switch rms current. Voltage regulation over varying input voltage is another concern. An optimum turns ratio *n*=5 and duty cycle *d=0.*8 are selected to achieve low overall conduction losses. Output voltage can be regulated from 150V to 300V by varying the duty cycle. Leakage inductance of L_{lk}=2.05μH is obtained from (5) for the given values.

(6) Value of boost inductor is given by

$$L = \frac{V_{in} \cdot (d - 0.5)}{\Delta I_{in} \cdot f_s} \quad (7)$$

Where, ΔI_{in} is the boost inductor ripple current. For ΔI = 1A, L=36μH.

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(7) the current and voltage stress of major components are given in Table I.

Table I Current and Voltage stress of major components

Components	Current Stress			Voltage Stress
	Peak Current	Average Current	RMS Current	Peak voltage
Primary Switches $S_1 \sim S_4$	I_{in}	$I_{P,av} = \frac{I_{in}}{2}$	$I_{P,rms} = I_{in}\sqrt{\frac{2-d}{3}}$	$V_0/2n$
Secondary Switches $S_5 \sim S_6$	I_{in}/n	$I_{S,av} = \frac{P_o}{2 \cdot V_o}$	$I_{S,rms} = \frac{I_{in}}{2n}\sqrt{\frac{2d-1}{3}}$	V_o
Secondary Switches Body Diodes $D_5 \sim D_6$	I_{in}/n	$I_{D,av} = \frac{I_{in} \cdot (7-6d)}{8n}$	$I_{D,rms} = \frac{I_{in}}{2n}\sqrt{\frac{11-10d}{3}}$	V_o
HF transformer	VA rating : $VA_{x-mer} = \frac{V_o \cdot I_{in}}{2n}\sqrt{\frac{2 \cdot (5-4d) \cdot (1-d)}{3}}$			

(8) VA rating of each HF transformer is given by

$$VA_{x-mer} = \frac{V_0 \cdot I_{in}}{2n}\sqrt{\frac{2 \cdot (5-4d) \cdot (1-d)}{3}} \qquad (8)$$

V.EXPERIMENTAL RESULTS

A) SIMULATION RESULTS

The proposed converter has been simulated using MATLAB & SIMULINK 2013b. Simulation results are illustrated in Fig.6, which coincides closely with theoretical operating waveforms in Fig.3

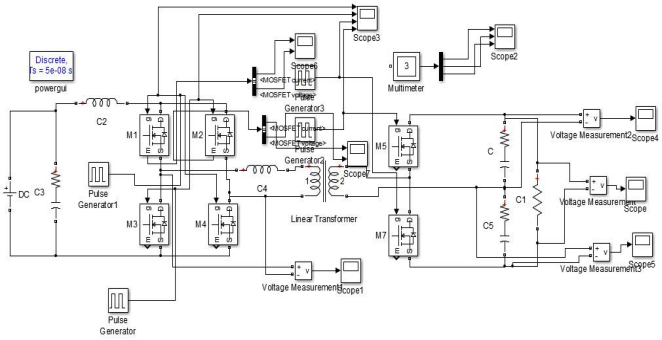

Fig.5. simulated circuit of proposed converter.

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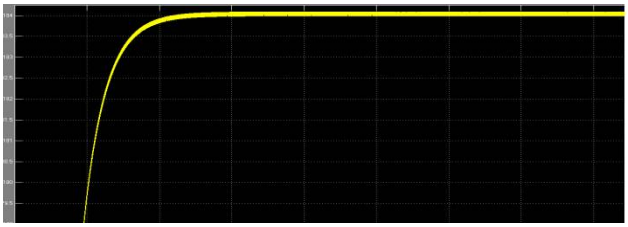
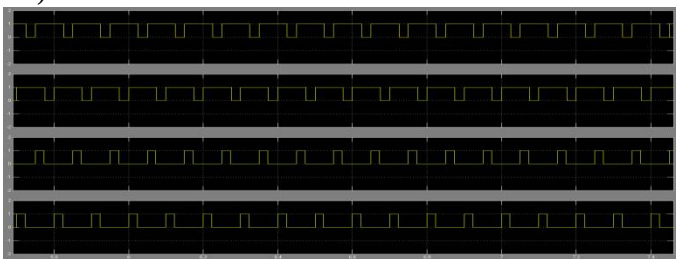
INPUT VOLTAGE: 12V DC

OUTPUT VOLTAGE: Fig.6(a) clearly shows the output voltage across resistor which is the total voltage of both output capacitors.



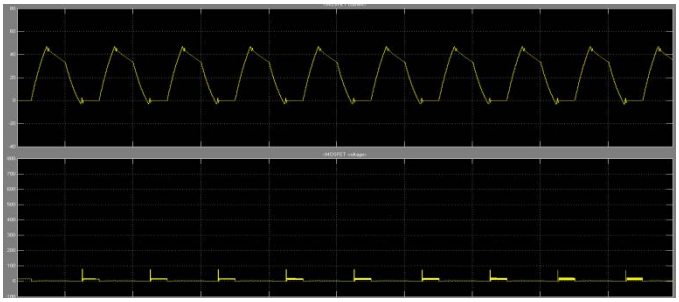
(a)

GATING SIGNALS TO THE MOSFETS: Fig.6(b) shows the gating signals generated to trigger the primary and secondary switches(MOSFET's).



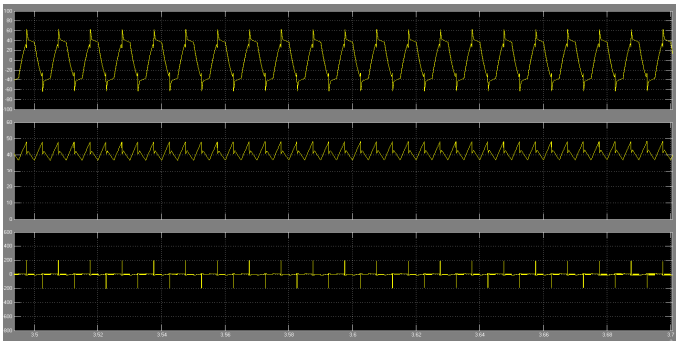
(b)

MOSFET VOLTAGE AND CURRENT:



(c)

SWITCHING VOLTAGE AND CURRENT: Fig.6(d) shows the switching current and voltage, which indicates the ZCC of switches.



(d)

Fig.6. simulation waveforms

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B) HARDWARE RESULTS

The hardware implementation of proposed converter prototype is shown in Fig.7. in proposed converter all subsystems such as transformer, MOSFET switch, capacitor and controller parts are implemented.

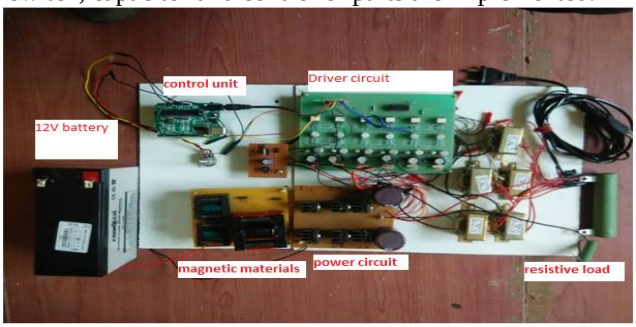

Fig.7. converter hardware Constant load: 470 ohms.

Duty cycle (%)	Voltage (V)
60	70
70	86
80	110

Constant dutycycle:70%

Resistance (ohms)	Voltage (V)
100	54
470	86
570	92

VI.CONCLUSION

A novel soft switching bidirectional current fed full bridge voltage doubler is proposed. Steady state operation, analysis and design are illustrated. Simulation results clearly demonstrate that the proposed converter maintains ZCS of primary devices and ZVS of secondary devices. Proposed novel modulation technique clamps the voltage across the primary side switches naturally with ZCC and therefore eliminates the necessity for active clamp or passive snubbers required to absorb device turn off voltage spike. Soft switching and voltage clamping is inherent and is maintained independent of load. Usage of low voltage devices leads to low conduction losses in primary switching devices, which is significant due to higher currents on primary side. The converter is suitable for higher boost ratio and high current applications, i.e., interfacing low voltage to higher voltage DC bus with higher current such as fuel cell vehicles.

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