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Design of Quadded Logic and Quadded Transistor Using Low Power Consumption

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ABSTRACT: CMOS technology have made digital circuits and systems very sensitive to manufacturing variations, aging and/or errors. A Fault-tolerant techniques using hardware redundancy have been extensively investigated for better reliability. Quadded Logic [QL] is interwoven redundant logic technique that corrects errors by switching them from the critical to subcritical status. however, QL cannot correct errors in the last one or two layers of a circuit. In contrast to QL, and Quadded transistor (QT) corrects errors while performing the function of a circuit. In this paper, a technique that the combined QL with QT is proposed to take an advantage of both techniques. The proposed QLQT technique is evaluated by the compared with other fault-tolerant techniques such as triple modular redundancy (TMR) and triple interwoven redundancy (TIR). Simulation results show that QLQT has a better reliability than the other fault-tolerant techniques. These results providing a new insight for implementing efficient fault-tolerant techniques in the design of reliable circuits and systems.

KEYWORDS: Quadded Logic, Quadded Transistor, Redundancy, Soft errors, Fault tolerant, Reliability.

I. INTRODUCTION

Fault tolerance is the ability of the system to continue to perform its tasks after the occurrence of faults. The ultimate goal of fault-tolerant design is to prevent system failure from occurring. Various requirements satisfied by the introduction of fault tolerance to a system include: dependability, reliability, availability, safety, performance, maintainability, and testability. Since soft errors are likely to affect a circuit on a temporary basis, a time-redundant soft error-tolerant technique have been proposed in [6]. However, TMR has been shown to be vulnerable to multiple bit errors in FPGA devices [7], and it may not work very well for highly unreliable nanoscale technologies [8, 9]. Recently, a *quadded-transistor* (QT) technique have been proposed for tolerating permanent defects in the digital circuits [10]. In the QT technique, every transistor in a design of circuit is placed with four same transistors and any single transistor error in the quadruple can be tolerated. The gate capacitance is also quadrupled, thus delay is increased.

A fault-tolerant technique is proposed by combining quadded logic with quadded transistors implemented by the last layer of a the circuit. In this technique, quadded transistors replace every transistor in the gates that produce the circuit outputs, while the quadded logic is implemented by the remaining circuit. This implementation is therefore referred to the *QLQT* technique and it takes advantage of both QL and QT. In QLQT, QT implements the logic function of the gate and simultaneously serves as a voter or arbiter. No additional voter is needed in QLQT . The QT voters in QLQT are also fault-tolerant, they lose the hard core nature as found in TMR. The proposed QLQT technique is evaluated using stochastic computational models [11-13] and compared to TMR, TIR and QL through an extensive simulation of benchmark circuits. It is shown that in most cases, the proposed QLQT performs the best in terms of reliability.

II. TRIPLE MODULAR REDUNDANCY

TMR is the most common and simplest case of NMR. In this technique, each module replicated by three functionally identical modules and the outputs of the modules are voted through a majority voter. TMR is good at tolerating any single fault in a module. For a constant component failure rate, an increase of the module size increases the probability of having multiple faults; however, a decrease in module size also results in the use of more voters and

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possibly a lower reliability. Hence, the reliability of TMR is dependent on the size of the modules and the voting process.

In simplest terms, TMR involves triplicating the logic functioning of the device and including a set or series of voter circuits to determine majority output for proper operation. In majority voting, the best two of three wins the vote and is considered the correct output. Unfortunately, if there is an error in the voter circuits themselves or the output path, then the voting scheme can lead to an overall logic failure. Triplicating voters guards against this type of failure. As such, the voters should be designed with sufficient logic to detect errors when compared to the other voting logic to trigger complete or partial reconfiguration of that portion in the TMR scheme. To better design for the environment of space, and to reflect the increased probabilities of SEUs and MBUs in newer FPGA series, new methods of TMR have been developed.

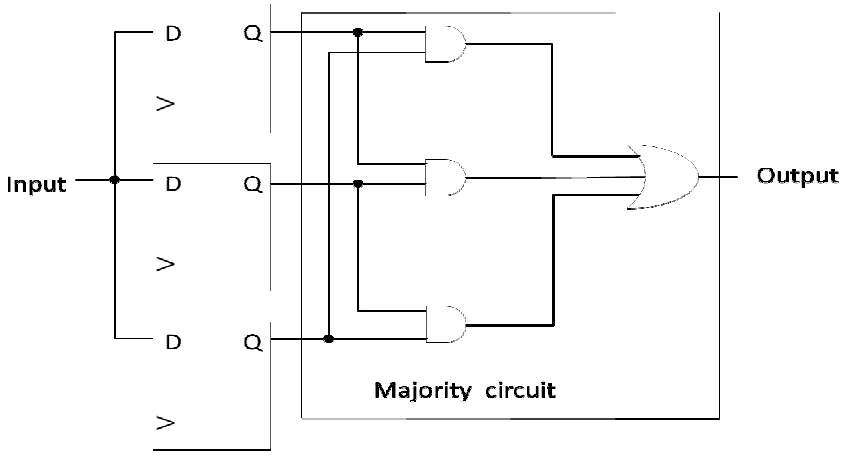

Fig1: Triple modular redundancy circuit

III. QUADDED LOGIC

Quadded logic [11, 14, 15] is an ad hoc configuration of the interwoven redundant logic. A quadded circuit implementation based on NAND gates replaces each NAND gate with a group of four NAND gates, each of which has twice as many inputs as the one it replaces. The four outputs of each group are divided into two sets of outputs, each providing inputs to two gates in a succeeding stage. The interconnections in a quadded circuit are eight times as many as those used in the non-redundant form. In a quadded circuit, a single critical error .1 or 0 is correctable after passing through two stages of logic and a single sub-critical error .0 or 1 will be corrected after passing a single stage. In quadded logic, it must be guaranteed that the interconnect pattern at the output of the stage differ from the interconnect patterns of any of its input variables. While quadded logic guarantees tolerance of the most single errors, errors occurring at the last two stages of logic may not be corrected. Figure 2 shows an example of TMR and quadded logic circuits. In, a defect tolerant computational architecture is proposed based on a heterogeneous CMOS–carbon nano tube fabric. A methodology for realized by the coded Boolean functions implemented in nano-gates is introduced. It is shown by the yield of nano-circuits is significantly increased by the presence of high defect density. Have analyzed the use of series-parallel or bridge configurations of the application of redundancy to relay networks. Has evaluated the reliability of the quad-relay structure shown and has shown its application using bipolar junction transistors. However, the reliability of the single structure is evaluated and no extensive circuit reliability analysis is made.

Defect Avoid Techniques Unlike defected tolerant techniques which are designed to work properly despite the presence of defects, defect avoidance techniques are based on the different principle. They are based on the identification of defective modules and replacing them by other redundant modules through configuration.[17] have proposed a defect avoidance approach to nano system design based on a large recon- figurable grid of nano blocks. Each of these blocks can be configured as one of the basic logic building blocks like AND, OR, XOR, a half-adder. The approach is based on the mapping defects on nano blocks and synthesizing a feasible configuration realized the application for each nano fabric instance. The main limitation of this approaches that it requires mapping, synthesis,

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and configuration at such a fine granularity, making it not scalable for large nano systems [8]. Furthermore, extensive connectivity among nano blocks is required for defect mapping. To address the scalability, reliability, density challenges the emerging nanotechnologies. [8] proposed a hierarchy of design abstractions, constructed by the reconfigurable fabric regions, whereby designers assign small functional flows too.

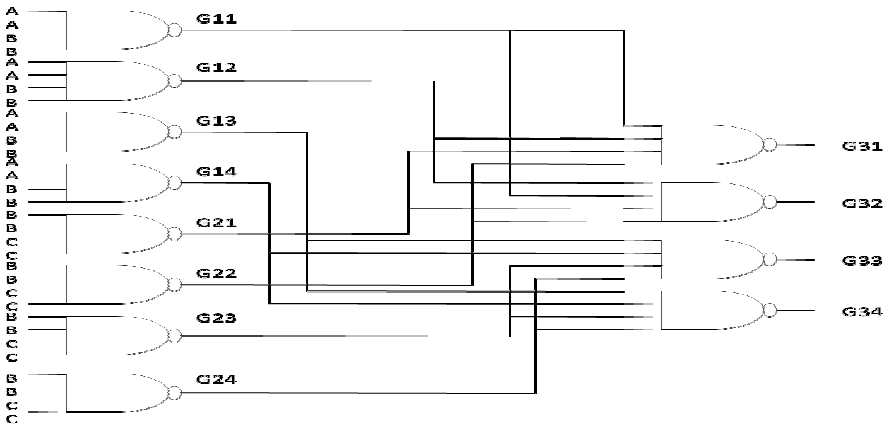
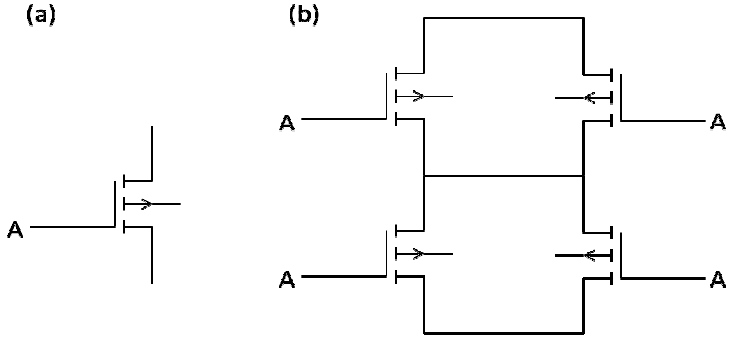


Fig2 : Quadded logic circuit

IV. QUADDED TRANSISTOR

Quadded Transistor uses four transistors for the function of a single transistor. As a transistor with input A is replaced by a Quadded-transistor structure, which is logically equivalent to a function [A+A]. Therefore, an error is any single transistor can tolerated by QT. Many double errors can also to be tolerated as long as they do not occur in transistors placed in parallel. The gate capacitance of the Quadded Transistor structure is quadrupled and the replacement of every transistor with Quadded Transistor makes the circuit slower with an area overhead.



(a) Transistor (b) A quadded transistor structure

V. QUADDED LOGIC WITH QUADDED TRANSISTORS (QLQT)

A. Proposed QLQT Technique

In most cases, QL and QLQT show better reliabilities than non-redundant, TMR and TIR circuits. However, they also incur a larger area overhead than TMR and TIR. For some small circuits, QL and QLQT are not as reliable as TMR and/or TIR.QL has the ability to correct single errors in two layers, but it also may spread the error into more than

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one gate before correcting it. Hence for circuits containing very short paths from the primary inputs to the primary outputs, such as majority, count and C1908, QL and QLQT are not very effective. Since the probability of having single errors in a short path is high, TMR and TIR could be viable. At a higher gate error rate, however, QL and QLQT are more reliable than TMR and TIR due to their better ability in handling multiple errors. In a large circuit with a high gate error rate, multiple faults are significantly better handled by QLQT than any of the other techniques, thus QLQT achieves the best reliability overall. Note that in QL, a single error in the four outputs is considered to be tolerable and is masked by the majority voting at the output. If all of the signals are required to be error-free to produce a correct output, the advantage of QLQT over QL becomes very significant.

It is overcome the drawbacks of QL and QT, a hybrid design using the QT in QL is proposed to enhance the gates that generate by the primary outputs in a QL circuit. In a QLQT implementation of the benchmark C17 for example, the two NAND gates at the last logic layer are implemented using QT . In QLQT, if any single error in the second-to-last layer of gates or in the last layer of transistors can be correct the QT circuits at the outputs. This provides a significant advantage over QL. However, a critical error at the third layer that would be corrected in QL, may not be necessarily corrected in a QLQT circuit.This is caused by the fanouts of the subcritical errors induced at the second layer onto the last QT structures. However, these errors may not cause an erroneous output due to 1) the errors may propagate to two transistors that are not in parallel in QT, and 2) the errors may be corrected by the other signals due to their subcritical nature. Therefore, the negative effects of the QLQT are rather limited circuit.

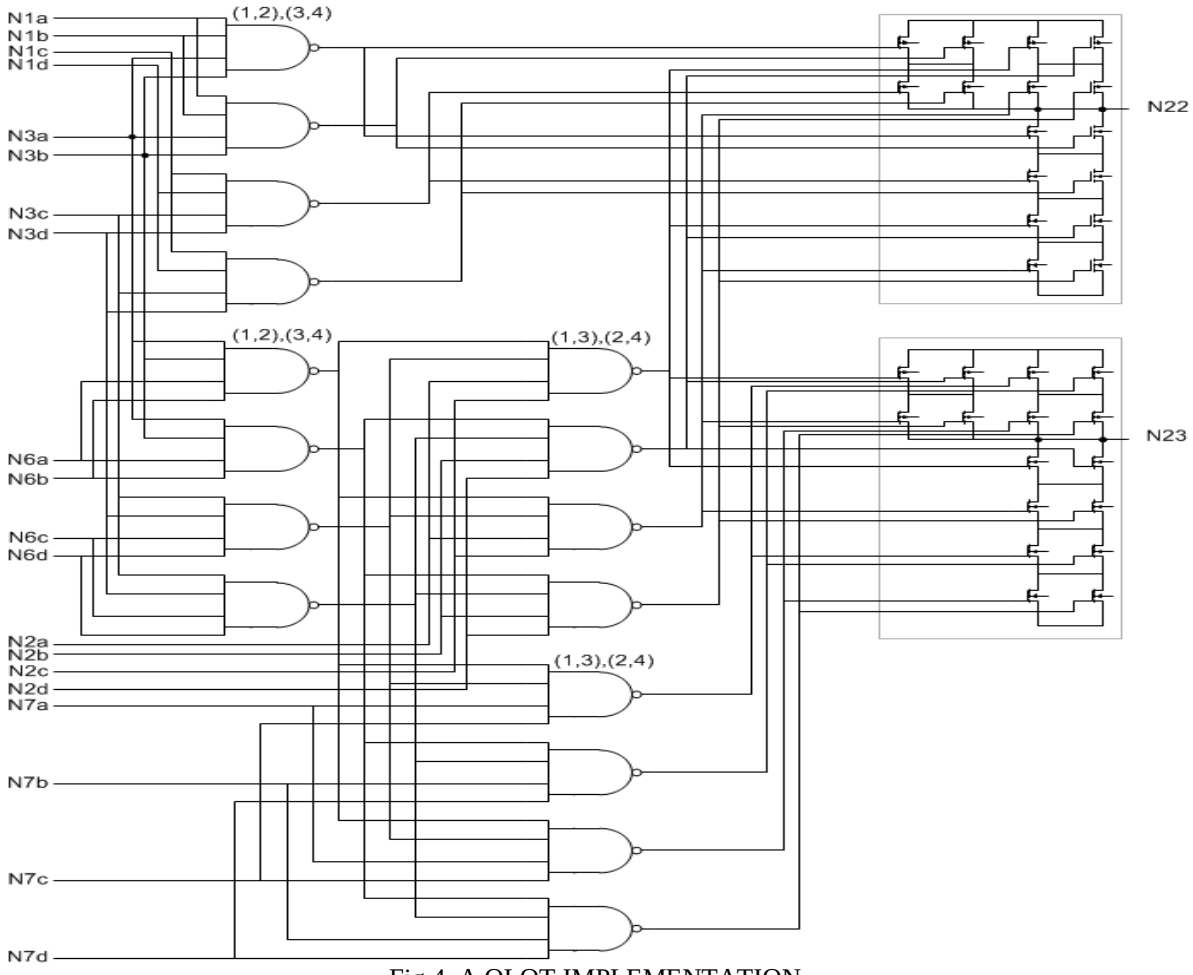

Fig.4. A QLQT IMPLEMENTATION

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B. Comparison on Area, Power and Delay

TMR and TIR, the area is tripled and so the power is consumed due to triplication of the gates. If voters are considered, the area and power are slightly larger than three times of the original circuit, whereas the delay is only marginally larger. QL requires four times as many gates are in the original circuit and twice as many interconnects, i.e., each gate in QL has twice the number of the inputs in the non-redundant circuit. Therefore, the number of transistors in QL is eight times the original circuit. If the gate size is considered for the same delay and power, the required area is larger than the power consumption is no less than the four times the original circuit.

The measures for QLQT are similar, but slightly less than for QL due to the use of quadded transistors is the last layer of the circuit. The number of transistors in QT is half of QL.

The area of circuit delay dominated by the load of capacitance, the delay in QL is at least twice as large as in the original circuit due to the fanout of signals into two different gates, where as the delay in the QLQT is slightly smaller than the QL. This is due to the similar delays that the quadded transistors include as the original logic gates would have in the last layer. However, QLQT does not required additional transistors for the voters or arbiters that would be needed in a QL circuit.

VI. SIMULATION RESULTS

Simulation results are reported in Figs. 3 – 5 in ascending order of circuit size. These circuits are equivalent to functional modules of different sizes for implementing the redundancy techniques. Reliability is defined as the joint probability that all outputs are correct for a circuit.

Due to the small size of C17 (with only six gates), the use of redundancy is not justified as it may result in a less reliable structure with the unreliable voters. The reliability of the count circuit (with 179 gates) is plotted in Fig. 3 (a) and (b) for lower and higher ranges of gate error rates. It can be seen that TMR and TIR do not work well at a large gate error rate (such as 0.05). QLQT has the best reliability when the gate error rate is large, whereas in some cases, QL and QLQT are less reliable than TMR and TIR. This is caused by the short data paths in this circuit, such that some errors cannot be corrected before reaching the outputs. Similar considerations also apply to the majority circuit (with 16 gates) and C1908 (with 816 gates).

The reliability of C6288 (2399 gates). QL and QLQT have a clear advantage over TMR and TIR, especially when the gate error rate is large. For a circuit of this size, QL performs very well and its reliability is very close to QLQT. For the two triple redundancy techniques, TMR improves the circuit reliability, whereas TIR deteriorates it. This is due to the interwoven nature of TIR, i.e., errors can spread, whereas errors are confined in the same module in TMR. Similar behavior in reliability has also been observed for C3540.

A)**Comparisons of simulation results:**

Fault-Tolerant Techniques	Average power(µ watts)
Triple Modular Redundancy technique	46.92
Quadded logic	23.32
Quadded Logic and Quadded Transistor	15.38

Fig.5 Comparisons of Average power

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Fault-Tolerant Techniques	Delay
Triple Modular Redundancy technique	2.094n
Quadded logic	4.867n
Quadded Logic and Quadded Transistor	1.087n

Fig6: Comparison of delay

VII. CONCLUSION

This paper has proposed a novel fault-tolerant technique that uses both quadded logic and quadded transistors (QLQT). In the QLQT technique, QTs are implemented at the last layer of a circuit, while the remaining circuit is implemented by QL. Simulations have shown that the proposed QLQT technique improves QL by using QTs to implement functions of both the output gates and voters. The fault-tolerant QT circuits correct faults that occur in the last two logic layers, hence leading to a better reliability. Extensive simulations reveal insights with respect to the features and application scopes of these fault-tolerant techniques for reliable circuit and system design.

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