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Modified Five Level Inverter

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ABSTRACT: Multilevel Inverter is very efficient alternative for Medium voltage and High power applications. The demand for Multilevel Inverter is increasing now-a-days since it is impossible to connect the power semiconductor switch to high voltage network directly. One of the most important features of the multilevel Inverter is that as the number of level increases, the THD (Total Harmonic Distortion) in these output-voltage waveform decreases. This paper presents the CHB (Cascaded H-bridge) with equal and unequal dc voltage and their comparison. In order to obtain the increased voltage level Cascaded H-bridge with unequal DC voltage is beneficial than Cascaded H-bridge with equal DC voltage. But there are some disadvantages associated with Cascaded H-bridge with unequal DC voltage. Multilevel Inverter consists of the H-bridges connected in cascade (series). The number of the H-bridge connected in series increases with the increased number of levels. The structure of Cascaded H-bridge is simple as compared to other types of Multilevel Inverter as it does not require clamping diodes and flying capacitors. The advantage of using H-bridge is that both positive and negative level at the output is obtained. This is called the Developed Cascaded H-bridge Inverter. Reduction in the number of power switches, driver circuits and dc voltage sources are advantages of the Developed Single-Phase Cascaded H-bridge Inverter. Since reduced number of components is required in each H-bridge therefore cost and losses are reduced resulting in increased efficiency. With the increased efficiency maximum output is obtained.

KEYWORDS: Multilevel inverter featutes, Modified fivelevel inverter,Total harmonic distortion, SPWM

I.INTRODUCTION

A Power inverter or inverter is an electronic device or circuitry that changes direct current (DC) to Alternating Current (AC). Figure 1.1 shows a conventional two-level inverter. Two level inverter creates two different output voltages V_{dc2} and $-V_{dc2}$when fed with a DC voltage Vdc. To build an AC output voltage, these two voltages are usually obtained using Pulse Width Modulation (PWM). Though this method is effective, yet it creates harmonic distortions on the output voltage, Electro Magnetic Interference (EMI) and high dv/dt.The concept of multilevel inverter is not just creation of output waveform with two levels. Instead different voltage levels are added and higher levels are generated to get a stepped waveform as shown in Figure 1.2. As the number of levels increases, more smoother will be the output waveform. It also has advantages like low harmonic distortion, low dv/dtand less EMI. But, in order to increase the number of levels, more number of components is required and same will make the circuit complex and congested. However the cost of production will also increase.

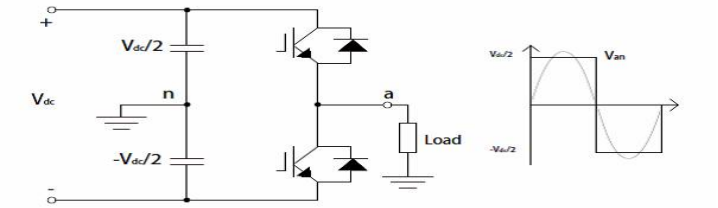

Fig: 1.1. One leg of a two level inverter and output waveform

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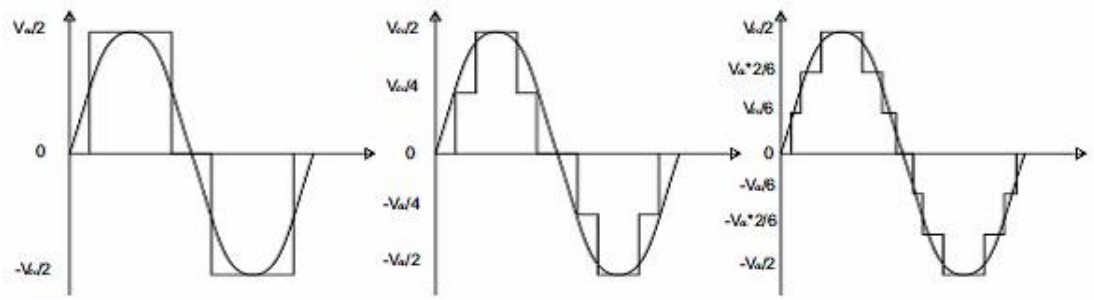

Fig: 1. 2. 3, 5 and 7 level output waveforms of MLI which has been triggered at fundamental frequency

There are several types of multilevel inverters: cascaded H-bridge (CHB), neutral point clamped, flying capacitor and others. In particular, among these topologies, CHB inverters have been focused because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. CHB inverters can also increase the number of output voltage levels easily by increasing the number of H-bridges. However, if the number of output voltage levels is increased, the number of switching devices is also increased, which makes a multilevel inverter more complicated.

The concept of multilevel inverter (MLI) can be better explained using a conventional 3-level inverter as given in Fig 1.3. It is called as 3-level inverter because each phase of it can generate 3 levels of output $+V_{dc}/2$, 0, $-V_{dc}/2$. A three level inverter is very much similar to conventional two level inverter but there are twice as many valves per phase leg. Clamping diodes are also present in this topology and it is connected to the neutral midpoint between two capacitors. The function of the capacitor is to divide the input DC voltage. Here input is V_{dc}, and across each capacitor $V_{dc}/2$ will be obtained. By switching the two switches which are closest to the midpoint, a zero voltage level can be achieved. And now, if the number of valve pairs is increased, the number of levels will also increase. But, in such cases, the component count will increase. That means the number of clamping diodes and coupling capacitors will increase.

When it is compared with conventional inverter the most attractive features of MLI include low harmonic distortion, low voltage stress(dv/dt), can generate smaller common mode voltage and can be operated with lower switching frequencies. By reducing the switching frequency, switching losses can be reduced which is significant in case of inverters. The Multilevel inverter topologies that are investigated in this work are: Neutral- Point Clamped Multilevel Inverter (NPCMLI), Capacitor Clamped Multilevel Inverter (CCMLI), and Cascaded Multicell Inverter (CMCI).

II. MULTILEVEL INVERTER FEATURES

Multilevel converters have received increased interest recently for high-power and medium-voltage applications. They can synthesize switched waveforms with lower levels of harmonic distortion compared to a two-level converter. The multilevel concept is used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. The most attractive features of multilevel inverters are as follows:

1) They can generate output voltages with extremely low distortion and lower dv/dt.
2) They draw input current with very low distortion.
3) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor ….bearings. In addition, using sophisticated modulation methods, CM voltages can be ….eliminated.
4) They can operate with a lower switching frequency.

By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped); capacitor- clamped (flying capacitors); and cascaded multicell with separate dc sources.

In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic

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elimination, and space-vector modulation (SVM).Three major types of MLIs applied in industrial applications are flying capacitor, diode clamped and H-bridge converter with separate DC sources. Flying capacitor type multilevel inverters are not widely used because of its bulk nature due to the presence of a large number of capacitors, diode clamped multilevel inverters have the highest cost of implementation compared to flying capacitor and cascaded H-bridge multilevel inverters.

Cascaded H-bridge multilevel inverter is simpler than diode clamped and flying capacitor multilevel inverter topologies because of some advantages such as automatic voltage sharing, smaller switching stresses, low switching redundancy and requirement of least number of components, no high rated capacitors and diodes. Main disadvantage of cascaded H-bridge multilevel inverter is that for increasing the number of levels of output voltage, number of DC input sources is to be increased, since for the operation of cascaded H-bridge multilevel inverters separate DC sources are required for each H-bridge and at the same time number of switches is also increasing. For example, to obtain a five level inverter output, number of input DC sources required is two and the number of switches is eight, this is not so advantages. These drawbacks can be overcome by using a single source multilevel inverter with reduced number of switches which is suitable for multi string solar panel applications.

III. MODIFIED FIVELEVEL INVERTER

Fig.3.1. shows a 5-level transistor clamped MLI in which a normal H-Bridge inverter and an auxiliary circuit which consisting of a single switch is combined. The power circuit of Transistor Clamped H-Bridge (TCHB) multilevel inverter is such that it can produce more output levels with reduced number of power switches. The number of switches is reduced in TCHB topology, so the size of device is reduced, stress is reduced, and also THD is reduced.

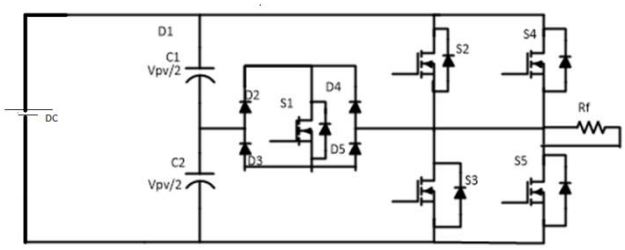

Fig: 3.1. Modified five level inverter circuit

TCHB topology needs only one source. So, in PV applications TCHB is better. Fig: 3.1 have only five switches. And they provide five level output. The arrangement shown in this figure is considered as a cell. And cascading of this cell provides more number of outputs.

Modes of operation

The required five output voltage levels are generated as follows:

1) Level Vdc: S2 is in ON state, connects the load positive terminal to Vdc, and S5 is in ON state, connects the load negative terminal to ground. The other switches are OFF thus the applied voltage to the load terminals is Vdc. Fig. 3.2 shows the current paths at this stage.

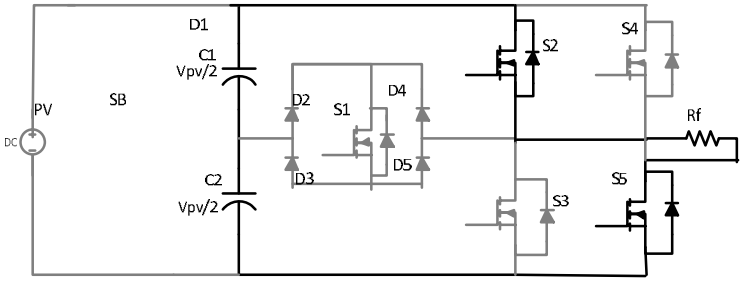

Fig: 3.2. Generation of Vdc voltage level and load current path

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2) Level Vdc/2: The auxiliary switch, S1 and S5 is ON and the other controlled switches are OFF; the voltage applied to the load terminals is Vdc/2. Fig. 3.3 shows the current paths at this stage.

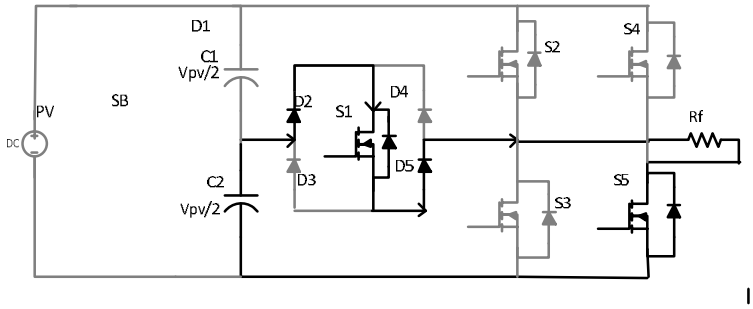

Fig: 3.3. Generation of Vdc/2 voltage level and load current path

3) Zero output: The two main switches S3 and S5 are ON, short-circuiting the load. All other controlled switches are OFF; the voltage applied to the load terminals is zero. Fig. 3.4 shows the current paths at this stage.

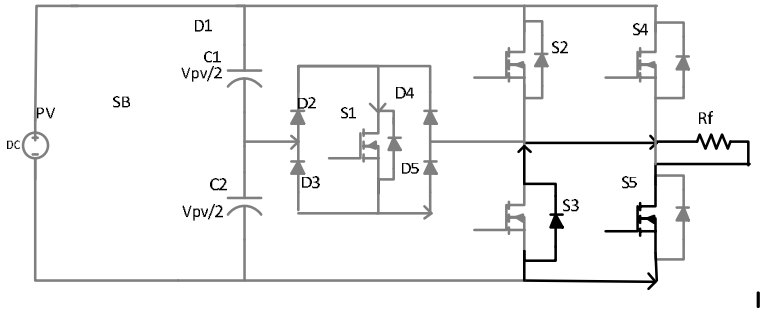

Fig: 3.4. Generation of zero voltage level and load current path

4) Half-level negative output, Vdc/2: The auxiliary switch, S1 is ON and S4 is ON and the other controlled switches are OFF; the voltage applied to the load terminals is - Vdc/2. Fig. 3.5 shows the current paths at this stage.

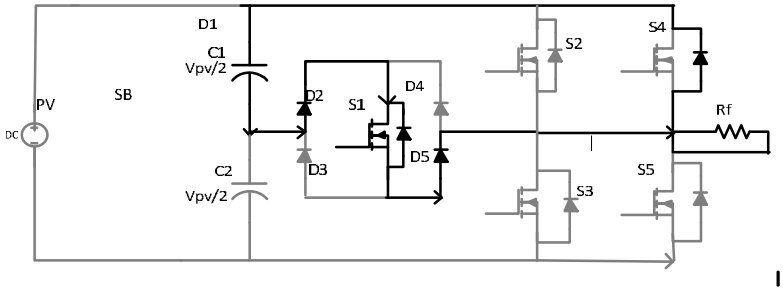

Fig: 3.5. Generation of -Vdc/2 voltage level and load current path

5) Maximum negative output: S4 is ON and S3 is ON and the other controlled switches are OFF; the voltage applied to the load terminals is - Vdc. Fig. 3.8 shows the current paths at this stage.

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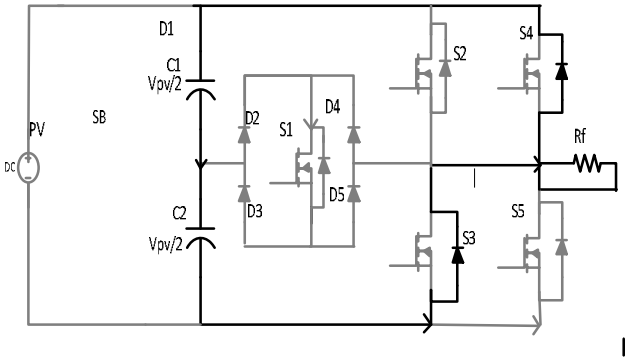

Fig: 3.6. Generation of -Vdc voltage level and load current path

Control scheme

A single carrier multi reference PWM technique is used to generate the switching signals. A five level inverter requires four high frequency carrier signals and one reference signal for a multi-carrier SPWM. A multi-reference single carrier SPWM requires two reference signals and single high frequency carrier signal for obtaining a five level inverter. Here both the reference signals are compared with a carrier signal. The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal.

In this topology five level output voltage is obtained by reduced number of switches compared to that of conventional cascaded H-Bridge multilevel inverter.

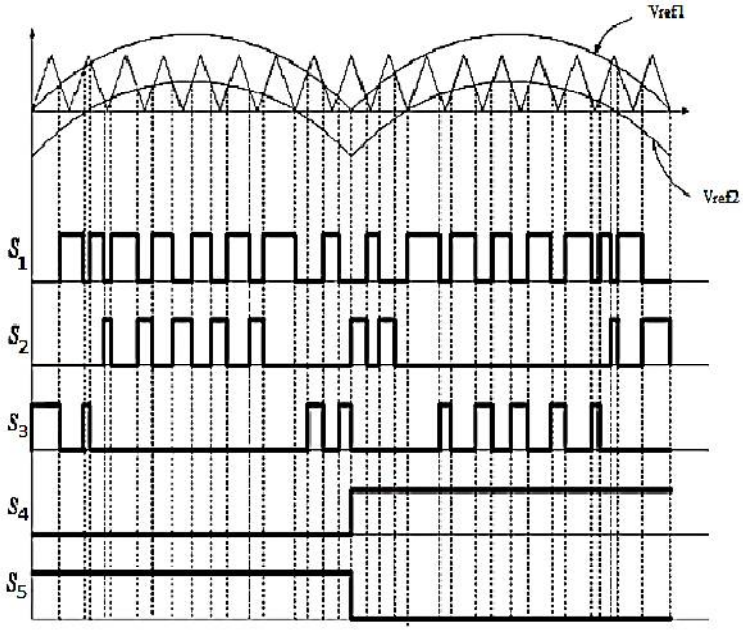

Fig: 3.7. Switching pattern for generating 5-level PWM output voltage.

Two reference signals Vref1 and Vref2 will take turns to be compared with the carrier signal at a time. If Vref1 exceeds the peak amplitude of the carrier signal Vcarrier, Vref2 will be compared with the carrier signal until it reaches zero. At this point onwards, Vref1 takes over the comparison process until it exceeds Vcarrier. This will lead to a switching pattern as shown in Fig.3.7. Switches S1- S3 will be switching at the rate of the carrier signal frequency while S4 and S5 will operate at a frequency equivalent to the fundamental frequency.

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Table: 3.1. level Inverter output voltage during s1−s5 switch on and off

LEVELS	S1	S2	S3	S4	S5	OUTPUT VOLTAGE
1	0	0	1	0	1	0
	0	0	0	1	1	
2	1	0	0	0	1	+Vpv/2
3	0	1	0	0	1	+Vpv
4	1	0	0	1	0	-Vpv/2
5	0	0	1	1	0	-Vpv

The switching states of TCHB inverter is given in table: 3.1. The triggering of switches can be done by using PWM method in simulation. The hardware implementation of such inverters is also done by the help of these switching states.

IV. RESULT AND DISCUSSION

Here single sine wave and two carrier waves are used for the purpose of pulse generation.

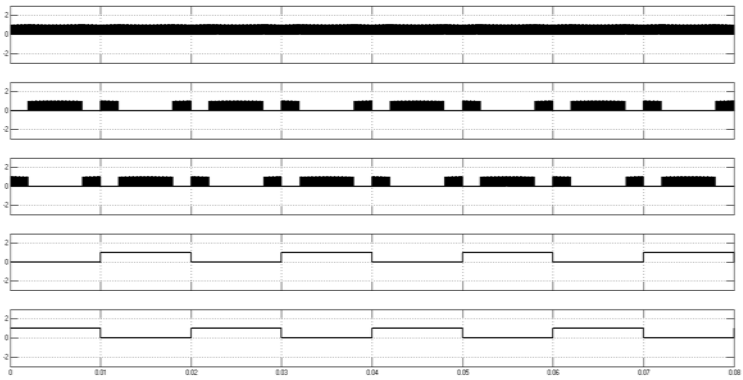

Fig: 4.1 Pulse waveform of five level inverter switches.

The pulses obtained from the PWM technique is given in fig: 4.1 These pulses are given to the switches S1-S5, to obtain the corresponding five level output voltage. That means the conversion of DC voltage to AC can be done by the help of these pulses.

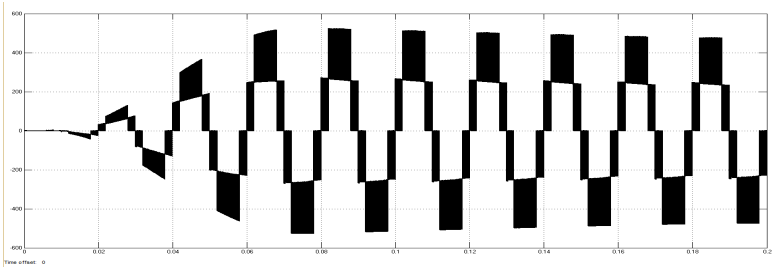

Fig: 4.2 Output voltage waveform of five level of inverter

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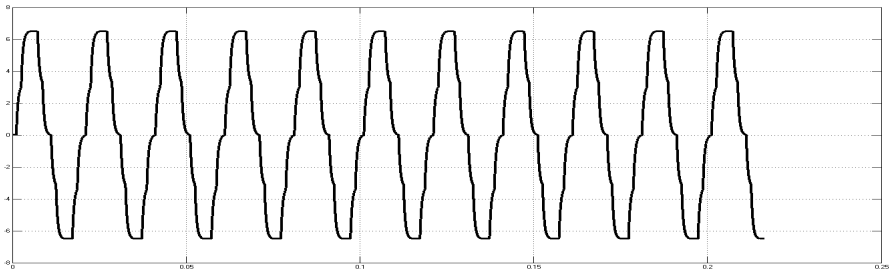

Fig: 4.3 Output current waveform of five level inverter

Output voltage and current waveforms are shown in fig: 4.2 and fig: 4.3 respectively. Five levels are clearly obtained in the output. And each levels are equal in magnitude.

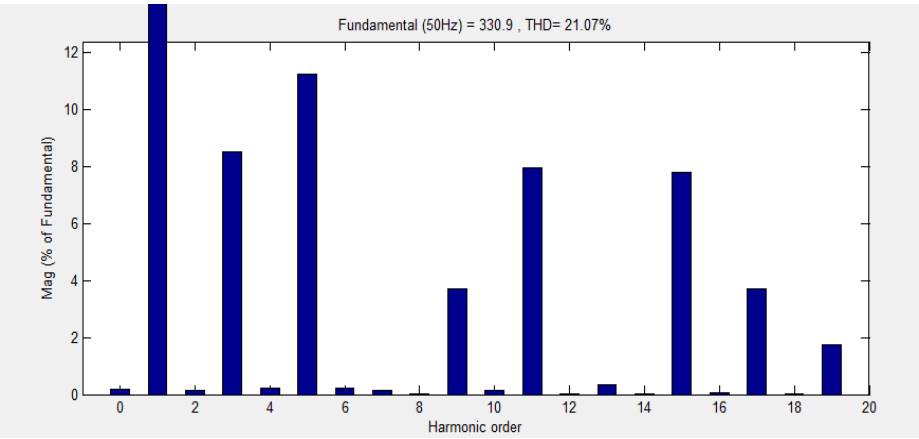

Fig: 4.4 THD of five level inverter

The THD of basic cell shown in fig: 4.4 According to this the value of THD is 21.07%, which means, this is a high distorted wave. However the presence of even harmonics is less

VI.CONCLUSION

Thus Through this section we learned about different multilevel inverter topologies, different modulation techniques and are analyzed related to our project. The proposed inverter is simulated and output is verified. In symmetrical and asymmetrical cascading methods, same number of switches is used. But the output levels are different because of the cascading method.

Experimental results indicate that the THD of the modified five level inverter is much lesser than that of the conventional five-level inverter. The number of switches used in twenty five level inverter is less and so the switching stress and development cost can be reduced.

The advantages of proposed topology are:

- Harmonics distortion is very low
- Reduced cost
- Reduce heat loss
- Reduce switching loss
- Increase efficiency
- High voltage capability with voltage limited devices

The levels of inverter output can be increased by adding more cells to the inverter circuit. The only criterion is that the nearer cells have voltage ratio 1:5. By using this way the THD of output voltage can be reduced and also get perfect AC as output.

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