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Review of Sigma-Delta ADC

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ABSTRACT: This paper presents the detailed study of sigma-delta analog to digital converter. The operations, characterizing parameters and different structures proposed are presented in fundamental form. The various techniques and methods that make the sigma-delta ADC advantageous over the conventional Nyquist rate converters have been discussed.

KEYWORDS: Sigma-Delta ADC, Sigma-Delta Modulator, SNR, Oversampling converters, Incremental ADC, Sturdy MASH SD-ADC, Decimation Filter.

I.INTRODUCTION

The advancement of technology requires the high performance devices, to fulfil these requirements the existing devices need revision e.g. high speed digital signal processors, high speed Tele-communication systems, high speed wireless applications, high accuracy instrumentation and measurement systems etc. require the high speed, wide bandwidth, low power and accurate analog to digital converters. A sigma-delta ADC is one such device that fulfils all these requirements.

A sigma-delta ADC is oversampled mixed signal circuit block [1]. It comprises of analog sigma-delta modulator and digital decimation filter. Analog sigma-delta modulator accepts the analog or continuous input signal and outputs a pulse density modulated (PDM) signal.[1],[2]. This output of the modulator is applied to the digital decimation filter that performs the task of low pass filtering and down sampling and provides the digital signal at the Nyquist rate[3]. In sigma-delta ADC the accuracy of the output depends on the performance of the sigma-delta modulator and digital decimation filter.

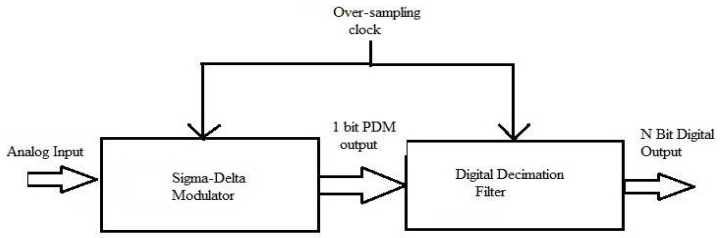

Fig. 1 Block Diagram of Sigma-Delta ADC

This paper is organized as follows. A brief review of sigma delta modulator and its operational features are presented and discussed in section II. In section III, modulator architectural space is discussed. Section IV presents the special variants of sigma-delta modulator. Decimator is discussed in section V and various performances measures are discussed in section VI. Conclusions are drawn in section VII.

II. SIGMA-DELTA MODULATOR

A sigma-delta ADC consists of two parts viz. analog sigma-delta modulator and digital decimation filter [1]. The digital filter is a simple low pass filter with down sampler. So in order to improve the signal-to-noise ratio (SNR) at the output it is the responsibility of the sigma-delta modulator to perform the operations of over-sampling and noise

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shaping [4]. These two techniques employed in sigma-delta ADC make it advantageous over the conventional Nyquist rate converters.

A sigma-delta modulator is basically an analog part composed of basic analog elements such as summer, Integrator, comparator in feed-forward path and a digital to analog converter in feedback path [5] as shown in fig.2.

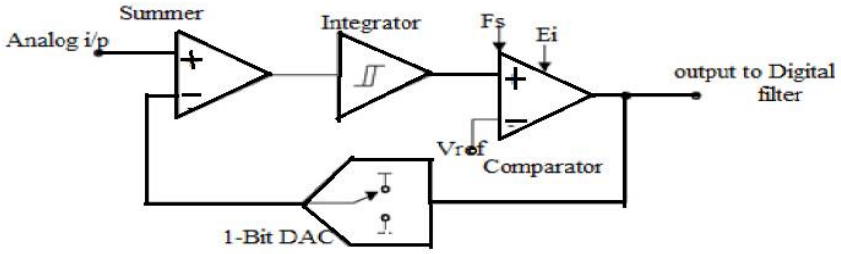

Fig. 2 Block Diagram of Sigma-Delta Modulator

2.1 OPERATION OF THE SIGMA-DELTA MODULATOR

The operation of sigma-delta modulator is as follows. The continuous time (analog) input signal is applied to the summing amplifier (summer), where the error signal E is generated. This error signal is defined as the difference between the input signal and the feedback signal from the DAC. This error signal is summed using the integrator and the output is applied to comparator circuit, operating at the oversampling frequency (f_s), following the integrator circuit. The comparator (1 bit quantizer) outputs a positive pulse for the signal greater than reference signal and negative pulse for signal smaller than reference of the comparator [5].

2.2 QUANTIZATION NOISE

In the process of analog to digital conversion, the process of quantization is the discretization of amplitudes. The noise resulting from the quantization process is called quantization noise and is independent of the input signal. Moreover, the quantization noise power spectral density (PSD) , denoted by $S_e(f)$, is white and uniformly distributed in the sampling frequency, $\pm f_s/2$, where f_s is the sampling frequency. The total quantization power is $\Delta^2/12$, so the amplitude of the power spectral density of quantization noise is given by the following expression:

$$S_e(f) = \frac{\Delta^2}{12} * \frac{1}{f_s} \tag{1}$$

The total power of the quantization noise is uniformly distributed within $\pm f_s/2$ .As it is seen in equation 1 that increasing the sampling frequency reduces the amplitude of the spectral density but doesn't affect the amount of total quantization noise [6].

2.3 OVERSAMPLING

Oversampling is the process of sampling a signal faster than the minimum sampling frequency required to avoid aliasing i.e. Nyquist rate. In oversampling process, the rate at which signal is sampled is represented by Oversampling ratio (OSR), defined as the ratio between the sampling frequency and the Nyquist frequency [6].

$$OSR = \frac{f_s}{2 * f_b} \tag{2}$$

In an oversampled converter, the power of the quantization error is spread in the sampling frequency range $-f_s/2 \text{ to} + f_s/2$, but only a part of the total error falls within the signal band, as long as $f_s > 2 * f_b$. A low-pass decimation filter can be used to eliminate the quantization noise that exists outside the signal band f_b. Thus the quantization noise power can be expressed as

$$P_e = \int_{-fs/2}^{fs/2} S_e(f) |H(f)|^2 df \tag{3}$$

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Therefore, by using an oversampling technique, the quantization noise power of an ADC can be reduced by a factor of OSR. It is an effective way to increase the SNR, and hence the resolution, of an ADC system. Therefore, the peak SNR is given by

$$SNR_p = 10\log(\frac{e_s^2}{P_e}) = 6.02N + 1.76 + 10\log(OSR)dB \quad (4)$$

Equation 4 clearly shows the benefit of oversampling [6].

2.4NOISE SHAPING

Noise shaping is the methods used in sigma-delta ADC. It makes sigma-delta ADC advantageous due to application of a feedback loop. It also extends the dynamic range. The closed loop modulator acts as a high-pass filter (HPF) for quantization-noise (n_q) and as a low-pass filter (LPF) for the input signal. When the signal is over-sampled, the quantization noise power in the Nyquist bandwidth spreads over the wider bandwidth. The total quantization noise is still the same but the quantization noise in the bandwidth of interest is reduced significantly. As the order of modulator increases, the quantization noise shifts towards the higher frequency region [5].
The noise power of L^{th} order sigma-delta modulator is given by

$$S_{Noise} = \frac{\pi^{2L}}{2L+1} * \frac{\Delta^2}{12 * OSR^{2L+1}} \quad (5)$$

From the above equation it is clear that increasing the order of the modulator reduces the noise power in the band of interest [4].

III. MODULATOR ARCHITECTURE SPACE

In the design of Sigma-Delta modulator, the design constraints are selected in the context of applications as well as the various architectural choices available. The modulator architecture presents the following choices;

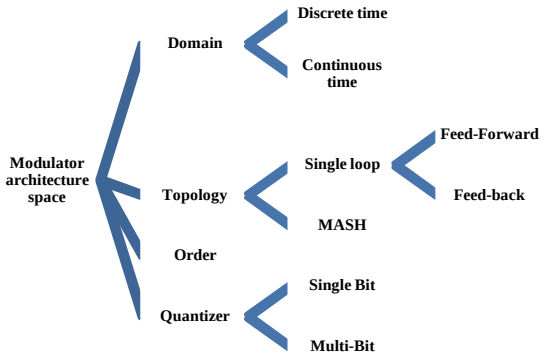

Fig.3 Modulator architecture space

3.1 DOMAIN: Based on the design of integrator circuit the sigma-delta modulator can be categorized into two domains i.e. continuous time and discrete time.

In continuous time sigma-delta modulator, the sampling is performed after the integrator and the signal is applied to comparator for the decision making. In continuous time sigma-delta modulator the analog RC integrator is used as continuous integrator. In continuous time sigma-delta modulator higher sampling frequency can be used.

Whereas in discrete domain the Switched capacitor integrator is used to perform integration operation and sampling is performed in the first stage of the input i.e. before the summer stage. Due to the limited switching of transistors sampling frequency is limited.

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3.2 TOPOLOGY:- Based on the number of stages sigma-delta modulators can be of two types:

3.2.1 SINGLE LOOP MODULATOR

In single loop sigma-delta modulator the quantization noise is shaped using integrators. As it can be observed that increasing the order of modulator (number of integrators) noise can be well shaped. But increasing the order of single loop modulator leads to instability. Hence the higher order noise shaping can be achieved in single loop modulator with stability degradation.

Figure 4 shows the basic block diagram of single loop sigma-delta modulator. In this diagram X is the analog input signal, Y digital output signal and E is the quantization error introduced from the quantizer Q. the Lsi(Z) and Lni(Z) represents the signal transfer function and noise transfer function respectively.

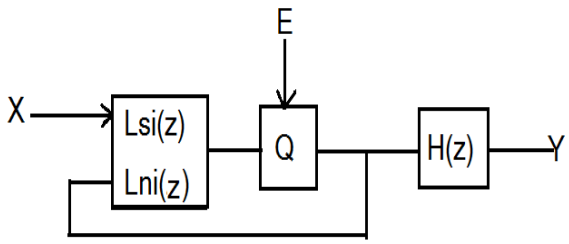

Fig. 4 Block diagram of Single loop sigma-delta modulator

For the single loop sigma-delta modulator, the output Y is given by

$$Y = STF * X + NTF * E * H \tag{6}$$

Where, STF and NTF are the signal transfer function and noise transfer function, respectively.

3.2.2MULTI STAGE NOISE SHAPING (MASH)

In order to reduce the extent of quantization noise in the output of the modulator, high order modulator with more stable operations is required. In order to get better noise shaping the order of modulator is increased by using MASH technique. In MASH (multi stage noise shaping) structure cascading of a number of low orders single loop stable modulators is done to get higher order.

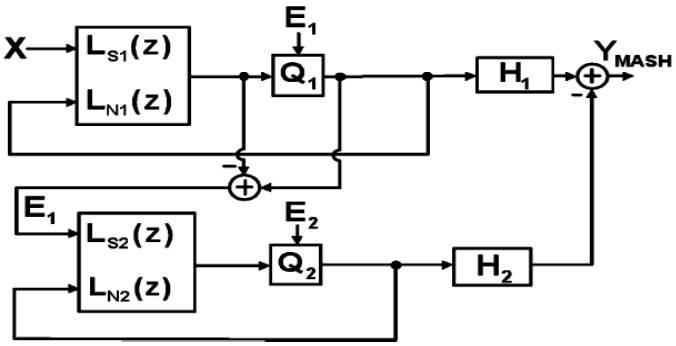

Fig. 5-stage MASH sigma-delta modulator

In MASH structure to achieve higher order of noise shaping the first stage quantization error (E_1) is fed into the input of the second loop. At the back-end of the modulator, the output of the second stage loop is subtracted from the output of the first loop via digital filters (H_1 and H_2) outside the modulator loops.

The main objective of the MASH sigma-delta modulator structure is to cancel all except the last stage quantization error by use of the digital filters at the output. For a 2-stage MASH modulator the signal and noise transfer functions can be found as

$$Y_{MASH} = STF_1 * X + (NTF_1 * H_1 - STF_2 * H_2) * E_1 + NTF_2 * H_2 * E_2 \tag{7}$$

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Where STF_1 and NTF_1 are the signal and noise transfer functions for first stage and STF_2 and NTF_2 are the signal and noise transfer functions of the second stage respectively.

From equation (7) it is observed that, to minimize the quantization error at the output of the modulator, E_1 can be cancelled and only E_2 remains to be shaped. As the quantization error E_1 can be cancelled by setting H_1 equal to the signal transfer function of the second loop and H_2 equal to the noise transfer function of the first loop. So

$$H_1=STF_2 \quad \text{and} \quad H_2= NTF_1 \tag{8}$$

By selecting the digital filters as above the error E_1 can be completely removed and only error E_2 is needed to be shaped by the overall order of the modulator.

As in MASH structure, ideally, the quantization error E_1 can be removed by designing equivalent digital filters but practically any mismatch between the analog loop filter and the digital filters will cause the residual quantization noise E_1 of the first stage. This introduces the quantization noise leakage from the first stage quantization error. This noise leakage severely deteriorates the overall performance of the modulator. In MASH structure, limited DC gain of Op-Amps is often the main source of this mismatch problem. This limitation can be overcome by using the high gain Op-Amps such as two-stage or gain boosted Op-Amps. This increases the design complexity and power consumption [7].

3.3 QUANTIZER

In sigma-delta modulator, the quantizer can be of two types based on the levels represented by quantizer. As the quantization level depends on the number of bits used to represent the signal. So the quantization step is expressed by

$$\Delta = \frac{V_{FS}}{q} = \frac{V_{FS}}{2^n} \tag{9}$$

Where, V_{FS} is the full scale voltage, q is the quantization level and n is the number of bits used in the quantizer.

$$q = 2^n \tag{10}$$

From equation 9 and 10, it is clear that increasing the number of quantizer bits increases the number of quantization levels for the fixed full scale voltage. Consequently reduces the step size of quantization, which further decrease the quantization noise as can be seen in equation 5. Based on the number of bits quantizer can be classified into two categories viz. single-bit and multi-bit quantizer.

IV. VARIANTS OF SIGMA-DELTA MODULATOR

4.1 INCREMENTAL SIGMA DELTA CONVERTERS

In the sigma-delta ADCs discussed in above sections, the sigma-delta modulators used are mainly designed for telecommunication and audio applications that do not require the high absolute accuracy. But in the context of Instrumentation, measurement and sensor applications, it is necessary to have high linearity, high absolute accuracy in sample representation and negligible offset. To achieve these requirements a special variant of sigma-delta modulator is used called Incremental or Integrating (also known as One-shot or charge-balancing sigma-delta converters).

4.1.1FIRST ORDER INCREMENTAL CONVERTER

The first order incremental ADC is the way of using the two methods with their positive approach. The two methods include the Nyquist rate Dual-Slope converter and the Sigma-Delta converter. In the incremental ADC the integration operation is performed on the applied input signal and the corresponding reference signal when they alter. But in the conventional dual slope converter, the separate integration is performed. [8].

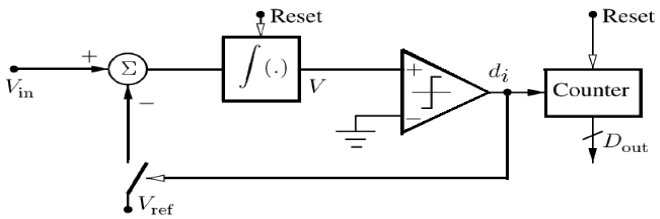

Fig.6 first order Incremental Sigma-Delta ADC

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As in the incremental ADC, the conversion is done at different rate for the input and the reference signal hence at the beginning of each new conversion, the integrators in loop and the output counter (Digital Filter) are both reset. Next, a fixed number of integration steps, i.e. equal to the total number of quantization levels, are performed. When the input to the comparator exceeds zero, its output becomes 1, and –Vref is added to the input of the analog integrator. After n steps, the output of the integrator becomes

$$V = n*Vin - N*Vref \tag{11}$$

Where N is the number of clock periods when feedback was applied. Since V must satisfy –Vref<V<Vin. It follows that

$$N = n*(\frac{Vin}{Vref}) + \varepsilon \tag{12}$$

Where ε belongs [-1, 1]. Generating N with a simple counter at the output of the modulator one can easily get the digital representation of the input signal. Note that the residual error at the output of the integrator is

$$V = -2*e_q*Vref \tag{13}$$

Where e_q belongs to $[-\Delta/2, \Delta/2]$ is the quantization error of the conversion.

The sigma-delta converter with incremental technique can be realized using simple analog and digital circuitry, needs no precision components, and can easily be extended to bipolar operation, even using only a single reference.

4.2 STURDY MASH

A stable sigma-delta modulator having well noise shaping performance with low DC gain Op-Amp can be achieved by using a different structure called sturdy MASH. In the sturdy MASH structure the combination of single loop modulator and MASH modulator is used to achieve better modulator performance. As in the single loop modulator both the quantization noise and the signal are processed inside a single loop, the single loop modulator is used to achieve the final noise transfer function. And in the MASH structure, the stability of the modulator can be obtained by sacrificing the circuit requirements.

In the Sturdy MASH (SMASH) modulator, the output of the second stage is fed back into the first loop at the first stage quantizer output in the digital domain. This in loop addition eliminates the need of digital filter and hence the requirements of the high DC gain Op-Amp that is used for digital filters auxiliary.

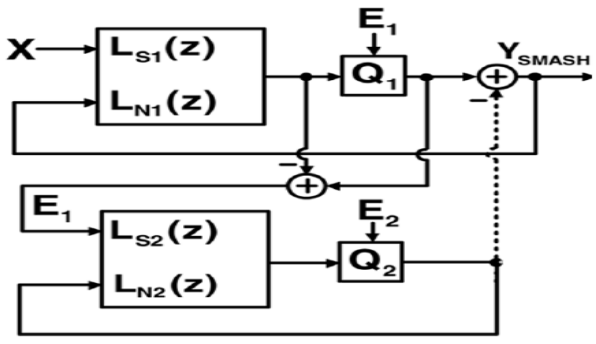

Fig. 7-stage Sturdy MASH Sigma-Delta ADC

For a 2-stage sturdy MASH sigma-delta modulator the signal and noise transfer functions are related to the output as given by

$$Y_{MASH} = STF_1X - NTF_1NTF_2E_2 + NTF_1(1-STF_2)E_1 \tag{14}$$

The above equation shows that the output of the sturdy MASH contains three terms. The first term contains the desired signal which only relies on the first loop signal transfer function. The second term contains E_2 which is shaped by the product of the first and second stage noise transfer functions. The third term which contains E_1, however, is not only shaped by the first stage noise transfer, but also multiplied by an extra term (1-STF_2). The basic idea in this

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structure is to use this extra term to match the order of noise shaping for both quantization errors. This can be done by simply choosing

$$STF_2 = 1 - NTF_2 \tag{15}$$

Hence

$$NTF_{total} = NTF_1 NTF_2 \tag{16}$$

This shows that the output of the modulator is itself the desired signal which can be directly obtained without the need of digital filters [7].

In Discrete time Sturdy MASH sigma-delta modulator the error E_1 is not eliminated unlike in MASH structure due to the mismatching of the analog and digital transfer functions. Instead E_1 is shaped by $NTF_1*(1-STF_2)$. $(1-STF_2)$ is set to NTF_2 in order to shape both E_1 and E_2 by NTF_1NTF_2 without requiring digital filters matched to analog transfer function. However the signal bandwidth of the DT-SMASH sigma-delta modulator is limited due to the inherent sampling frequency limitation of the DT implementation. In order to improve the signal bandwidth and achieve cancellation of E_1, Continuous Time (CT) SMASH sigma-delta modulator is proposed in [9].

V. DECIMATOR

In sigma-delta ADC, the second part is digital decimation filter. A decimation filter performs two operations, first is the low pass filtering and second is down sampling. The output of the modulator is applied to the decimation filter, which is the high frequency pulse density modulated signal. The decimation filter samples down the frequency to the Nyquist rate and gives a high resolution digital output [1], [3].

As in the sigma-delta modulator the incoming signal goes under the process of oversampling and noise shaping, the oversampling spreads the quantization noise to wider bandwidth than band of interest and Noise shaping shifts this noise towards the high frequency region. Hence to eliminate this high frequency quantization noise a digital low pass filter is used. Also the incoming signal is a high frequency signal, to bring it to the Nyquist rate a down sampling operation is done [1].

A digital decimation filtering operation is represented by summation of all the samples and division by the sampling factor [10]. The sampling factor is equal to oversampling ration used for the sampling of the input signal

.

$$H(z) = \frac{(1 + z^{-1} + z^{-2} + \ldots + z^{1-D})}{D} \tag{17}$$

$$H(z) = \frac{1}{D}\sum_{n=0}^{D-1} z^{-n} \tag{18}$$

In practice, decimation is done in multiple stages by cascading several smaller decimation factors, such that the overall decimation factor equals the product of decimation factors of the individual decimation stages. One big advantage of multistage filtering is the power reduction made possible by making the subsequent components operate at lower sampling rates. The power reduction, along with reduction in number of filter tabs makes a multistage approach more desirable [10].

As in the design of decimation filter addition and multiplications are performed. To avoid the need of D-1 summation and multiplication decimation is performed using cascaded integrator comb (CIC) filter. A CIC filter is typically a combination of an integrator (I) and a subtractor (comb section)(C) [10]. Before the signal is sent to a Comb filter, it is decimated (down sampled) by a factor of M. Then the down-sampled data is passed to the Comb section.

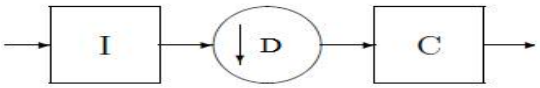

Fig. 8 Basic Diagram of CIC filter

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VI. PERFORMANCE MEASURES

A large set of specifications are used to characterize the performance of sigma-delta converters. These give general information and describe the features and limits of the modulator. The most popular specifications and its technical terms are explained as follows.

1. OVERSAMPLING RATIO (OSR)**:** In signal processing, oversampling is the process of sampling a signal with a sampling frequency (f_s) significantly higher than twice the signal bandwidth (f_b). Oversampling helps avoid aliasing, improves resolution and reduces noise but increases the consumed power of the modulator. The oversampling ratio is defined as

$$OSR = \frac{f_s}{2 * f_b} \tag{19}$$

2. SIGNAL-TO-NOISE-RATIO (SNR): The SNR defines how much a signal has been corrupted by noise. The SNR is defined as the power ratio between the signal and the total noise produced by quantization and the noise of the circuit. The SNR accounts for the noise in the entire Nyquist interval. Moreover the SNR can depend on the frequency of the input signal and it decreases proportional to the input amplitude. Because many signals have a very wide dynamic range, the SNR is often expressed using the decibel scale (dB) and defined by

$$SNR_{|dB} = 10 * \log(\frac{p_{sign}}{p_{noise}}) \tag{20}$$

Where p_{sign} and p_{noise} are the power of the signal and the power of the noise in the band of interest.

3. SIGNAL-TO-NOISE-AND-DISTORTION-RATIO (SNDR OR SINAD).It is similar in definition to the SNR however, non-linear distortion terms, produced by the input signal, are also included. The SNDR is defined as the ratio between the root-mean-square (rms) of the signal and the root-sum-square (rss) of harmonics components plus noise, but excluding the DC component. The SNDR is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion. This parameter is often plotted for various input amplitudes and frequencies. It is usually given in dB

4. SPURIOUS-FREE-DYNAMIC-RANGE (SFDR)**:**It is the ratio between the rms of the signal and the rms of the highest spurious spectral component in the first Nyquist Zone. With large input signals the highest (or worst) component is given by one of the harmonics of the signal. Quoted in dB, the SFDR is an important specification in communications systems because it represents the smallest value of signal that can be distinguished from a large interfering signal.

5. EFFECTIVE-NUMBER-OF-BITS (ENOB)**:**This parameter measures the SNDR (or SINAD) using bits. An often used definition for ENoB, where the SNDR is expressed in dB, is

$$ENoB = \frac{SNDR_{|dB} - 1.76}{6.02} \tag{21}$$

6. DYNAMIC-RANGE (DR)**:**Typically expressed in dB, dynamic range is the value of the input signal at which the SNR or SNDR is 0 dB. The DR specification is useful for sigma-delta architectures that do not obtain their maximum SNR or SNDR at full-scale input amplitude (0 dBFS).

$$DR = 20 \log(\frac{S_{\max}}{S_{\min}}) \tag{22}$$

Where S_{max} is the max signal power that can be measured and S_{min} is the minimum signal that can be sensed by modulator.

7. FIGURE-OF-MERIT (FOM)**:**This parameter establishes the power effectiveness of Modulator. The FoM is expressed in Joules-by-conversion-level (J/convlevel) and is given by

$$FoM = \frac{Pw}{2^{ENoB}.BW} \tag{23}$$

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Where Pw is the total power consumption of the modulator, BW is the bandwidth of the input signal and ENOB is the effective number of bits described before. An effective solution shows a FoM lower than 500 fJ/conv-level. The figure of merit depends on the architecture of the modulator and the line-width of the technology. Moreover, there are several definitions of the FoM. In some cases the dynamic range is used instead of ENoB [11].

VII CONCLUSION

From the study of sigma-delta ADC presented in this paper, it is concluded that various applications requires sigma-delta ADCs with different specifications. The single loop sigma-delta modulator is best suited for audio and Tele-communication applications with low resolution. High accuracy, low power sigma-delta ADCs is required for sensor applications and for portable devices. High absolute accuracy and low offset error achieved with incremental sigma-delta ADC is good for instrumentation and measurement applications. Applications requiring very low voltage and high resolution can be realized by using sturdy-MASH ADCs.

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BIOGRAPHY

Sagar Chetani received the Bachelor of Engineering degree in Electronics and Tele-communication engineering from Government Engineering College, Bilaspur in 2012. During 2012-2013, served as a lecturer in Government Engineering College, Bilaspur. Currently, he is enrolled in Mtech program in Electronics and Tele-communication with Digital Electronics specialization in Chouksey Engineering college, Bilaspur, Chhattisgarh.

Jagveer Verma received the B.E degree from M.I.E.T Gondia in 2000 and M.E degree from S.S.G.M.C.E Shegaon Maharashtra in 2006.During the M.E he was the winner of Cadence design contest in VLSI Design.After completion of M.E he worked as a research associate at SGIARC research centre for one year .He is having total teaching experience of 9 years and industrial experience of 2 years. His research interest includes Analog and Digital CMOS design .He joined as a lecturer in DIMAT in 2007 and presently working as a assistant professor in Chouksey Engineering College, Bilaspur (C.G).

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