



# **Leakage Power Reduction in Domino Logic Circuits At 45 Nm Technology**

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**ABSTRACT:** Technology advancement means reduction in circuit size, as well as reduction in supply voltage, threshold voltage, gate oxide thickness and also in several other factors, but the drawback of scaling is, the leakage in device has increased. Considering this factor, it can be summarized that after few generations the leakage power dissipation will equal to the active power dissipation. Hence, efficient leakage power reduction techniques are very important for the deep-submicron and nano-meter circuits. In this paper, a technique based on the use of dual-threshold has been used for leakage reduction in lector based footed diode domino logic circuit, in which a high threshold nmos transistor has been inserted at the dynamic node of lector based domino logic circuits. By using the proposed technique, leakage and power delay product has been reduced to a substantial amount as compared to lector based domino logic circuits.

**KEYWORDS:** Leakage, Delay, Deep submicron, Domino Logic, Power optimization, Sub-threshold Leakage, Transistor Stacking.

## **I. INTRODUCTION**

Power dissipation is an important factor of consideration while designing of CMOS VLSI circuits. High power consumption results in reduction in the battery life in the case of battery-powered applications and also affects the reliability, cooling costs and packaging cost of the circuit. There are mainly three sources of power dissipation in digital electronics. i.e.: 1) capacitive power dissipation which is due to the charging and discharging of the load capacitance; 2) short-circuit currents due to the existence of a conducting path between the voltage supply and ground for the brief period during which a logic gate makes a transition; and 3) leakage current, which is of two types i.e. sub-threshold leakage and gate leakage. The gate oxide leakage current is due to the stored charge between the drain and bulk of active transistors while the sub-threshold leakage current is due to the carrier diffusion between the source and drain of the transistors, which are off. IC power dissipation consists of different components depending on the circuit operating modes. First, the switching or dynamic power component dominates during the active mode of operation. Second, there are two primary leakage sources, the active component and the standby leakage component. The standby leakage may be made significantly smaller than the active leakage by changing the body bias conditions or by power-gating. The paper is organized as follows: Section 2 gives brief explanation about leakage current and sources of power dissipation. Section 3 compares the conventional domino logic circuit and lector based domino logic circuit. Simulation results are given in Section 4 followed by the conclusion in Section 5.

## **II. LEAKAGE CURRENT CHARACTERISTICS IN DOMINO LOGIC CIRCUITS**

When a low input signal is applied to any circuit, it must produce low output but that's the idle case. Practically there are some distortions, which is because of the negligible current flowing in the wires of circuit, that current is called as leakage current. There are four main sources of leakage current in a CMOS transistor namely (a) Reverse-biased junction leakage current (IREV): occurs from the source or drain to the substrate through the reverse biased diodes when a transistor is off, (b) Gate induced drain leakage (IGIDL): caused by high field effect in the drain junction of MOS transistors, (c) Gate direct-tunnelling leakage (IG): flows from the gate through the "leaky" oxide insulation to the substrate and (d) Sub-threshold (weak inversion) leakage (ISUB): is the drain-source current of a transistor operating in the weak inversion region. Out of these, sub-threshold leakage current is expected to be most dominant leakage current because it increases exponentially at reduced threshold voltage. Thus the techniques which aim at lowering leakage current are highly desirable.

### III. LEAKAGE POWER REDUCTION TECHNIQUES IN DOMINO LOGIC CIRCUITS

The leakage power reduction techniques in domino logic circuit are explored in this section. The main techniques for leakage reduction which are compared in this paper are conventional footer less domino logic circuit, lector based footed diode domino logic circuit and sleep switch based domino logic circuit.

#### 3.1 Conventional Footerless Domino Logic Circuit

Circuit diagram of conventional 2-Bit OR gate implemented using domino logic circuit has been shown in Fig. 3.1. In this circuit pull up network of cmos based design has been replaced with a single pmos and a keeper transistor has been inserted in parallel with this pull up transistor, gate of this keeper transistor is controlled by output signal of inverter. This circuit will operate in two phases i.e. Precharge phase, and an evaluation phase.

- (a) Precharge Phase: During this phase of operation the clock signal will be low, so the dynamic node will be high, that will result in low output for any combination of input signal.
- (b) Evaluation Phase: During this phase of operation the clock signal will be high, so the charging and discharging of dynamic node will depend upon the input combination applied, and according to the applied input combination the output node will be low or high. The sub-threshold leakage current and gate oxide leakage current will also depend on the input vectors applied.

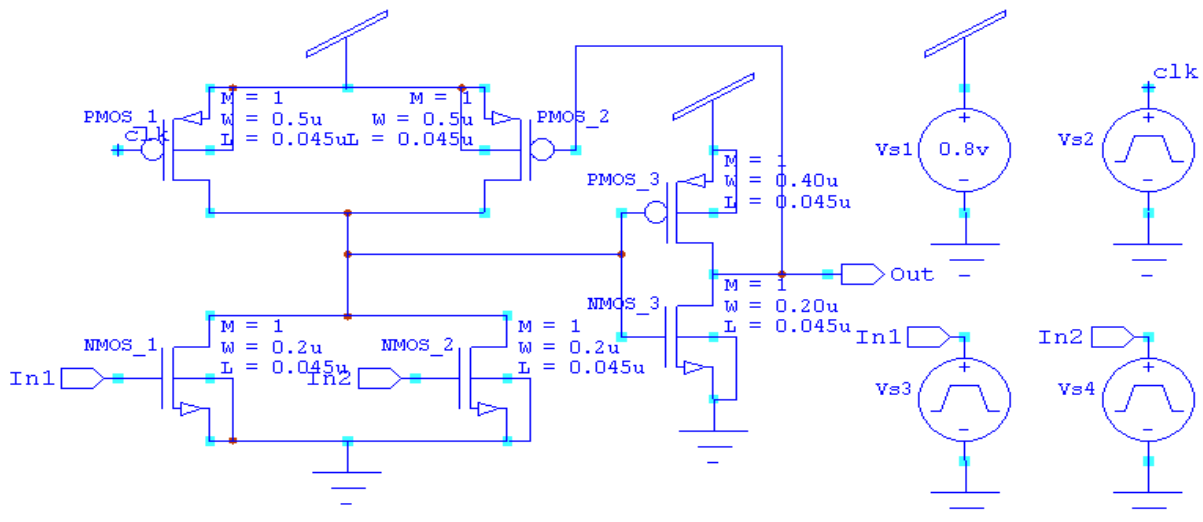


Fig. 3.1: Schematic Capture of Conventional OR Gate

#### 3.2 Lector Based Domino Logic Circuit

This technology is a combination of several technologies in which concept of transistor stacking, concept of keeper transistor and concept of footed diode have been utilized. Stacking means to increase the number of transistor in between  $V_{DD}$  and GND. Because of that resistance between supply and GND path will increase. Increased resistance results in reduced leakage. A keeper transistor is inserted in parallel to pull up network to maintain the state of dynamic node against several problems such as charge sharing, coupling noise and sub-threshold leakage, size of keeper transistor is kept smaller as compared to pull down network in order to minimize the power and delay degradation caused by keeper contention current. Footed diode is added because it has better timing characteristics because of isolation of pull-down network. In this technology two leakage control transistors are inserted in between the pull up network and pull down network. The transistors are connected in such a manner that gate of one transistor is controlled by source of another transistor. Such type of combination of transistor is called Lector. This combination of transistor ensures that one of the LCT will always operate in cut-off region, which results in increased resistance between supply voltage and ground. So the leakage of the critical path will decrease but the delay and area will increase, so there is no

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considerable effect on power delay product, which is main concern in low power VLSI design. This circuit provides less leakage and increased delay when compared with conventional domino logic based 2-bit OR gate. Circuit design of 2-bit OR gate designed using lector based domino logic has been shown in fig. 3.2.

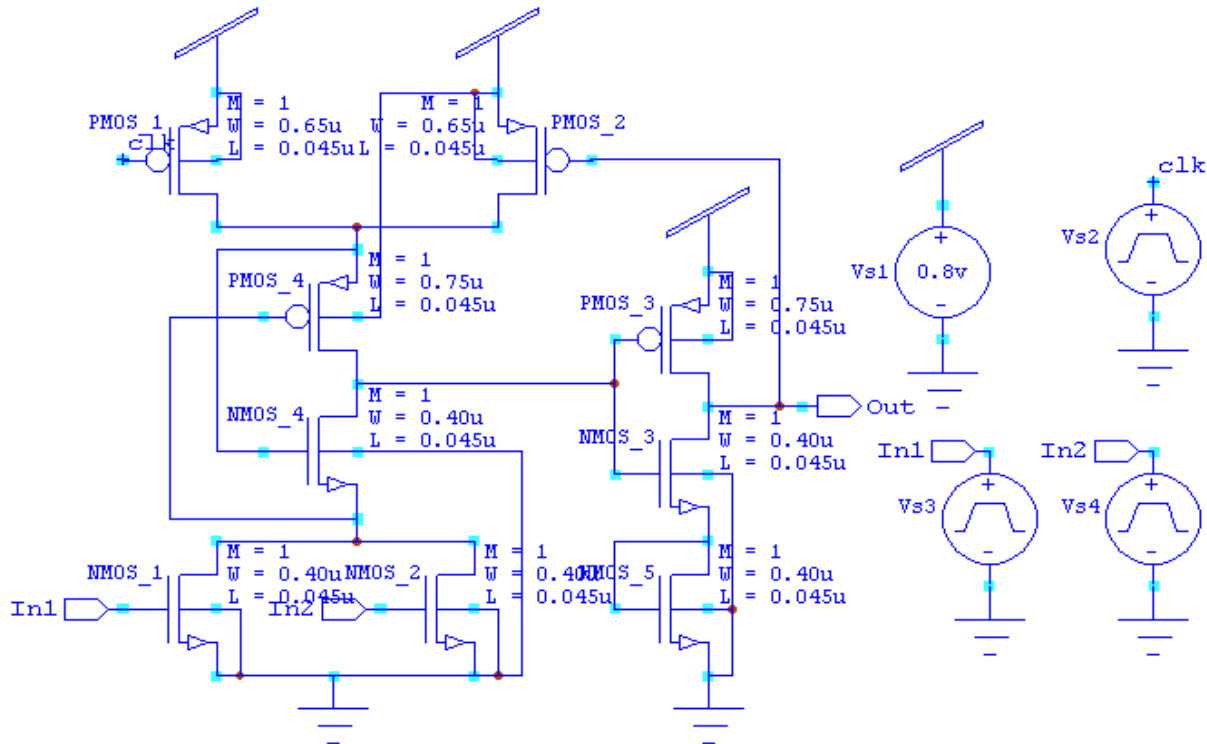
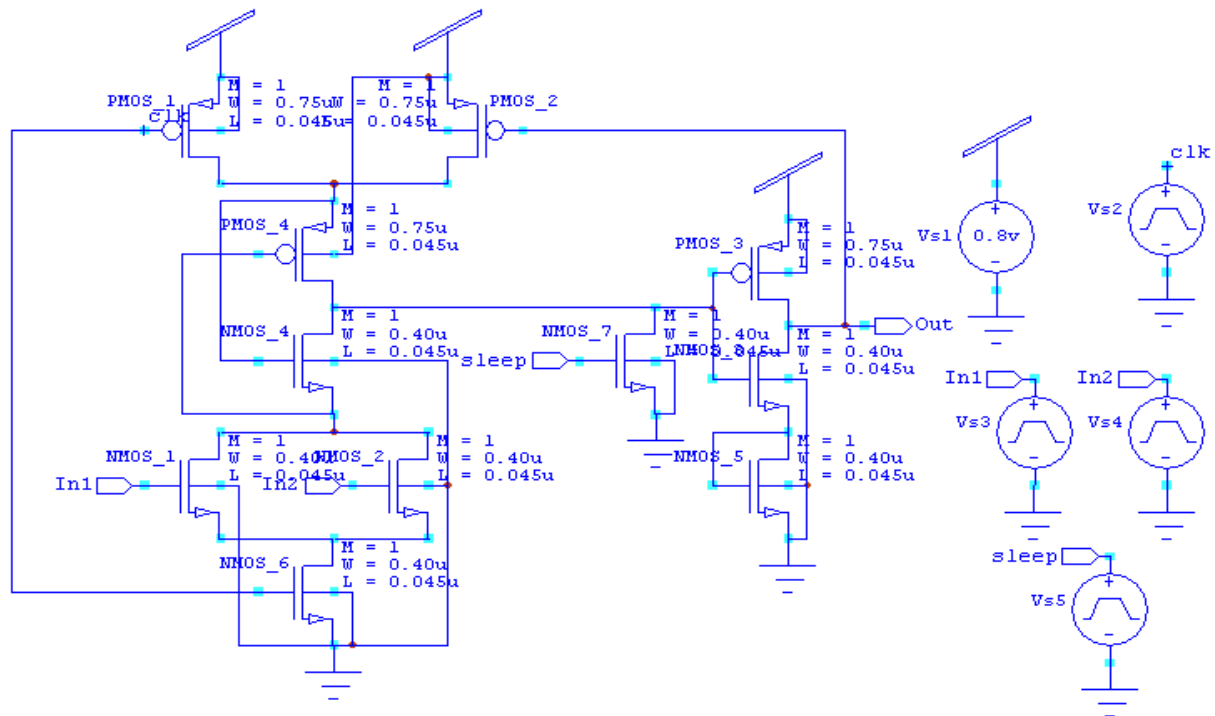


Fig. 3.2: Schematic Capture of Lector Based Footed Diode Domino Logic OR Gate

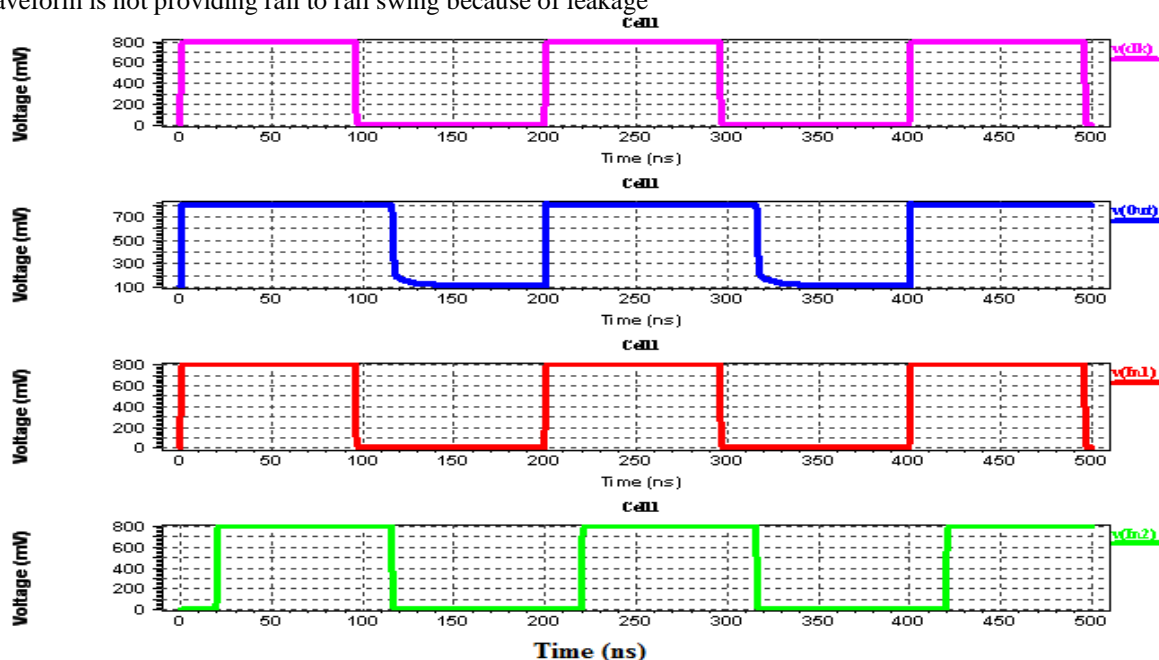
### 3.3 Sleep Switch Dual Threshold Voltage Domino Logic Based Approach

In this approach of leakage control, a sleep switch dual threshold voltage domino logic technique has been utilized for further reduction in leakage of lector based circuit so that overall power delay product of circuit can be reduced, for which high-threshold transistors have been employed in non-critical precharge paths, and low-threshold transistors are used in evaluation path, which is speed critical high-threshold path. In this technique one NMOS is inserted at the dynamic node of circuit, which is controlled by a separate sleep signal, and a high threshold transistor has been inserted at the bottom of the circuit, which is controlled by a clock signal. If sleep signal is low, the high-threshold sleep transistor will be off and the circuit will work as normal lector based circuit but if high voltage input signal is provide to sleep transistor, then the high threshold NMOS will be ON. Therefore, dynamic node of circuit will discharge through the sleep switch and will provide leakage reduction in domino logic based circuit. This proposed technique provides sufficient reduction in leakage, but the overall delay of the circuit is almost constant, therefore the proposed technique is providing considerable reduction in power delay product. Major advantage of used technique is that it does not provide trade-off in between leakage and delay. This technique employees sleep switches and a dual threshold voltage CMOS technology in order to place an idle domino logic circuit into a low leakage state, as shown in Fig. 3.3.



**Fig. 3.3: Schematic Capture of Sleep Switch Based 2-Bit OR Gate**

Output waveforms for proposed sleep switch based 2-bit OR gate circuit has been shown in Fig. 3.4, from waveforms. From diagram, it is clear that the proposed technique is providing output waveform similar to conventional 2-bit OR gate. It means output will be high for any input combination other than the both low inputs. The resultant output waveform is not providing rail to rail swing because of leakage



**Fig. 3.4: Output Waveform of Sleep Switch Based 2-Bit OR Gate**



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## IV. SIMULATION RESULTS

TANNER EDA tool has been used for circuit designing and analysing. BISM device model is used for simulation of conventional domino logic circuit, lector based domino logic circuit and sleep switch based domino logic circuit for accurate estimation of sub-threshold leakage. The circuits are designed using S-EDIT tool, simulated T-EDIT tool and waveform are obtained using W-EDIT toll, for simulating circuit, 45nm CMOS technology and supply voltage of 0.8V has been used. Table 3.1 is showing the result comparison for 2-Bit OR gate implement by using the above explained techniques. In this table comparison is done on the basis of several parameters such as power consumption, delay, and power delay product.

Table 3.1: Comparison Table for 2-bit OR gate

Circuit Design	Active Power Consumption	Delay of Circuit	Leakage Current	Leakage Power	Power Delay Product
Standard. 2-bit OR gate	$1.024 \times 10^{-6}$	$1.154 \times 10^{-7}$	$3.015 \times 10^{-8}$	$2.412 \times 10^{-8}$	$2.78344 \times 10^{-16}$
Lector based 2-bit OR gate	$3.52 \times 10^{-7}$	$1.16 \times 10^{-7}$	$2.703 \times 10^{-8}$	$2.2024 \times 10^{-8}$	$2.572 \times 10^{-16}$
Reduction	24.1% reduction	Approx Similar	11.5% reduction	10%	23.52%
Modified 2-bit OR gate	$9.9765 \times 10^{-8}$	$0.973 \times 10^{-7}$	$2.66 \times 10^{-8}$	$2.1296 \times 10^{-8}$	$2.072 \times 10^{-15}$
Reduction as compared to Lector based circuit	17.64%	16.1%	1.09%	3.805%	7.18%

## V. CONCLUSION

In 45-nm technology both sub-threshold leakage current and gate leakage current must be reduced to reduce leakage power consumption in idle mode of operation. Therefore a technology based on sleep switch logic has been proposed to reduce leakage power. It is concluded that there is a sufficient reduction in leakage of the circuit. After result analysis, it is found that there is reduction of 3.08% and 7.18% in leakage and power delay product respectively by using sleep switch based approach. Thus sleep switch based is an appropriate technique to reduce leakage power with respect to constant delay and therefore reduces power delay product.

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## **BIOGRAPHY**



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