ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 4, April 2016

Power Quality Improvement in Multi-Level Inverters with Reduced Number of Switches

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ABSTRACT: Now a days renewable energy systems become a major role of the modern power systems and to connect the main grid, a power inverter is needed. Poor power quality and harmonic distortions are main problem in power system applications and overcome these problems need a power inverter based power electronics devices. There are two major topologies namely conventional two-level and multi-level topology. The modular multilevel converter (MMC) is one of the recent technique in multi-level topologies these requires no need for snubber circuits and can deliver both active and reactive power it is an ideal choice for our applications. In MMC number of switches, capacitors will more to rectify these parameters by using Proposed MLI with fewer number of switches and diodes, reducing gate driver circuit for those switches. In this paper SPWM technique uses multicarrier waveforms with level shifting ensuring the reduction in total harmonics distortion (THD) and improve power quality.The proposed model is done by using MATLAB Simulink software.

KEYWORDS: Modular multilevel converter (MMC), proposed inverter, Level shifting SPWM, PD, POD, APOD, Total Harmonics Distortion (THD) and Power quality.

I.INTRODUCTION

Recently Multi-level Inverters (MLI) have large interest in medium voltage and high power applications. The arrangement of multilevel voltage source inverters (VSI) allows high voltages and low harmonics without using the series connected switching devices or transformers or filters [1]-[2]. Now a days, voltage source multilevel inverters have received for industries and researchers, because they are handling high voltage with low stress on switching devices, to generate output voltage with minimum harmonic distortion, and generate low dv/dt, which results in reduced stress on different type of applications [1]-[3]. The most common types of multilevel inverters are:

- Diode clamped multilevel inverter
- Capacitor clamped multilevel inverter
- Cascaded multilevel inverter

Diode clamped multilevel inverter is the most accepted topology in industry for a medium voltage applications such as medium voltage drive systems. However, they suffer from the problem of voltage imbalance of the first two methods [2]-[7]. The problem becomes more complex with increased number of levels. In diode-clamped and capacitor clamped inverters are suffer from the problem of voltage imbalance of the clamping diode and capacitors we have to modify this problem by using cascaded H-bridge inverter or Proposed inverter [3]-[5].

Recently, modular multilevel inverter topology have been reported as an alternative to conventional multilevel inverters in medium to high voltage applications [12]-[13]. It is able to overcome most difficulties of conventional multilevel inverter and provides new set of features such:

- Modular construction
- No need for snubber circuits
- Requires only one dc source
- Can deliver both active and reactive power
- It is extendable to any number of levels and capacitors voltage balance is attainable.

Since, there are some similarities between the modular multilevel inverter and proposed inverter in their structures, operational principles and pulse width modulation techniques [10]-[14]. But proposed topology is to reduce the number of switching devices, voltage stress on switches and modular MLI reduce THD and improve power quality. Therefore, detail comparisons between modular multilevel MLI and Proposed inverter are investigated in this paper [12].

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 4, April 2016

II.REVIEW OF MODULAR MULTILEVEL INVERTERAND PROPOSED TOPOLOGY

A. Modular multilevel inverter (MMC)

MMC is a converter system comprised of arbitrary numbers of identical half-bridge (HB) sub-modules(SMs). Each SM is a two-terminal device, considered a controllable voltage source, consisting of two switches working in a complementary manner and a local DC-storage capacitor [12]-[15]. Generally, an n-level single-phase MMC inverter consists of (n-1) a series connection of basic SMs, two buffer inductors, and two DC capacitors which translates to 2(n-1) switches and (n-1) SM capacitors, in addition to two inductors and two DC link capacitors [13].

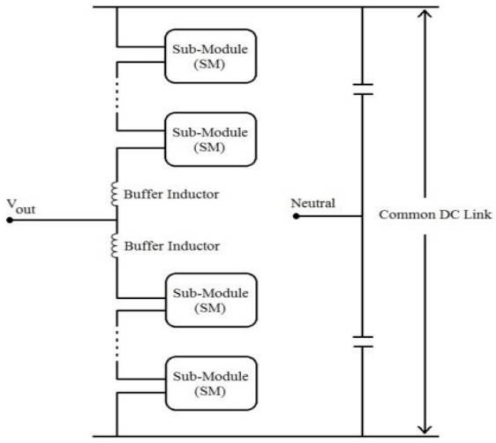

Fig.1 Schematic diagram of Modular Multi-level converter

Buffer inductors must provide current control in each phase arm and limit the fault currents. The output voltage of each SM (Vo) is either equal to its capacitor voltage (Vc) or zero, depending on the switching states. In this structure, two sub-modules (SM) are connected upper and lower arms of the leg. Fig.1 Schematic diagram of Modular Multilevel converter [11]-[14].The configuration of a Sub-Module (SM) is given in Fig.2 Each SM is a simple chopper cell composed of two IGBT switches (*T1* and *T2*), two anti-parallel diodes (*D1* and *D2*) and a capacitor [9]-[10].

With reference to the SM shown in Fig.3

Uo = Uc if *T1* is *ON* and *T2* is *OFF*

Uo = 0 if *T1* is *OFF* and *T2* is *ON*

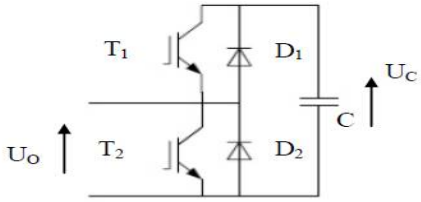

Fig.2 Sub-Module of half-bridge inverter

The equivalent circuits of all four modes are shown in Fig.3. The output current depends on load like R or RL [9].

Mode 1: During this mode the switches T_1 is OFF and T_2 is ON. The output voltage is zero i.e. load is short circuited.

$$Uo = 0 \quad \text{- - - - - - - - -} \quad (1)$$

Mode 2: During this mode the switch T_1 is ON and T_2 is OFF. The output voltage is equals to the input voltage (Uc) i.e. load is connected across source directly. And load current flows through Uc- T_1-load-Uc.

$$Uo = Uc \quad \text{- - - - - - - - -} \quad (2)$$

ISSN (Print) : 2320 – 3765
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International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 4, April 2016

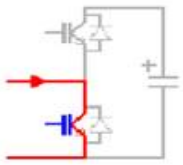


Fig. 3(a): MODE 1

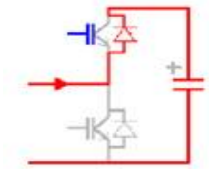


Fig. 3(b): MODE 2

Mode 3: Mode 1 and Mode 3 are same only the switching sequence is different. During this mode the switches T_1 is OFFand T_2 is ON at negative direction. The output voltage is zero i.e. load is short circuited.

Mode 4: During this mode the switch T_1 is ON and T_2 is OFF. The output voltage equals to the negative of input voltage (-Uc) i.e. load is connected across source directly. And the load current flows through Uc – T_1- Load-Uc.

$$Uo = -Uc \quad \text{- - - - - - - - -} \quad (3)$$

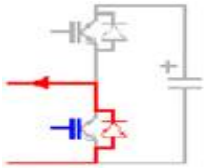


Fig. 3(c): MODE 3

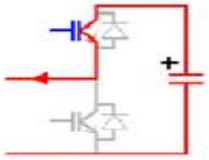


Fig. 3(d): MODE 4

Fig.3 shows the current flows in both useful states. Table.1 Shows switching states for each SM of MMC topology. In a MMC the number of steps of the output voltage is related to the number of series connected SMs [6]-[9].

Table1. Switching states for each SM of MMC topology

Mode	T_1	T_2	U_o
1	1	0	U_c
2	0	1	0

B. Proposed Topology

The proposed MLI is designed for 9-level using 7 switches as shown below in Fig.4. This topology is modified conventional H-bridge inverter where number of levels can be increased by little number of diodes, switches and voltage sources [10]. Switches S1, S5, S6 and S7 represent H-bridge in which S1, S5 are used for generating negative voltage levels whereas S6, S7 are used for generating positive voltage levels. In addition switches S2, S3 and S4 are used to increase the number of levels. The proposed method 9-level inverter requires 7-switches, 3-diodes and 4-voltage sources [10]-[12]. Fig.5 Shows circuit diagram of N-level proposed MLI.

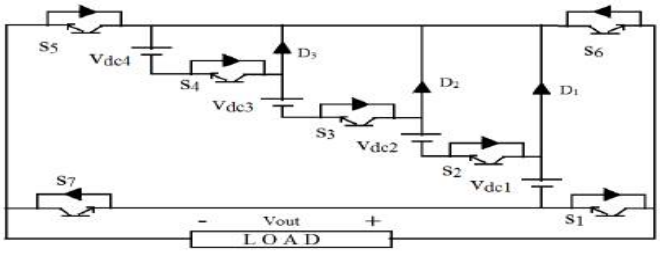


Fig.4 Circuit diagram of proposed 9- level MLI

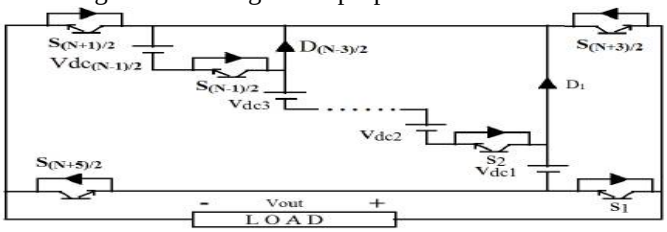


Fig.5 N-level proposed MLI

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 4, April 2016

The relationship between number of output levels, switches, diodes and voltage sources is stated in Table.2.

Table.2 Relationship between numbers of output levels, Switches, diodes and voltage sources

No. of levels	No. of switches	No. of clamping diodes	No. of sources
3	4	0	1
5	5	1	2
7	6	2	3
9	7	3	4
N	(N+5)/2	(N-3)/2	(N-1)/2

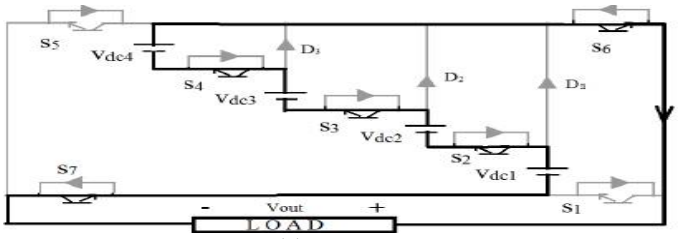
III. OPERATION OF PROPOSED TOPOLOGY

The operation for 9-level MLI with 7-switches as shown in Fig. 4 is discussed above. Switches S1 and S5, S6 and S7 are complementary to each other. S1, S5 are turned ON to generate negative output levels and S6, S7 are turned ON to generate positive output levels [2]-[6].

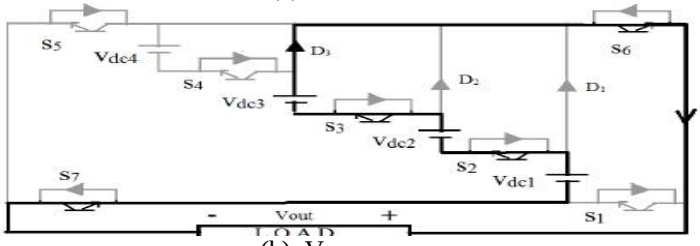
Table.3 Switching states with corresponding voltage levels

Voltage levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7
$V_{1 = 4Vdc}$	0	1	1	1	0	0	1
$V_{2 = 3Vdc}$	0	1	1	0	0	1	1
$V_{3 = 2Vdc}$	0	1	0	0	0	1	1
$V_{4 = Vdc}$	0	0	0	0	0	1	1
$V_{5 = 0}$	0	0	0	0	0	0	0
$V_{6 = -Vdc}$	1	0	0	0	1	0	0
$V_{7 = -2Vdc}$	1	1	0	0	1	0	0
$V_{8 = -3Vdc}$	1	1	1	0	1	0	0
$V_{9 = -4Vdc}$	1	1	1	1	1	0	0

Switches S2, S3, and S4 are turned ON when maximum positive and negative output level is required and turned OFF with corresponding levels as shown in Table.3. The current flow direction through the circuit for positive and negative voltage levels as shown in Fig.6 (a)-(d) and Fig.7 (a)-(d) respectively.



(a). $V_{1 = 4Vdc}$



(b). $V_{2 = 3Vdc}$

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

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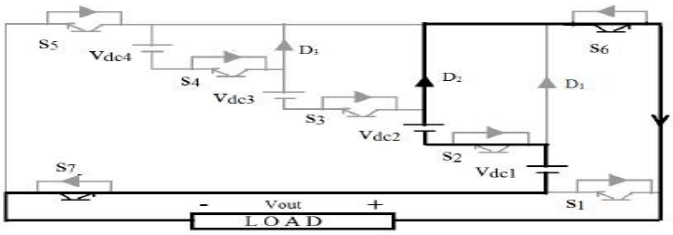
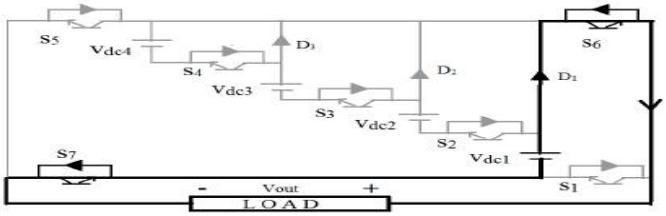
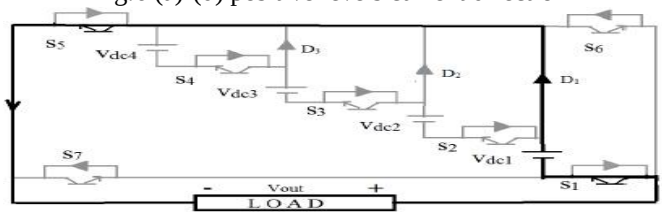


(c). $V_{3 = 2Vdc}$

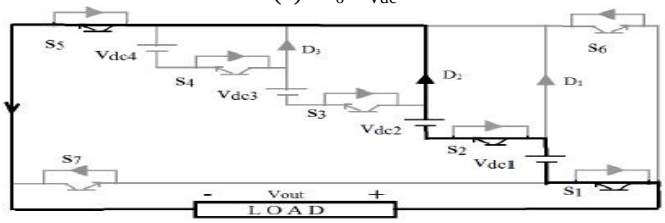


(d). $V_{4 = Vdc}$

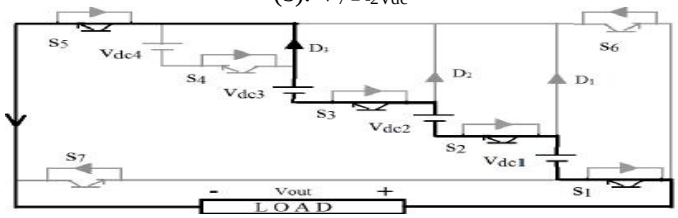
Fig.6 (a)-(d) positive levels current direction



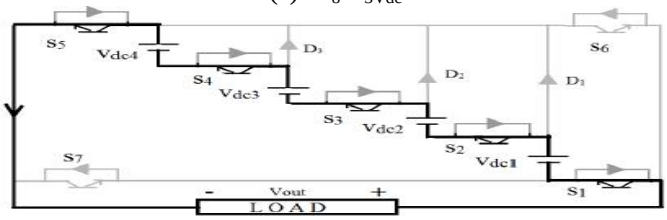
(a). $V_{6 = -Vdc}$



(b). $V_{7 = -2Vdc}$



(c). $V_{8 = -3Vdc}$



(d). $V_{9 = -4Vdc}$

Fig.7 (a)-(d) Negative levels current direction

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 4, April 2016

IV. SPWM TECHNIQUE FOR PROPOSED TOPOLOGY

Sinusoidal pulse width modulation (SPWM) technique is used for pulse generation where reference wave is sinusoidal and carrier wave is triangular wave. In this paper PD, POD and APOD has been used for the pulse generation for the proposed MLI. Fig.8, 9 and 10 shows PD, POD and APOD of SPWM for 9-level proposed MLI respectively.

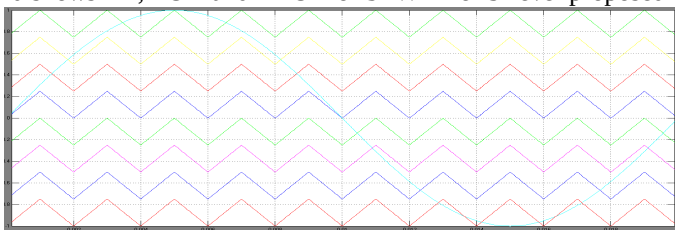


Fig.8 Phase Disposition (PD) with SPWM

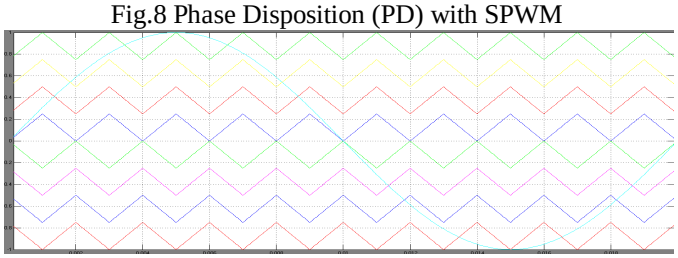


Fig.9 Phase Opposition Disposition (POD) with SPWM

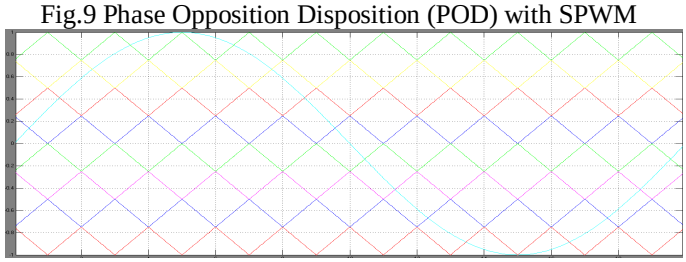


Fig.**10** Alternate Phase Opposition Disposition (APOD) with SPWM

V. SIMULATION RESULTS

The proposed MLI has been designed 9-level output voltage using 7-switches. In this circuit mainly four input voltage sources are used and each voltage source is equal to 10V. The simulation has been performed in MATLAB/SIMULINK. Fig.11 Simulation of Modular Multilevel Converter and 9-level voltage total harmonic distortions (THD) for a output waveform are shown in Fig.12, 13 and 14 respectively.

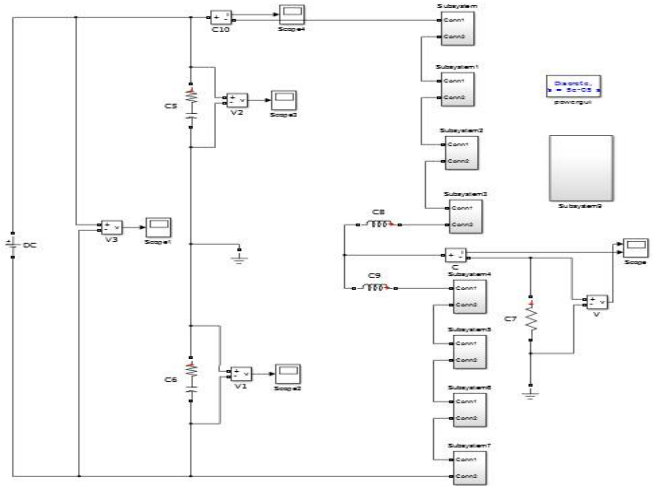


Fig.11 Simulation of Modular Multilevel Converter

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ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

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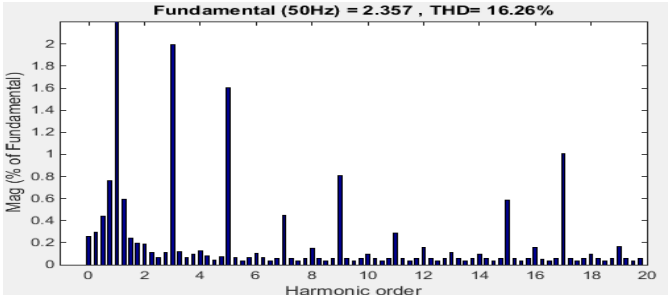

Fig.12 THD of Modular Multilevel Converter with PD

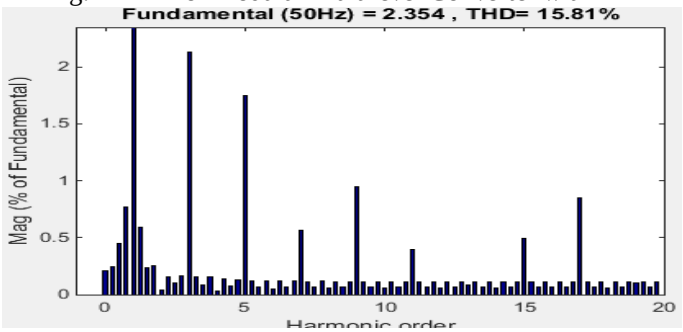

Fig.13 THD of Modular Multilevel Converter with POD

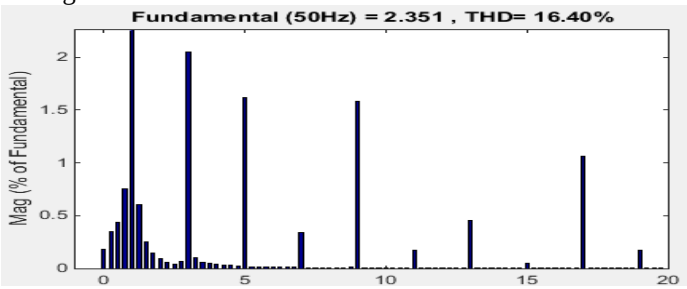

Fig.14 THD of Modular Multilevel Converter with APOD

The switching pulse generation for switches S1 and S5, S2, S3, S4, S6 and S7 has been shown in Fig.15 to Fig.19 respectively. 9-level output voltage and output current waveform are shown in Fig.20. 9-level voltage total harmonic distortions (THD) for a output waveform are shown in Fig.21, 22 and 23 respectively.

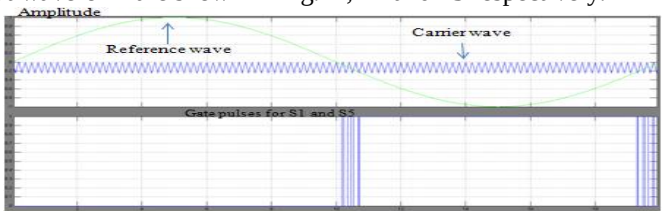

Fig.15 Pulse generation for switch S1 and S5

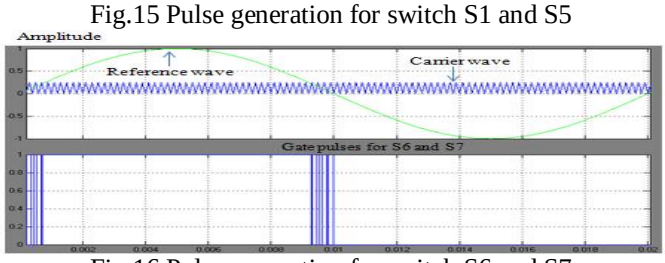

Fig.16 Pulse generation for switch S6 and S7

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ISSN (Online): 2278 – 8875

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(An ISO 3297: 2007 Certified Organization)

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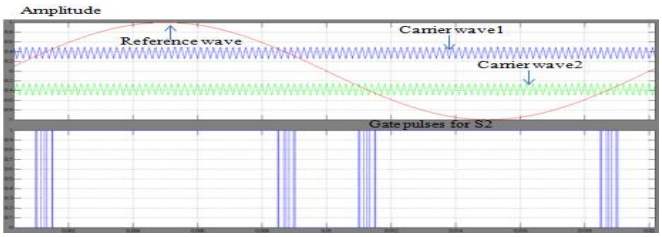

Fig.17 Pulse generation for switch S2

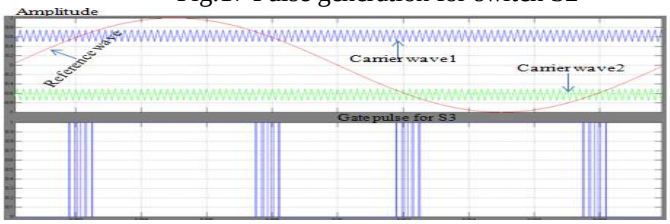

Fig.18 Pulse generation for switch S3

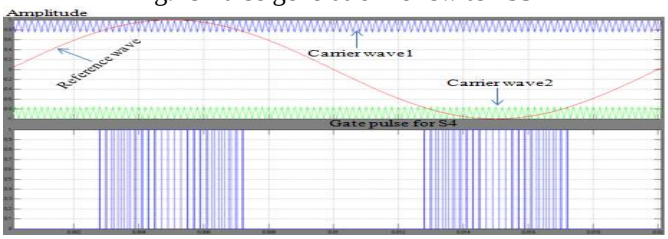

Fig.19 Pulse generation for switch S4

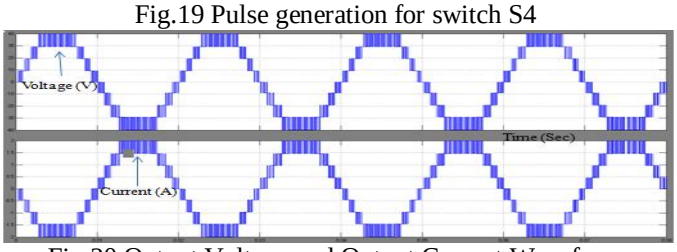

Fig.20 Output Voltage and Output Current Waveform

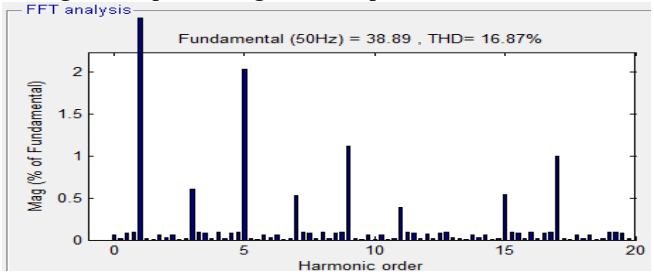

Fig.21 THD of proposed topology with PD

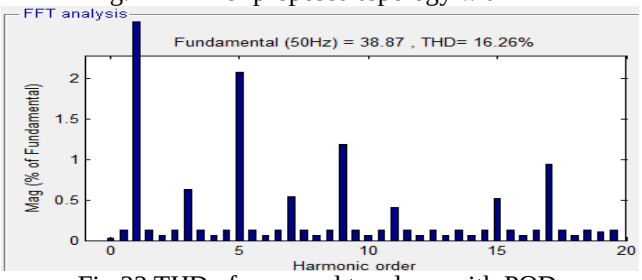

Fig.22 THD of proposed topology with POD

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

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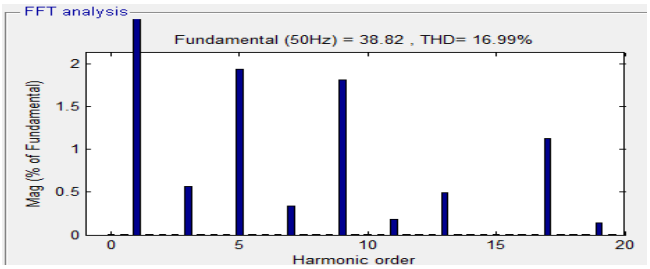

Fig.23 THD of proposed topology with APOD

VI. COMPARISON OF MODULAR MULTILEVEL CONVERTER AND PROPOSED MLI

Modular MLI required only one DC source and more number of switches. Later the above discussed drawback is overcome by modifying proposed MLI. Table.4 shows the comparison between Modular MLI and proposed MLI voltage harmonic distortion with PD, POD and APOD.

Table.4 Comparison between Modular MLI and Proposed MLI

Parameter	Modular MLI	**Proposed MLI**
Level	9	**9**
Switches	16	**7**
Diodes	0	**3**
Voltage sources	1	**4**
PD	16.26%	**16.87%**
POD	15.81%	**16.26%**
APOD	16.40%	**16.99%**

VII. CONCLUSION

In this paper, discusses several issues concerning modular multilevel inverters and proposed inverter. The proposed MLI advantages include fewer number of switches which in turn reduced the corresponding gate driving circuitry, made the circuit compact in size. The modular multilevel converter (MMC) requires only one DC source and it can deliver both active and reactive power, it is an ideal choice for our applications. The proposed and MMC inverter is transfer both active and reactive power, but is able to control the power factor. Comparison of 9-level, level shifting SPWM techniques; PD, POD, APOD of MMC and proposed inverter reduced harmonics and improves power quality. The proposed MMC inverter is transfer both active and reactive power, but is able to control the power factor.

ACKNOWLEDGEMENT

I manifest my heartier thankfulness pertaining to our contentment over., **Mr. Anshul Mahajan,** Assistant professorin the Electronics and Electrical Engineering department, Lovely Professional University, Punjab for his precious suggestions apart from general guidance, constant encouragement throughout my work, without which it would probably not possible for me to bring out the work in this form.

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ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 4, April 2016

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