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Automatic Test Stimulus Generation for RF Transceiver Diagnosis

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ABSTRACT:The development of contemporary and future wireless communication systems creates high demands for time efficient and accurate methods for production and validation of products. Testing RF transceivers requires the measurement of various parameters of RF impairments and their specification and multiple testing setups has to be used. To ensure product quality, RF circuits need to undergo rigorous testing and diagnosis. In this work, they focused on the problem of test stimulus optimization for determining the critical behavioural model parameters of RF systems using nonlinear solvers. First, a generic test stimulus, which was very compact in nature and optimized for maximum accuracy, was generated to check the RF transceiver. In the proposed design, the modulation technique is applied to the RF data transmitter and demodulation to the receiver and corresponding test stimulus is applied to the RF transceiver to detect the faults.

KEYWORDS:RF Transceiver,OFDM,BPSK modulation scheme.

I.INTRODUCTION

Due to the increased integration of RF circuits in scaled CMOS processes, manufacturing variability plays a critical role in end-to-end silicon yield. To ensure product quality, RF circuits need to undergo rigorous testing and diagnosis.
In this work, we focus on the problem of test stimulus optimization for determining the critical behavioural model parameters of RF systems using nonlinear solvers. Prior research in model parameter computation-based testing, used random stimuli resulting in longer than necessary test sequences incurring excessive test times. The keycontributions of this work are as follows:

1)We propose an algorithmic test stimulus generation technique for behavioral model parameter computation of RF transceiver systems. A compact test signal is derived that allows a nonlinear solver to determine the behavioral model parameters accurately from the observed time-domain test response which leads to reduction in test time. There are different types of test generation that includes multitoned signal, transient signal and many more. These deterministic test signals are sufficient to diagnose complex transmitter and receiver parameters.

2) It is shown that the RF power amplifier's fifth-order nonlinearity with AM-PM distortion and memory effects, nonlinearity of mixer and low-noise amplifier(LNA), I/Qgain and phase mismatch and dc offset can be diagnosed concurrently from the applied compact test. We show that with the use of only one sensor (an envelope detector attached to the output of the transmitter), it is possible to accurately diagnose individual nonlinearities of power amplifier (PA), LNA, and mixers (decoupling nonlinearities of cascaded blocks) of the transceiver in loopback connection along with other no idealities.

II.RELATED WORK

AUTHOR[1] Abhishek Chatterjee The rf impairments has a great impact in transmitter/receiver In phase/quadrature phase components gain and phase mismatch on the performance have become severe because of high operating speed and advanced technology. In this paper, we present a built-in-self-testing procedure for ofdm transceiver with quadrature modulation circuits which uses baseband signals of transmitter and receiver for test generation. The I/Q mapping between input signals of transmitter and output signals of receiver are used for extraction of rf impairment and nonlinearityparameters separately by means of Non linear least square (NLS) algorithm and detailed modeling of

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nonlinear system. Experimental results correspond to w the simulation results and they confirm the high accuracy of the proposedsystem.

AUTHOR[2] Anitha banerjee The ideal performance of digital predistortion technique depends on robust predistorters that can be used for complete compensation of the nonlinearities in power amplifier. In reality, the performance of the system can also be affected due to analog signal imperfections in the transmitter, which are caused by analog components ,particularly analog filters and quadrature modulators which are two common configurations for the up conversion chain in the transmitter: two-stage up conversion and direct up conversion. For a two-stage up conversion transmitter, we design a band-limited equalizer for the compensation of frequency response of the surface acoustic wave filter which are usually used in the intermediate frequency(IF) stage. For a direct up conversion transmitter, a model was developed to describe about the frequency-dependent in phase/quadrature phase component gain/phase imbalance and dc offset.Therafter two methods was developed to construct compensators for the phase/gain imbalance and dc offset. These compensation techniques are used to correct the analog imperfections, thereby improving the overall predistortion performance

III.PROPOSED SYSTEM

In proposed system, we are designing the BPSK modulator for modulating the original data and transmitted. This is in turn demodulated at the receiving end to retrieve the original data. Phase shift keying technique is widely used these days mostly in radio communications systems. This technique is mostly used in areas of data communications.

phase shift keying(PSK) allows data to be carried on a radio communications signal in a more efficient manner where more forms of communications are switching from analog formats to digital formats.Nowadays there is an increased importance in data communications feild along with its various forms of modulation techniques which can be used to carry data. The test stimulus is applied to the modulator and demodulator part to detect the faults occurred.

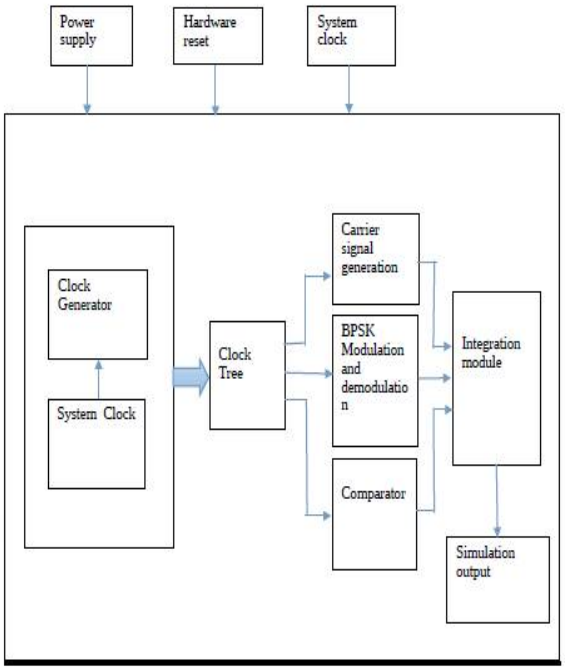

Fig 1. Proposed Block Diagram

IV.TESTING MODULE

FPGA are the next generation programmable logic devices. The word Field in (FPGA) refers to the ability of the gate arrays which are programmed for a specific function by the end user instead of depending on the programming techniques used by the manufacturer of the device.A series of columns and rows of gates are called as array which are programmed by the end user. When compared to standard gate arrays(SGA), the field programmable gate

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arrays(FPGA) are larger devices. The basic cell structure for FPGA is complicated than the basic cell structure of standard gate array.

FPGAs are semiconductor devices that are programmed based on the matrix of Configurable Logic Blocks (CLBs) connected by means of programmable interconnects.FPGA are opposite to Application Specific Integrated Circuits (ASICs),in which devices are custom and build for a particular design, FPGAs are programmed according to the desired application or functionality requirements.
One-Time Programmable (OTP) FPGAs are available as dominant type which are based on Static random access memory(S-RAM) and can be reprogrammed in various stages of design evolution. FPGAs provides designers the facility to change their designs as per their requirement in the design cycle– even after the manufacturing of end product and deployment of the same end product in the communication field for usage. In addition to this Xilinx FPGAs allow for field upgrades to be completed precisely , eliminating the redesigning cost or manually updating electronic system.

Fig 2.Spartan FPGA

V.DESIGN OF LFSR

A linear-feedback shift register (LFSR) is used for shifting operation where the input bits are used as a linear function of its previous state inputs. For the linear function of single bits The most commonly used gate is exclusive-or (XOR).Thus, an LFSR is most often used as a shift register whose input bit is obtained by the XOR operation of some bits from overall value of shift register. The initial value used in Linear Feedback Shift Register (LFSR) is called the seed. As the operation of this shift register is primitivistic , the stream of values obtained from the register can be completely determined from its current state or previous state value.
There are finite number of possible states in LFSR ,therefore it gradually enters a repeating cycle. An LFSR with a perfect feedback function that generates sequence of bits which appears in a random manner and has a very long cycle with n number of input test pattern generation.

Using the Trust-Worthy algorithm it defines a threshold value to the SUs to overcome the PUE attacks. It enables CR-Networks nodes to efficiently utilize the available spectrum channels. Nodes, which can easily find various licensed channel opportunities without interfering the primary system increases. This reveals that it has a potential to be able to convert the various network conditions into a performance improvement.

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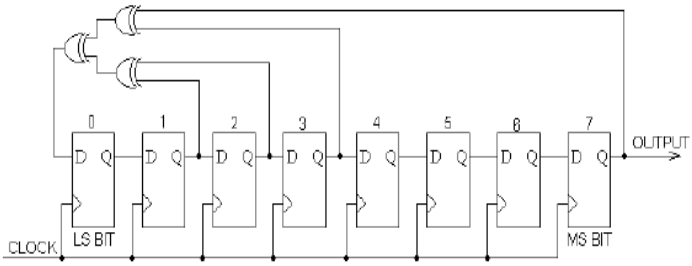

Fig 3.LFSR with digital logic

VI.SYSTEM CLOCK AND HARWARE RESET

One of the most important steps in the design process is to identify the usage of different types of clocks and procedures to route them. Here we can obtain the efficient usage of routing resources. Field-programmable gate arrays(FPGAs) has a dominating position in digital signal processing and embedded system applications. After completing calculationsprocedure in hardware, it is used to process data at rates much higher than most of well known fastest microprocessors. The availability of FPGA with increasing flexibility and affordable price of FPGAs have also made them most attractive alternatives to other application-specific integrated circuits Asynchronous integrated circuits (ASIC) are, particularly well suited for small-to-medium volume applications. As most complicated designs are implemented in FPGAs, it is common that most of them might have multiple data paths which runs on multiple clocks. The special attention is gained by FPGA with multiple clocks. There are various issues that has to be focused which includes maximum number of clocks and clock rates where skew rates can also be included. Relationship between clock and data and asynchronous clock design are important factors. In design of an Field Programmable Gate Array the reset are used as a synchronization signal which is used for setting all the storage elements to the state that is well known. In a digital designing process , designers usually use the global reset as an external pin which can initialize the design on power-up applications. The global reset pin is same as that of other input pins and it is often applied in an asynchronous manner to the FPGA. This signal is then used in the design for reset behavior either synchronously or asynchronously. Reset structures can be made more suitable according to our requirements. An optimal reset structure is used to enhance the utilization of device, timing and power consumption requirements in an FPGA.

VII.BPSK MODULATION SCHEME

Digital modulation is a process where the characteristics of carrier signal are varied according to the value of data or message bits that are transmitted. Therefore it is compatible with characteristics of the channel. The binary phase shift keying modulation technique is the most simplest of all other psk modulation techniques as it takes thelarge level of noise or distortion to reach an incorrect decision in the demodulator at the receiver side.BPSK technique uses inly one bit/symbol, for modulation purpose therefor it is not suitable for high data rate application.In BPSK carrier phase is varied in accordance with the modulating signal or input signal with carrier phase where the output with logic 0 undergoes phase shift and is obtained as the output with logic 1 and vice versa.The binary sequence is multiplied with the sine wave generated by the oscillator to get the BPSK modulated signal. The carrier is recovered by the carrier recovery circuit. The bpsk modulated signal is multiplied with the sine wave generated by the carrier recovery circuit and passed through the integrator and the decision device to detect the original modulated signal.In Binary Phase Shift Keying (BPSK), the phase of the sinusoidal carrier signal is variedin accordance with the value of the binary information data bit to be transmitted. It isalso called bi-phase modulation or phase reversal keying. The carrier phase is changed among $0^o$and 180^o by the input signal or message with varying bits. The BPSK signal can be expressed in the form , A sin (2πft) is carrier signal with A-asamplitude and phase shift value is given as sin term with 0^o as the initial phase. When the input message bits changes from 1 to 0 or 0 to 1 the modulated output signal undergoes the phase shift between two decision points.In this BPSK modulator, when clock signal (clk) is applied then STAGE0 generatesthe carrier sinusoidal signal (A sin (2πft)) and initial phase is 0^orepresented bySinWave0. Similarly, STAGE1 generates the carrier sinusoidal signal (A sin (2πft +π)) whose frequency is 322 MHz and initial phase is 180^o represented bySinWave180. So the output of STAGE0 and STAGE1 are same but they are out ofphase.The Bit Separator bloc is given as STAGE 2. Which is used for separation of one successive signal bit by considering the time

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period of length 1 in sinusoidal signal. Separates one successive massage signal bit by one time period of sinusoidal signal. Three input signals of bit separator include clock, start and data.

Start signal acts as enable signal forBPSK Modulator. Data signal represents the digital massage signal bit. The outputsignal of Bit Separator acts as a select input for STAGE3 which is basically amultiplexer and represented by MUX_BPSK. This signalselects output of STAGE0or STAGE1 as input signal of multiplexer. The output of multiplexer (BPSK_OUT) is the BPSK Modulated signal.

VIII POWER SUPPLY

Today's FPGAs tend to operate at lower voltages and higher currents than their predecessors. Consequently, power supply requirements may be more demanding, requiring special attention to features deemed less important in past generations. Failure to consider the output voltage, sequencing, power-on, and soft-start requirements can result in unreliable power-up or potential damage to FPGAs. Output Voltage Requirements The first criteria to consider when designing power supplies for FPGAs are the voltage requirements for the different supply rails.

Most FPGAs have specifications for the CORE and IO voltage rails and many require additional auxiliary rails that may power internal clocks, phase-lock loops or transceivers. Since FPGAs generally specify several permissible voltage levels for the IO, the voltage selected is dictated by the external digital circuitry. To provide flexibility, FPGAs will generally provide multiple IO banks that can be powered separately, allowing FPGAs to interface with various logic families. For simplicity, the solutions illustrated in this article will assume all IO banks are powered off of a single power supply rail.

Modern cores utilize 65 nm, 45 nm or even 40 nm geometry silicon processes and may operate from voltages as low as 0.9V. These lower voltages are valuable to reduce power dissipation in FPGAs. The trade off, however, is that keeping within the voltage tolerance requirements becomes more challenging for the power supply designer.

IX DATA FLOW DIAGRAM

A data flow diagram is a graphical representation of flow of data through an information system and modelling its process aspects.It is often used as an preliminary step to create an overview of the system.

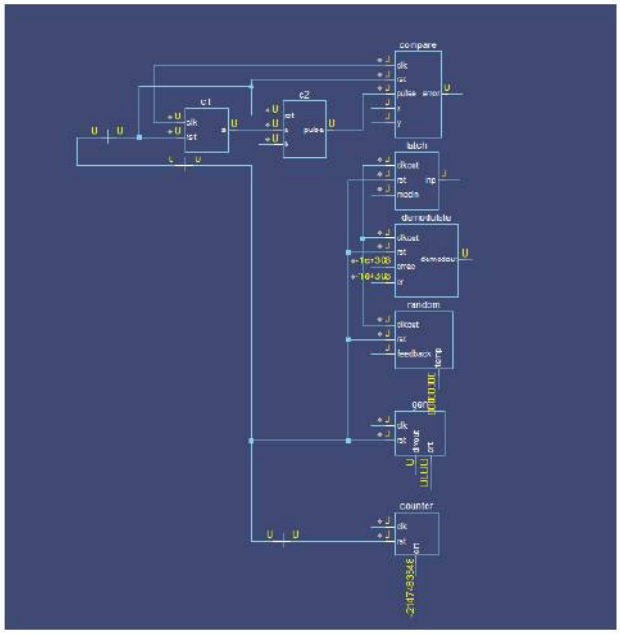

Fig 4. Modulation and Demodulation as well as error checking

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X.SIMULATION RESULTS

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device.

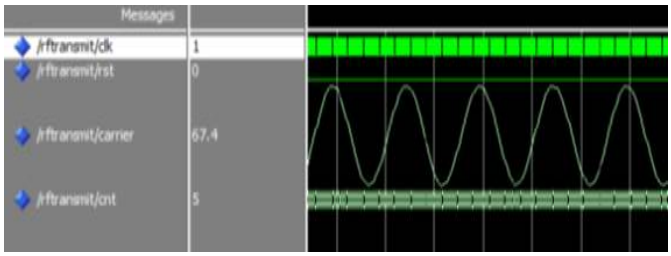

Fig 5.Carrier signal generation

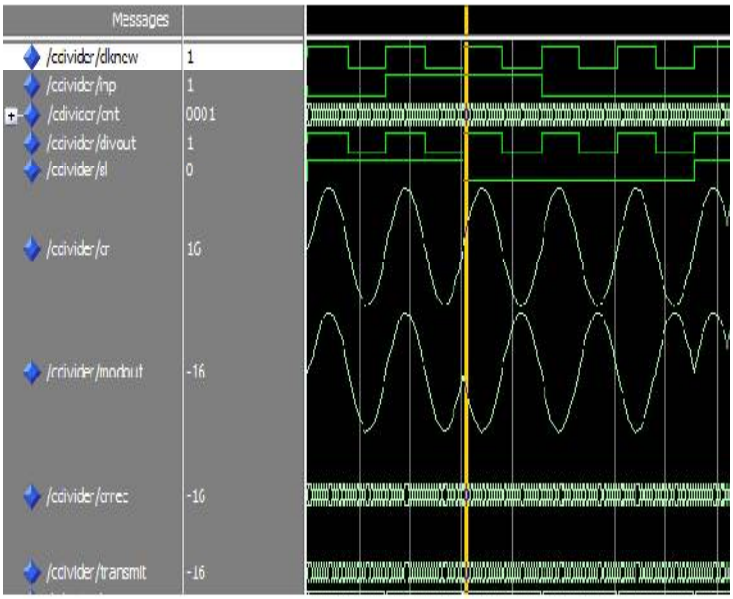

Fig 6 modulation and demodulation

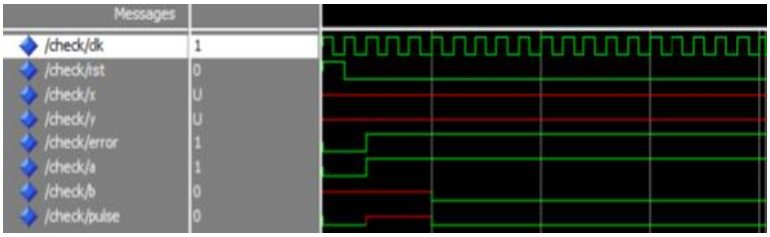

Fig 7 error checking mechanism

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XI. CONCLUSION

In this paper RF Testing is done using BPSK modulation technique. Optimized signals are generated with linear feedback shift register and carrier signals are generated by increasing the count value where modulation and demodulation takes place with two decision points. The original input data and carrier signals are recovered back .Input signal is compared with demodulated output to check whether Device under Test (DUT) is working or not.

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