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Wide Range of Voltage Conversion Using Level Shifter with Sleep Transistor In Multisupply Voltage Design

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ABSTRACT: Multisupply voltage design using Level Shifter based on Multithreshold CMOS technique is an effective approach to reduce power.Multisupply voltage design technique is widely used in modern system-on-chips to tradeoff energy and speed. Level shifters (LSs) allow different voltage domains to be interfaced. In this brief, new LS is presented for fast and wide range voltage conversion. Because ofa novel architecture combined with the use of multithreshold CMOStechnique, the proposed circuit guarantees robust voltage shifting, which exhibits fastresponse and low energy consumption. Level Shifter is combined with Sleep transistor for reducing the power. When implemented in a 90-nmtechnology node, theproposed design reliably converts 100-mV input signals into 1 V output signals. Post-layout simulation results demonstrate that this new LS shows a power output as $7.56x10^{-008}$W and Level Shifter along with Sleep transistor provide the power output as $8.79x10^{-010}$W.

KEYWORDS: Level Shifter, Multithreshold CMOS, Sleep transistor, Multisupply voltage design(MSVD).

I.INTRODUCTION

A number of techniques can be used to provide large voltage conversion range in modern system-on-chip applications. Fast and wide range voltage conversion in multi supply voltage is used for reducing power, increasing speed and to obtain large voltage conversion range. Supply voltage is one of the dominant factors that determine the timing performance and power consumption of VLSI chips. Multisupply voltage domain (MSVD) technique is emerging as an effective method to reduce both dynamic and leakage powers intoday's system-on-chips [1]. This approach consists of partitioning the design into separate voltage domains (or voltage islands), each operating at a proper power supply voltage level depending on its timing requirements. Time critical domains run at higher power supply voltage (VDDH) to maximize the performance, whereas noncritical sections work at lower power supply voltage (VDDL) to improve power efficiency without impacting on the overall circuit performance.

In an MSVD system, a well-known LS is the differential cascade voltage switch (DCVS) circuit that is typically used for converting signals between the two different above-threshold voltage domains [2]. Unfortunately, the DCVS-LS behaves as a ratioed circuit and the contention between the pull-up and pull-down networks becomes severe when input signals are in the subthreshold range, thus making the conventional sizing techniques impractical to obtain a properly functioning circuit [6]. To address this problem, several improvements to the conventional DCVS circuit have been proposed in [2], [3], and [6]–[10]. The four-stage cascaded DCVS circuit described in [3] assures robust level up conversion from the subthreshold regime. Unfortunately, it introduces large power penalties, owing to the intermediate power supplies. Furthermore, it shows a limited speed performance. Two-stage LS was proposed in [7]: the first stage exploits a DCVS circuit with an always-on diode-connected nMOS transistor on thetop; whereas, the second one is a conventional DCVS stage that achieves rail to rail swing. Such a strategy avoids intermediate power lines, but again it is not enough to reach high speed performances. A circuit based on current mirrors has been proposed in [6]. It is characterized by significantly better speed performance, but unfortunately, the current mirror output floats when the input voltage signal is high. This causes a significant detrimental effect on subthreshold leakage of the output buffer. Recently, we proposed low-power LS, suitable for voltage signal up-conversion from the near/subthreshold regime,

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which exhibits very low static and dynamic energy consumption [10]. This is obtained at the expense of reduced voltage conversion range, and of relatively limited speed. In this brief, we present a new LS that trades a certain amount of static power for a significantly improved operating speed and an extended voltage conversion range. When implemented with the 90-nm CMOS technology, the new design reliably converts input signals as low as 0.1 V to the 1 V voltages.

II. PROPOSED SYSTEM

The proposed system architecture consists of three stages they are input inverter stage, main voltage conversion stage and output inverter stage. In the proposed architecture each transistors perform its own function. The MTCMOS technique uses two type transistors in this design to provide fast switching and better performances. Logic is supplied by a virtual power rail. Low V_{th} devices are used in the logic where fast switching speed is important. High V_{th} devices connecting the power rails and virtual power rails are turned on in active mode, off in sleep mode. High V_{th} devices are used as sleep transistors to reduce static leakage power.

The system architecture is shown in Fig 1.1

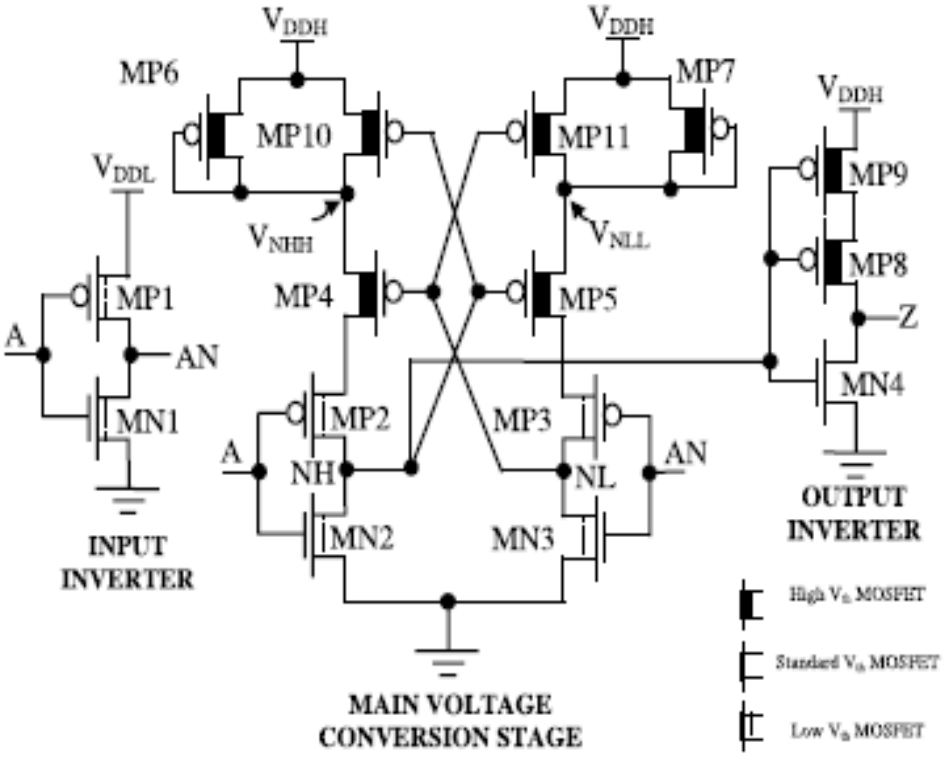

Fig 1.1 Proposed System Architecture

The transistors used here are high V_{th} MOSFET, low V_{th} MOSFET and Standard MOSFET.

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TABLE 1.1 Purpose of Each Transistor

TRANSISTOR	TYPE	PURPOSE
MP_1,MN_1	Lvt	Fast differential low voltage input signal
MN_2,MN_3	Lvt	Provide higher strength of pull-down network for main conversion range.
MP_2,MP_3	Lvt	Limits cross bar current
MP_4,MP_5	Hvt	Helps in weakening the pull-up networks and reduce leakage current flowing through the pull-up networks when they are turned off.
MP_6,MP_7	Hvt	Diode connected transistor for reliable voltage conversion.
MP_6-MP_{10},MP_7-MP_{11}	Hvt	Diode connected transistors to reduce switching delay
MP_{10},MP_{11}	Hvt	Controlled by NH and NL node
MN_4	Svt	Allows static current
MP_9,MP_8	Stacked HvtPMOS	Control the static current discharge in MN_4 ,when NH is high to significantly reduced.

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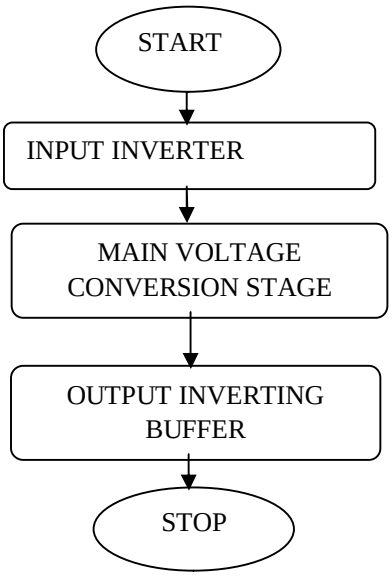
III. DATA FLOW DIAGRAM



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IV MODULE DESCRIPTION

The proposed system has three modules they are

- Input inverter stage
- Main voltage conversion stage
- Output inverter stage

4.1 Input inverter stage

Two transistor have been used at the input inverter stage (MP1/MN1).The input provided will be "A". The inverted outputs obtained by this "AN".MP1/MN1 transistor are the low threshold transistor, used for fast differential low-voltage input signal to Main voltage conversion range.

4.2Main voltage conversion range

Main voltage conversion range used as LS to shift voltage from one domain to another. Before the rising (falling) transition of the input signal A (AN), the nodes NH and NL are held high and low, respectively. Therefore, MP10 is switched off and MP11 is switched on. A high to low transition of the main input causes MP4 being turned on. Its drain current brings the diode-connected MP6, MP10device into the saturation region. This creates a voltage drop (i.e., Vth, MP6, MP10) across MP6, MP10terminals that produces a correspondent bulksource voltage drop on MP4. Due to the bulk effect, this increases the MP4 threshold voltage. The reduced voltage level (VDDH-Vth, MP6, MP10) on the source terminal of MP4 limits its VGS, thus further weakening the MP4 action. All the above effects reduce the contention on the node NH, thus allowing faster discharging to be achieved. When MP4 is turned on, MP5 is consequently turned off.

In this case, the small leakage current flowing through MP5 is not enough to turn MP7 on. For this reason, MP5 results power gated from the VDDH power rail, leading to a significant reduction in its sub-threshold current. The diode-connected MP7 device participates in minimizing the leakage current, also by increasing the threshold voltage of MP5. In fact, MP7get full VDDH voltage. As the input signal switches, the transistor MN2 is turned on and the node NH starts to be discharged. Owing to this, MP4 is weakened, thus speeding up the discharge of the node NH. In the meantime, the stronger pull-up of the right branch charges the node NL and a positive feedback is triggered causing MP4 to be turned off. This allows the discharging of NH to be further accelerated. As NH approaches the ground voltage, the positive feedback is again triggered, causing MP5 to be completely turned on. Therefore, NL is fully charged at the VNLL voltage level. Once transitions on the nodes NH and NL are completed, the virtual power supplies VNHH = VDDH and VNLL = VDDH−*V*dsat, MP7 are establishedto provide fast switching in the subsequent input transition.

4.3 Output inverter stage:

The output inverter stage is designed using standard threshold voltage transistor and stacked high threshold voltage transistors. These transistors get the output signal Z from the main voltage conversion stage. The extra PMOS transistor in the output inverter is used to control the static discharge of MP_8 transistors by maintaining the source gate voltage below VDDH.From this Vt of MP8 increases. So the source gate voltage of MP8 decreases.So,it reduce static current.

As this moment, sleep transistor is placed in series with MP6-MP10, MP7-MP11, MP8 and power supply. The sleep control scheme is used for efficient power supervision.In active time,sleep transistor is turned ON,while their on-resistances issmall and supply voltage almost function as real power line.During standby manner,sleep transistor turned off and decreasing the power dissipation.

V. RESULT

The tanner tool can be used to perform the post layout simulation of the proposed system. Table 5.1 shows that the comparison of power using different configuration of technology. Its power and delay are compared with different configuration of technology.

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Table 5.1 Resource Comparison for Power in existing method

CONFIGURATION	TECHNOLOGY (nm)	DELAY (ns)	POWER(µW)
CVS	90	28.27	-
DCVS	90	25	17.6
Current mirror	130	18.5	20.4

Table 5.2 shows that the power in proposed system of Multi-threshold CMOS technology and Multi-threshold CMOS technology along with Sleep Transistor.

Table 5.2 Resource for power in proposed system

CONFIGURATION	TECHNOLOGY (nm)	POWER(W)
MT-CMOS	90	7.568217e-008
MT-CMOS with Sleep transistor	90	8.796456e-010

This type of configurations is now used in modern system on chip to trade off power and speed. These low power circuits can be used to provide both low and high supply voltages with minimum power. Here by simulation can obtain a large voltage conversion range can be obtained by some 100mv to 1v this process of switching takes place with minimum delay. The power of the circuit can be varied by changing the channel length of each transistor the length and width for each device is already set to default in the tool for all types of transistors.

Here the virtual power supplies are varied in accordance with the input signal A. the two nodes follow the rising and falling transition of the device. If the node NH is weak the virtual power supply V_{NNH} can be fed with voltage V_{DDH}-V_{Dsat} the V_{Dsat} is the voltage just below the switching voltage. If the node NL is strong the node V_{NNH} is supplied with the full voltage V_{DDH} ie, 1V.

The fig 5.1.a shows the schematic of Level shifter of multi-threshold CMOStechnology.

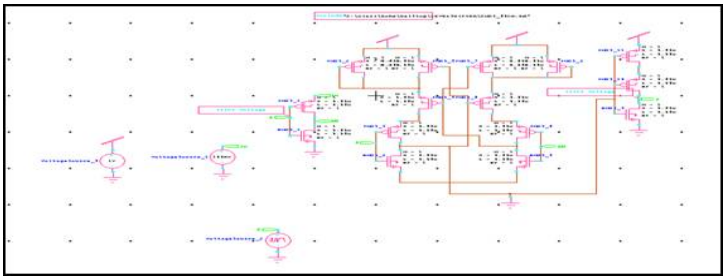

Fig 5.1.aSchematic Diagram of Level Shifter

The fig 5.1.b shows the output waveform of level shifter with input A and Output Z.While giving 100mv as the input it produce the output as 1V.

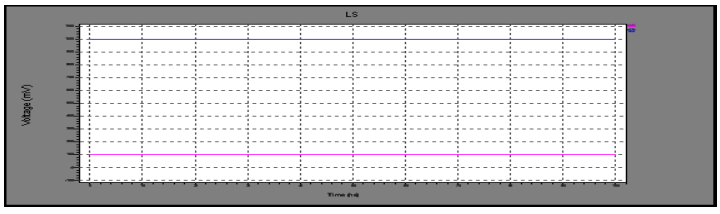

Fig 5.1b Output Waveform of Level Shifter

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The power results of level shifter are given below

Power Results
V_{DD} GND from time 0 to 1e-007
Average power consumed -> 7.568217e-008 watts
Max power 7.568217e-008 at time 8e-008
Min power 7.568217e-008 at time 4e-008

The fig5.2.a shows the schematic waveform of level shifter with sleep transistor in Multi-threshold transistor.

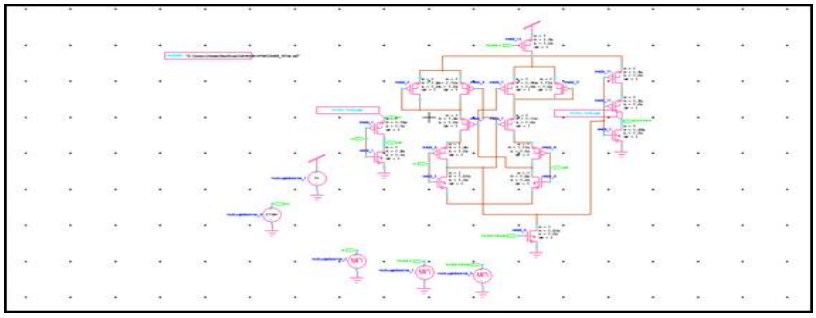

Fig 5.2.aSchematic Diagram of level shifter with sleep transistor

The fig 5.2.b shows the output waveform of level shifter with sleep transistor with input A and output Z. While giving 100mv as the input it produce the output as 1V.

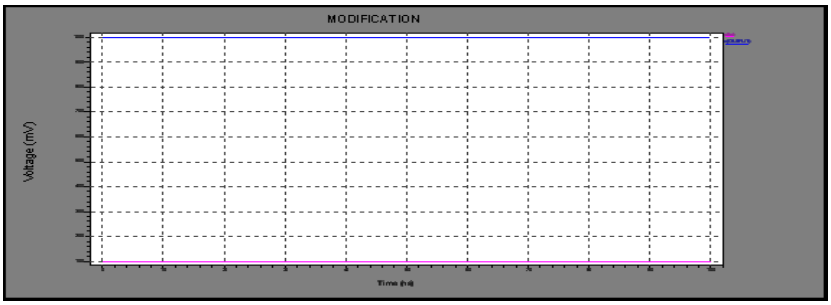

Fig 5.2b Output Waveform of level shifter with sleep transistor

The power results of level shifter with sleep transistor are given below
Power Results
V_{DD} GND from time 0 to 1e-007
Average power consumed -> 8.796456e-010 watts
Max power 9.246118e-008 at time 6.1e-008
Min power 1.001646e-009 at time 6e-008

VI. CONCLUSION AND FUTURE WORK

The proposed architecture exploits proper design strategies to increase the operating speed while maintaining very low energy consumption and large voltage conversion range. A new level shifter allows multi supply voltage conversion which uses CMOS technique. Such circuit guarantees robust voltage shifting from the deep sub threshold to the above threshold while exhibiting fast response and low energy consumption.
Future work will consider the evaluation of the benefits of the proposed technique. In the future works, going to implement this low power design in low power application like Shift register.

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BIOGRAPHY

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