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Mutilevel Inverter Hybrid DSTATCOM Topology for Power Quality Improvement

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ABSTRACT: -Power electronic device, nonlinear and unbalanced loads have given rise to power quality problem in distribution systems. Owing to factors like competitive generation patterns in an exceedingly deregulated electrical grid and an increasing level of sensitive end user devices, it has become necessary to confirm each reliable and power quality to the top client. A way to betterment the power quality is employing a Distribution Static Compensator (DSTATCOM) to compensate active and reactive power, power issue correction and voltage stability. In this paper, the planning of a DSTATCOM using a Cascade H-Bridge multilevel inverter (CHBMLI) (which reduces voltage stress, THD and improves efficiency) in an exceedingly medium voltage distribution grid is bestowed.. During this study, the planned controller in DSTATCOM structure so as to power quality improvement primarily based proportional integral (PI) controllers and p-q coordinates. Simulation result prepared by the assistance of Mat lab/Simulink software. The Simulink results are bestowed to verify the performance of the planned construction DSTATCOM.

KEYWORDS: Power quality (PQ), Total Harmonic Distortion (THD), Distribution static compensator (DSTATCOM), Cascade H-Bridge multilevel inverter (CHBMLI).

I. INTRODUCTION

The problems that have an effect on the power quality in distribution systems are relating to the specifications of the masses. A number of the foremost widespread effects are the harmonics generated by nonlinear masses and unbalanced masses. A part from the nonlinear masses, events like motor starting, condenser shift and strange faults might additionally impose power quality (PQ) issues. Here in this paper some hybrid topologies that are projected to think about the limitations of the standard DSTATCOM, wherever a reduced rating active filter is employed with the passive elements. However, the reduction in voltage is limited due to the utilization of an L-type interfacing filter. This conjointly makes the filter larger in size and includes a lower slew rate for reference chase. An LCL filter has been projected because the foreparts of the CHBI within the literature to beat the restrictions of an L filter. It provides higher reference tracking performance while using lower worth of passive elements. This However, the LCL filter uses a similar dc-link voltage as that of DSTATCOM using an L filter. Hence, disadvantages attributable with high dc-link voltage are still present in the LCL filter are employed. Another serious issue is resonance damping of the LCL filter, which can push the system toward instability.

These varieties of compensation have some disadvantages like restricted bandwidth, slower response, additional losses and large size. Recently, attributable with quick extension of high power switching components like IGBTs and IGCTs, DSTATCOM could be shunt custom power devices, that has been recognized in the second generation compensator for power factor correction, load leveling, voltage regulation and harmonic filtering in distribution systems.

In this paper here we tend to introduce an improved hybrid DSTATCOM topology with a PI-Controller based five-level CHBI for the current harmonic, voltage flicker and reactive power mitigation of the nonlinear load. Wherever the LCL filter followed by the series condenser is employed at the forepart of the CHBI to deal with the

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aforesaid problems. The adoption of cascade H–bridge inverter for DSTATCOM applications causes to decrease in the device voltage and also the output harmonics by increasing the quantity of output voltage levels and therefore the reference tracking performance at the same time.

The performance of the projected topology is valid through the intensive simulation results using Mat lab/Simulink.

II. PROPOSED DSTATCOM TOPOLOGY

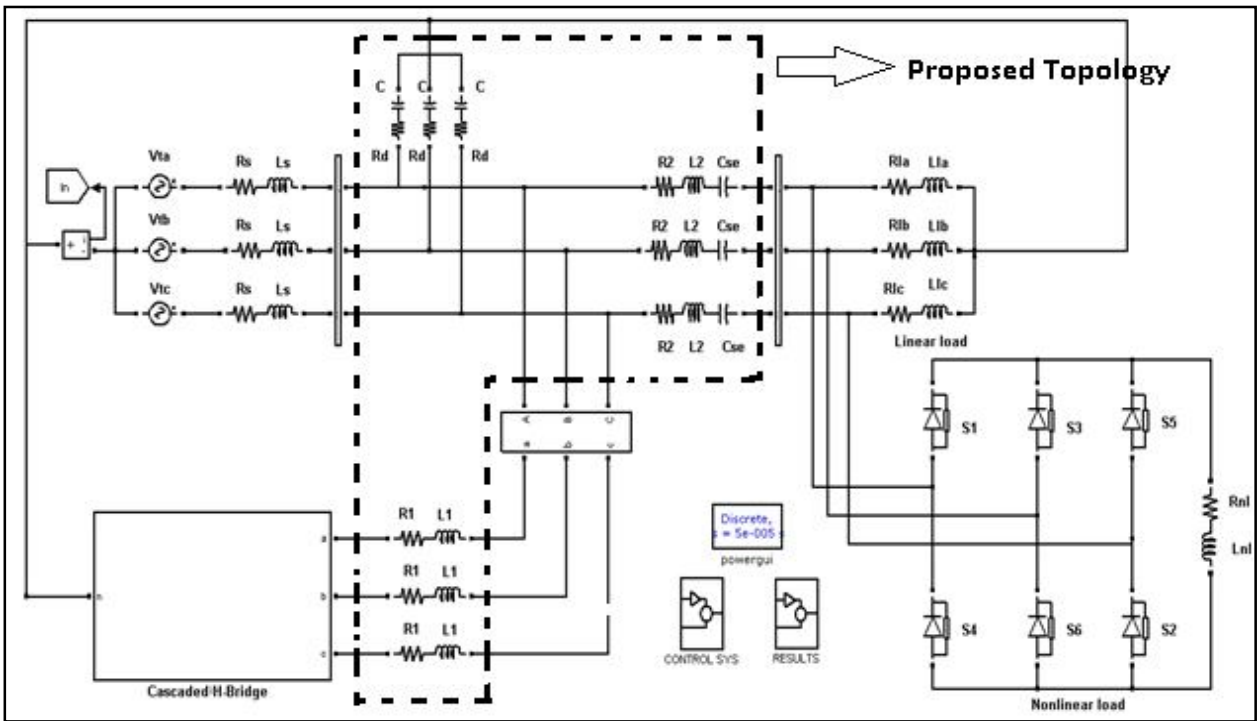

Figure. 1. Proposed DSTATCOM topology with five level Cascaded H-Bridge inverter in the distribution system to compensate unbalanced and nonlinear loads.

A three-phase equivalent circuit diagram of the projected DSTATCOM topology is shown in Fig. 1.It is completed by employing a three-phase four-wire two-level neutral-point-clamped inverter. The projected theme connects an LCL filter at the forepart of the electrical converter that is followed by a series capacitor C_{se}. Introduction of the LCL filter considerably reduces the dimensions of the passive part and improves the reference tracking performance. Addition of the series capacitor reduces the dc-link voltage and, therefore, the power rating of the inverter.

Here, R_1 and L_1 represent the resistance and inductance at the inverter side; R_2 and L_2 represent the resistance and inductance at the load aspect and C is that the filter capacitance forming the LCL filters part in all 3-phases. A damping resistance R_d is employed in series with C to damp out resonance and to supply passive damping to the system. Inverter and filter currents are $I_{f1a}$and I_{f2a} in phase-a and is similar for alternative phases. Additionally, voltages across and currents through the shunt branch of the LCL filter in phase-a are given by V_{sha} and I_{sha}, severally, and equally for the opposite 2 phases. The voltages maintained across the dc-link capacitors are $V_{dc1} = V_{dc2} = V_{dcref}$ .The DSTATCOM, source, and loads are connected to a typical point known as the point of common coupling(PCC).Loads used here has each linear and nonlinear part, which can be balanced or unbalanced.

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DSTATCOM CONTROL

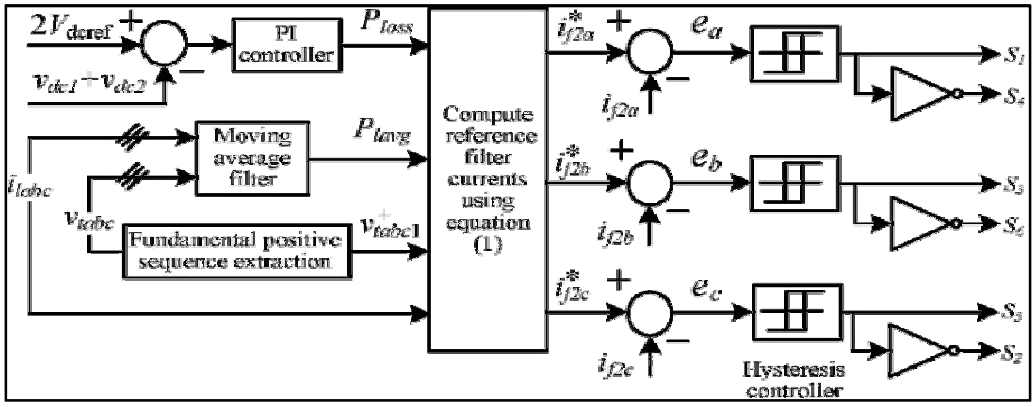

Figure. 2. Controller block diagram

The overall control diagram is shown in Fig. 2. The DSTATCOM is controlled in such a simplest way that the source currents are balanced, sinusoidal, and in phase with the individual terminal voltages. Additionally average load power and losses within the inverter provided by the supply. Since the source about here is non-stiff, the direct use of terminal voltages to calculate reference filter currents won't offer satisfactory compensation. Therefore, the fundamental positive sequence components of three-phase voltages are extracted to come up with reference filter currents (i^*_{f2a}, i^*_{f2b} and i^*_{f2c}) supported the instantaneous active and reactive power theory. These currents are given as follows:

$$i^*_{f2a} = i_{la} - i^*_{sa} = i_{la} - \frac{v^+_{ta1}}{\Delta^+_1}(P_{lavg} + P_{loss})$$

$$i^*_{f2b} = i_{lb} - i^*_{sb} = i_{lb} - \frac{v^+_{tb1}}{\Delta^+_1}(P_{lavg} + P_{loss})$$

$$i^*_{f2c} = i_{lc} - i^*_{sc} = i_{lc} - \frac{v^+_{tc1}}{\Delta^+_1}(P_{lavg} + P_{loss}) \qquad \textbf{(1)}$$

Where $V_{ta1}{}^+$, $V_{tb1}{}^+$, and $V_{tc1}{}^+$ are fundamental positive sequence voltages at the various section load terminal, the term φ is the desired phase angle between the source voltage and current and $\Delta_1{}^+ = (V_{ta1}{}^+)^2 + (V_{tb1}{}^+)^2 + (V_{tc1}{}^+)^2$.The terms P_{lavg} and P_{loss} represent the typical load power and also the total losses within the inverter, severally. The typical load power is calculated employing a moving average filter for higher performance throughout transients and might have a window dimension of half-cycle or full cycle relying upon the odd or even harmonics, severally, gift within the load currents. At any instant t_1, it's computed as follows

$$P_{lavg} = \frac{1}{T}\int_{t1-T}^{t1}(v_{ta}i_{la} + v_{tb}i_{lb} + v_{tc}i_{lc})\,dt \qquad \textbf{(2)}$$

The overall losses within the Inverter are computed employing a proportional–integral (PI) controller at the positive zero crossing of phase-a voltage. It helps in maintaining the dc-link voltage $\mathbf{V}_{dc1} + \mathbf{V}_{dc2}$ at a reference worth 2Vdcref by drawing a collection of balanced currents from the supply and is given in eq 3.

The current error $\mathbf{e}_{abc}$ is obtained by subtracting the particular filter currents from the reference filter currents. The error is regulated around predefined phenomenon band h mistreatment hysteresis current controller (HCC), IGBT switching Pulses are generated.

- If h ≤ lim then hys(h) = 1, top switch is turned ON, whereas bottom switch is turned OFF (S_a= 1, S'_a= 0).
- If h ≥ lim then hys(h) = −1, bottom switch is turned ON, whereas top switch is turned OFF (Sa= 0, S'_a= 1).

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$$P_{loss} = K_p e_{vdc} + K_i \int e_{vdc}\, dt \qquad (3)$$

Where Kp, Ki, and $e_{vdc} = 2V_{\text{dcref}} - (v_{dc1} + v_{dc2})$are the proportional gain, integral gain, and voltage error of the PI controller, respectively

III .Five-Level Cascade H-Bridge Inverter Based DSTATCOM

Fig.3 shows the circuit diagram of 5-Level CHBI-DSTATCOM. Where R+$\omega$is impedance of the convertor. A 5-Level CHBI is in parallel with the power line through the reactor. By adjusting the phase and magnitude of the AC output voltage of the convertor, the convertor will send or absorb reactive power that meets the requirements and achieves the dynamic reactive power compensation. This is often the essential principle of CHBI-DSTATCOM.The drop of the connected reactor has generated by the compensation current it may also filter the number of the high harmonics are generated by the supply aspect. So, by adjusting the output voltage and currents of the H-Bridge modules, the dc bus voltage may also be corrected. If the dc bus voltage is controlled the reactive power may also be controlled.

IV.DSTATCOM PARAMETER DESIGN

The dc bus voltage and interfacing filter values of the traditional DSTATCOM are calculated based on the procedure outlined in [28]. For a provided voltage of 230 V, a load rating of 10 kVA, a most switching frequency of 10kHz, and a ripple current of 1A (5% of the rated current), the dc-link voltage and interfacing inductor values are found to be 520 V and 26 mH, severally. For the LCL filter based mostly DSTATCOM topology, the dc bus voltage and filter parameters are chosen for constant set of design necessities .The 1-phase revalant circuit diagram of the passive filter of the planned theme connected to the PCC is shown in Fig. 4. The term uV_{dc} represents the inverter pole voltage with $\mathbf{u}_{as}$ a switching variable having a worth of +1 or −1 relying upon the switching states. The procedure to style the filter parameters is given here very well.

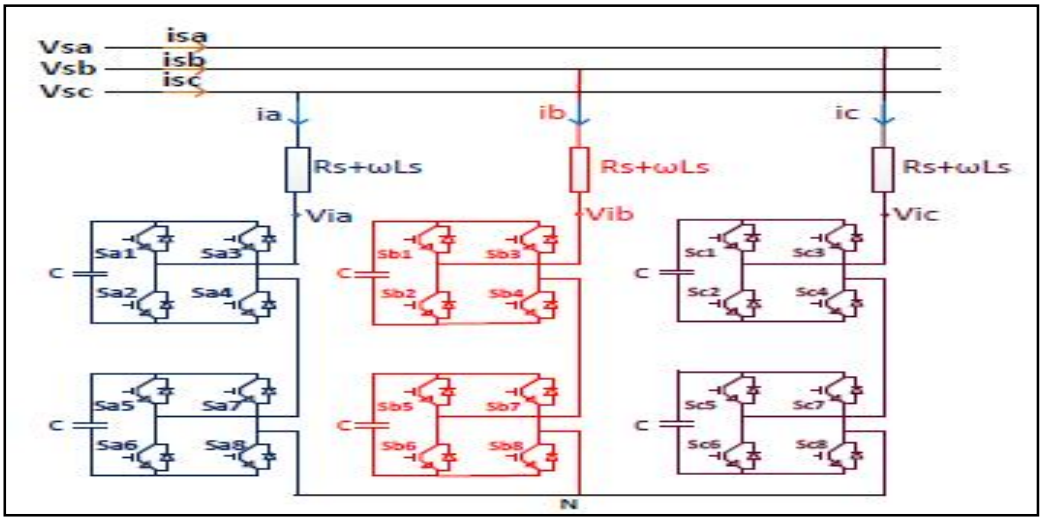

Figure 3. Five level Cascaded H-bridge inverter based DSTATCOM

1) ***Reference DC-Link Voltage V_{dcref} :*** The voltage across the dc condenser could be a source of energy and is chosen to attain good trailing performance. Here, the employment of a series condenser and a tiny low filter electrical device has enabled a major reduction in the dc-link voltage. In present case, a dc-link voltage of 110 Vis chosen, that is found to produce satisfactory compensation.

2) ***Design of LCL Filter Parameters:*** whereas coming up with appropriate values of LCL filter parts, constraints

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like cost of inductor, resonance frequency f_{res}, selection of damping resistor Rd, and attenuation a switching frequency f_{sw} ought to be thought-about.

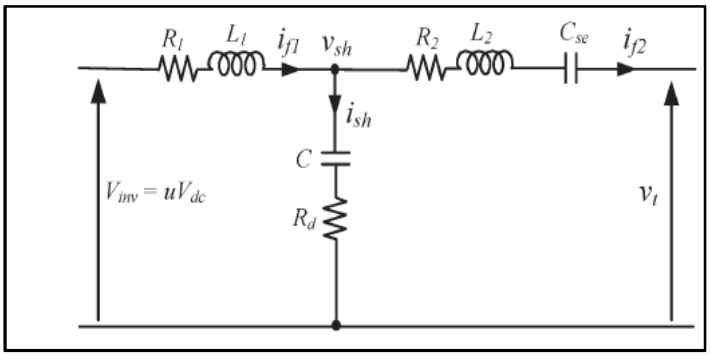

Fig 4.Single phase circuit diagram of the passive filter

Consider only L_1 of the filter, as shown in Fig. 4, is used. The worth of inductance L_1 is chosen from an exchange, which provides a fairly high switching frequency and sufficient rate of modification of the filter current, such the CHBI currents follow the reference currents. At any point of time, the following equation represents the inductor dynamics

$$L_1 \frac{di_{fi}}{dt} = -v_t - R_1 i_{fi} + V_{\text{dcref}} \qquad (4)$$

For further analysis, $\mathbf{R}_1$ can be neglected. The inductor is designed to provide good tracking performance at maximum switching frequency, which is achieved at zero supply voltage in the HCC.Taking these into consideration, inductance *L*1 is given by

$$L_1 = \frac{V_{\text{dcref}}}{(2h_a)(2f_{\max})} = \frac{V_{\text{dcref}}}{4h_a f_{max}} \qquad (5)$$

Where $2h_a$ is allowable ripple in the current and f_{max} is the maximum switching frequency achieved by the HCC.The large ripple current can lower the IGBT switching frequency and lowers the losses. However, it may be seen from eq (5) that the smaller ripple current leads to higher inductance and, thus, a lot of core losses. Therefore, a ripple current of 20%is taken whereas compromising the ripple and inductor size. The use of a series capacitor has reduced the dc-link voltage to 110 V. Therefore, subbing the values of the ripple current and reference dc-link voltage V_{dcref} in eq(5) while keeping f_{max} constant at 10 kHz, the worth of L_1 comes resolute to be 1.375 mH. To restrict the switch frequency below 10 kHz, L_1 is taken more than the calculated worth, therefore, 1.5 mH is chosen.

Once L_1 is chosen to attenuate lower order harmonics, L_2 and C have to be compelled to be designed for elimination of upper order harmonics. At higher frequencies, the resistance offered by C_{se} is going to be abundant below that of L_2 and might be neglected while coming up with LCL filter parameters. Neglecting R_1, R_2, and C_{se} at higher frequencies, the subsequent transfer functions are obtained:

$$\frac{I_{f1}(s)}{V_{inv}(s)} = \frac{s^2 + \frac{1}{L_2 C}}{sL_1\left(s^2 + \left(\frac{L_1+L_2}{L_1 L_2 C}\right)\right)} \qquad (6)$$

$$\frac{I_{f2}(s)}{V_{inv}(s)} = \frac{\frac{1}{L_1 L_2 C}}{s\left(s^2 + \left(\frac{L_1+L_2}{L_1 L_2 C}\right)\right)} \qquad (7)$$

From eq (7), the expression for resonance frequency will be Where $k = L_2/L_1$. The resonance frequency should

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be larger than the highest order harmonic of this to be remunerated. If the highest harmonics order to be compensated is 40 and taking a variation of 20%, f_{res} seems to be 2400 Hz for a 50-Hz system. Choice of $L_2 > L_1$ (i.e.,$k > 1$) can scale back the aptitude of L_1 to attenuate lower order harmonics. Therefore, lower order harmonics are going to be conjointly attenuated by inductor L_2 to attain satisfactory compensation performance.

$$f_{\text{res}} = \frac{1}{2\pi}\sqrt{\frac{1+k}{kL_1C}} \qquad (8)$$

Usually, the magnitude of the lower order harmonics within the LCL filter is employed to be high as compared with the higher order harmonics. Hence, the current through the shunt capacitor and therefore the inductor L_1 can increase for k>1.This will increase the damping power losses, the reactive power loss in inductor L_1, and therefore the inverter current. Moreover, the source current will increase because the damping power losses are extracted from the supply. Hence, $L_2 > L_1$ can end in more losses and value.

Therefore, to make sure low loss and high efficiency, a lower worth of k is chosen ($k < 1$). A higher C will give a low resistance path for harmonics however can draw more reactive current from the CHBI that any will increase the loss in L1 and IGBT switch. However, a smaller capacitance will not give decent attenuation, which, in turn, is paid by choosing a bigger inductor. As a trade-off between these necessities, C = 10 μF is chosen. The value of k is found to be 0.42 exploitation eq (8). With this worth of k, L_2 will be0.6 mH.

The equivalent resistance of the LCL filter approaches to zero at the resonance frequency f_{res}, and therefore the system might become unstable. However, the system may be created stable by inserting a resistance R_d in series with the capacitor. Usually, it is chosen in proportion to the capacitive reactance at f_{res}, i.e., X_{cres}, such the damping losses are minimum whereas assuring system stability. The reactance electrical phenomenon at resonance will be

$$X_{\text{cres}} = \frac{1}{2\pi f_{\text{res}} C} \qquad (9)$$

The power losses in the damping resistor will be

$$P_{loss} = 3 * R_d * \sum_{h=1}^{n} I_{sh}^2 \qquad (10)$$

Where h is that the harmonic order of the current flowing through R_d. within the LCL filter-based DSTATCOM topology, R_d is chosen such the damping losses are reduced whereas assuring that the adequate resonance damping is provided to the system.

The reason for considering damping power losses is that the numerous current is drawn by the shunt a part of the LCL filter. This additional reduces the efficiency of the CHBI.However, one among the foremost benefits of the planned theme is that the voltage across and thus the current through the shunt a part of the LCL filter, is greatly reduced. This reduction in the shunt current considerably whereas planning a damping resistor within the proposed methodology. For C = 10 μF and fres = 2400Hz, the reactance offered by C at f_{res} is 6.63 Ω. Here, a 15-Ω resistance is chosen, that provides satisfactory resonance damping.

3) *Design of Series capacitor C_{se}*: The most criterions for Designing of C_{se} is that it ought to offer an occasional impedance path for the fundamental frequency current element [17].

$$I_f^1 = \frac{V_{inv1} - V_{t1}}{R_f + \mathrm{j}(X_{f12} - X_{se1})} \qquad (11)$$

It was ensured that the shunt condenser C can offer a high impedance path for the lower order harmonics. Therefore, a negligible fundamental current drawn by C and might be neglected at the fundamental frequency. Therefore, the elemental current equipped by the filter whereas considering R1, L1, R2, L2, and C_{se} as series connected is given as

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Wherever R_f = R1 + R2, $X_{f12} = \omega_1(L1 + L2)$, $Xse_1 = 1\omega_1 Cse$, and Vt1 is that the fundamental rms PCC voltage. The voltage $V_{inv1}$is the fundamental rms voltage per phase obtainable at the CHBI terminal and is given as [29]

$$V_{inv1} = \frac{V_{dc}}{\sqrt{2}} \qquad (12)$$

After simplification equation (12) becomes

$$I_f^1 = \frac{(V_{inv1} - V_{t1})R_f - j(V_{inv1} - V_{t1})(X_{f12} - X_{se1})}{R_f^2 + (X_{f12} - X_{se1})^2} \qquad (13)$$

Interfacing resistances are terribly tiny compared with reactive part and may be neglected. Therefore, the imaginary part of a complex number magnitude of I^1_f is

$$\mathrm{Im}\left[I_f^1\right] = -\frac{V_{inv1} - V_{t1}}{X_{f12} - X_{se1}} \qquad (14)$$

It may be discovered from eq (14) that to inject reactive current from the compensator to the PCC, the fundamental rms voltage per phase is possible at the CHBI terminal (i.e., dc-link voltage) must be abundantly larger than the terminal voltage. Otherwise, the compensation performance won't be satisfactory. In the traditional topology wherever the series capacitor is absent, the maximum injected current solely depends upon the dc-link voltage (since V_{t1} and X_{f12} are fixed). Therefore, the dc voltage is maintained at a far higher price as compared with the terminal voltage. Insertion of the condenser nonparallel with the interfacing LCL filter ends up in the reduction of the entire impedance provided by the compensator that is additionally evident from eq (14).

Therefore, the dc-link voltage may be reduced from its reference price for an equivalent reactive current injection. Hence, the worth of the series condenser depends upon the most reactive filter current and to the extent that the decrease in the dc-link voltage is needed. The most reactive current that a compensator will offer should be an equivalent as that of the maximum load reactive current to attain unity power factor at the load terminal. The load current are maximum when it will supply minimum impedance at full load, i.e,($Z_{lmin} = R_{lmin} + jX_{lmin}$). Therefore, the maximum fundamental current drawn by the load in a very specific phase is given as

$$I_{lmax} = \frac{V_{t1}}{R_{1min} + jX_{lmin}} \qquad (15)$$

Calculating the imaginary load current magnitude from the preceding equation (15) and equating with (14)

$$\frac{V_{t1}X_{lmin}}{Z_{lmin}^2} = \frac{V_{inv1} - V_{t1}}{X_{f12} - X_{se1}} \qquad (16)$$

A more generalized expression can be written as

$$I_{lmax}\sqrt{1 - pf_{lmin}^2} = \frac{V_{inv1} - V_{t1}}{X_{f12} - X_{se1}} \qquad (17)$$

Where $I_{lmax}= V_{t1}/Z_{lmin}$, and $pf_{lmin}$is the minimum load power factor given by R_{lmin}/Z_{lmin}. Hence, Xse1 will be

$$X_{se1} = X_{f12} - \frac{V_{inv1} - V_{t1}}{I_{lmax}\sqrt{1 - pf_{lmin}^2}} \qquad (18)$$

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Table 1. Simulation Parameters.

System quantities	Values
Source voltage	230 V rms line to neutral, 50Hz
Feeder impedance	$Z_{s=}$ 1+j3.14Ω.
Linear load	Z_{la} = 30+j62.8Ω,Z_{lb} = 40+j78.5Ω,Z_{lc} = 50+j50.24Ω,
RC nonlinear load	R_l= 50 Ω, C_l =1000μF.
RL nonlinear load	R_l= 50 Ω, L_l=200mh.
VSI parameters(Traditional topology)	V_{dc} = 520V, C_{dc}=3000 μF, R_f= 50 Ω, L_f =0.1mh.
VSI parameters(LCL Filter)	V_{dcref}=520V,C_{dc}=3000μF,L_1=6.5mh,L_2=1mh,C=10μF, R_d= 15 Ω,R_1= R_2= 0.05 Ω.
VSI parameters(Proposed topology)	V_{dcref}=110V,C_{dc}=300,μF,L_1=1.5mh,L_2=0.6mh,C=10μF, R_d= 15 Ω,R_1 = R_2= 0.05 Ω,C_{se}=50 μF.
CHBI parameters(Proposed topology)	V_{dcref} =110V,C_{dc}=3000 μF, L_1=1.5mh,L_2=0.6mh, C=10μF,R_d= 15 Ω,R_1 = R_2= 0.05 Ω,C_{se}=50 μF.
Hysteresis Band(h)	+ or - 0.5A
PI Controller Gains	K_P =2, K_i =0.5

We can use eq (16) once the load impedances are glorious, whereas in sensible things, only nameplate information are accessible, and thus, eq (18) should be used. Supported the values given in Table 3, wherever phase-b needs the most reactive current having the minimum electric resistance, the worth of the series capacitor will be computed. For the given values, C_{se} is found to be 46.13 μF. For practical issues, Cse is taken as 50 μF.

V. SIMULATION RESULTS

The advantages of the projected topology are that it uses a lower rating of the CHBI, incorporates a smaller worth of the filter inductor, reduces the damping power loss, and provides improved current compensation. All these results are verified through simulation. System parameters accustomed validate the performance are given in Table 3. Fig. 5(a) shows the 3-phase source currents. These currents are unbalanced and distorted due presence of unbalanced linear and nonlinear loads.

The performance of the standard DSTATCOM topology is presented in Fig. 6. The 3-phase source currents, which are balanced and curved, are shown in Fig. 6(a). As seen from waveforms, the source currents and therefore contains switching frequency components of the VSI. The 3-phase filter currents are shown in Fig. 6(b). The waveforms of voltages across higher and lower dc capacitors, moreover as well total dc-link voltage, are given in Fig. 6(c). The voltage across every condenser is maintained at 520 V, whereas the overall dc-link voltage is maintained at 1040V mistreatment the PI controlled.

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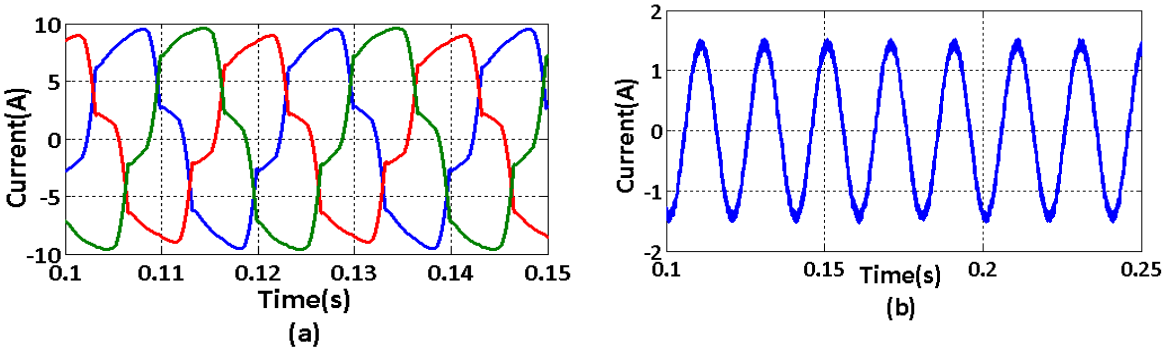

Figure 5. Simulation results without DSTSTCOM (a) Source Current (b) Neutral Current.

Fig.7.shows the compensation performance for LCL filter based DSTATCOM. The source currents are balanced and sinusoidal however contain variety switch harmonics ripple. Their percentage total harmonic distortions (THDs) are given in Table 5. To accommodate power losses in the damping resistor, the source currents are slightly accumulated compared with the normal topology. Moreover, the total dc-link voltage is maintained at 1040 V (same as the ancient scheme) to attain load compensation.

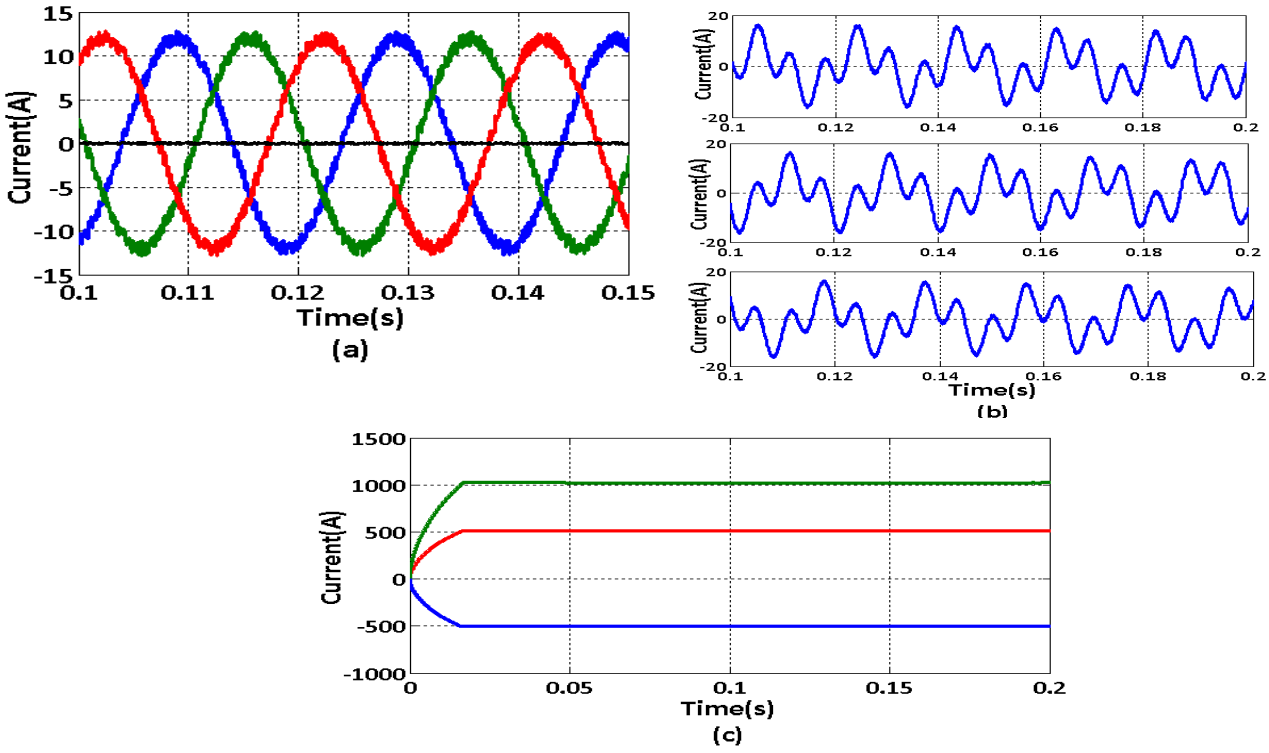

Figure. 6. Simulation results for traditional topology.(a)Source currents. (b) Filter currents (c) Voltages across the dc link.

The compensation performance of the proposed topology with VSI & CHBI is shown in Fig. 8.& Fig 11. The load and source parameters are the same as given in Table I. In Fig. 8(a), 11(a) the three-phase source current waveforms are shown, which are balanced, sinusoidal, and have negligible switching ripple compared with the traditional topology. In addition, neutral current is nearly zero. Additionally, source currents are in phase with their

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respective phase voltages. The filter currents, as shown in Fig. 8(b), 11(b) have smaller ripples as compared with that of the traditional topology. The voltages across each capacitor and the total dc-link voltage are shown in Fig. 8(c), 11(c) having maintained at 110 and 220 V, respectively.

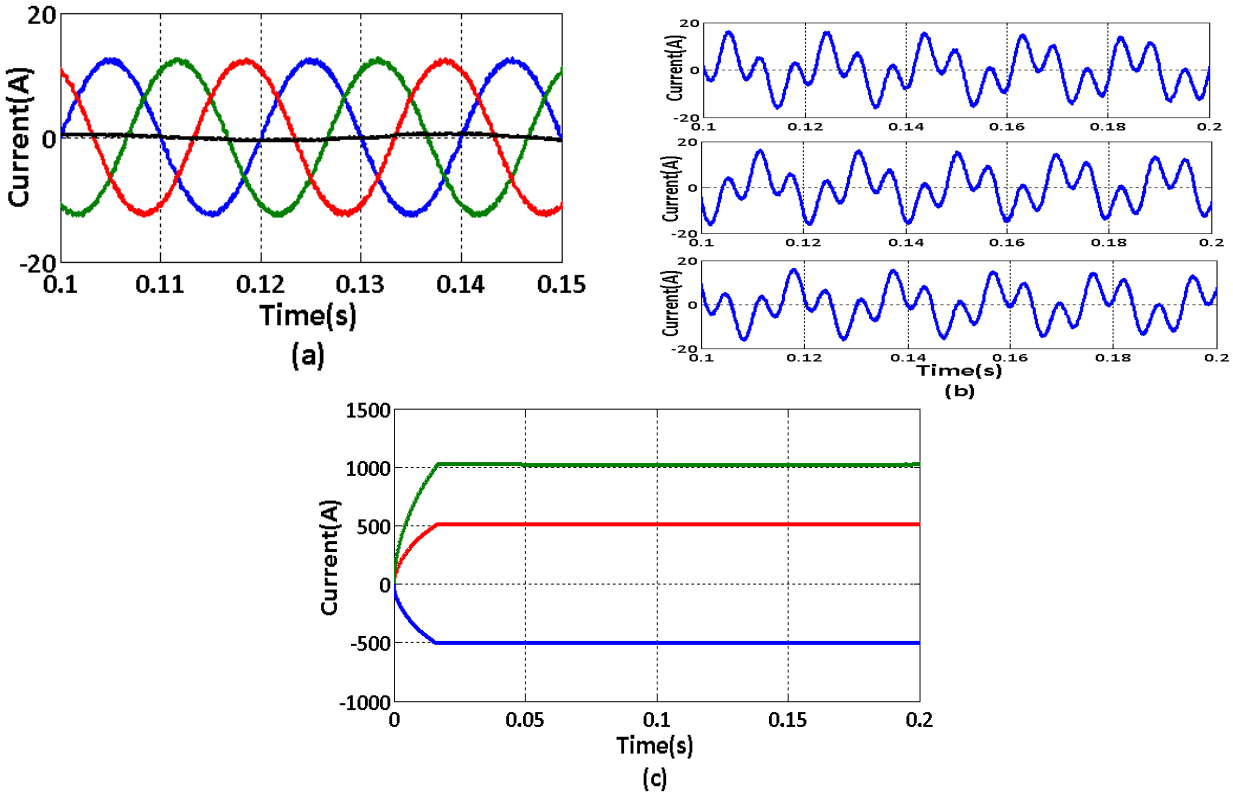
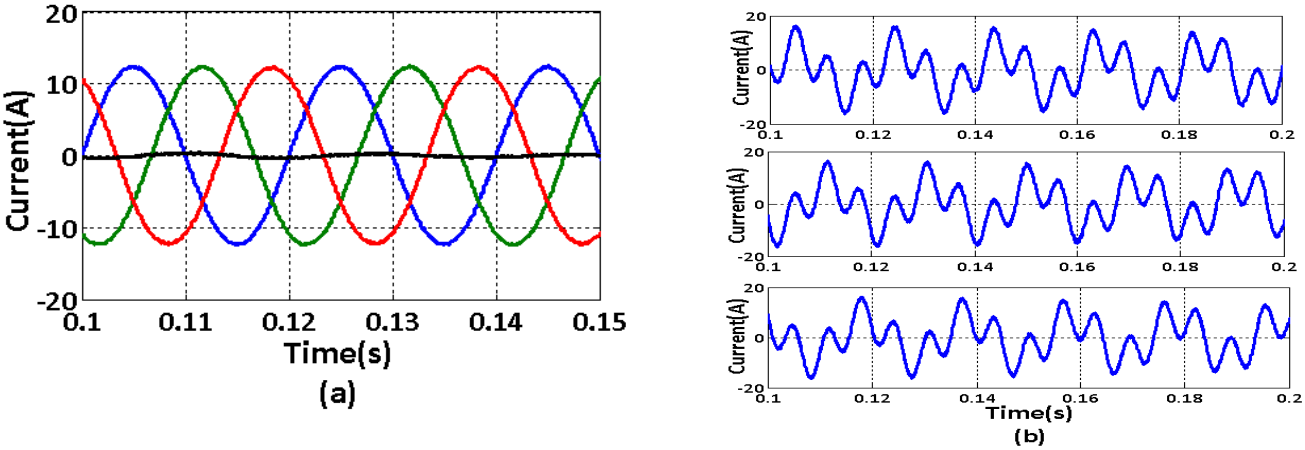


Figure. 7. Simulation results for DSTATACOM with the *LCL* filter. (a) Source currents. (b) Filter currents. (c) Voltages across the dc link.

The performance of the proposed topology is compared with traditional DSTATCOM topologies, and corresponding percentage THDs in currents are illustrated in Table 5. It is clear from Table 5 that the percentage THDs in three-phase source currents considerably lesser in the proposed topology.



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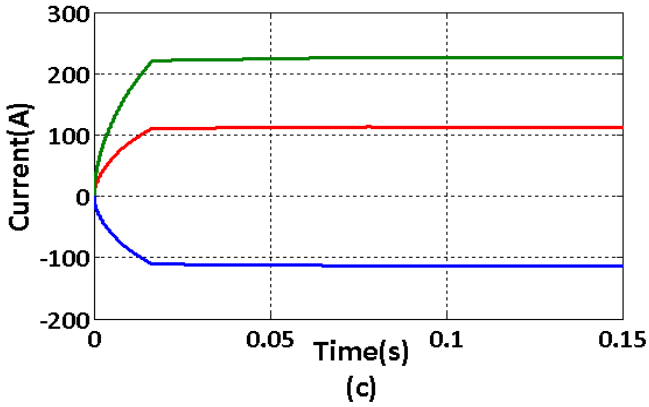


Figure.8.Simulation results with the proposed topology using VSI.(a) Source currents. (b) Filter currents. (c) Voltages across the dc link.

Moreover, these confirm that the reduced dc-link voltage is sufficient for the DSTATCOM to achieve its current compensation performance. Comparative analysis of Inverter parameters in terms of dc-link voltage, total filter inductance is presented in Table 4.

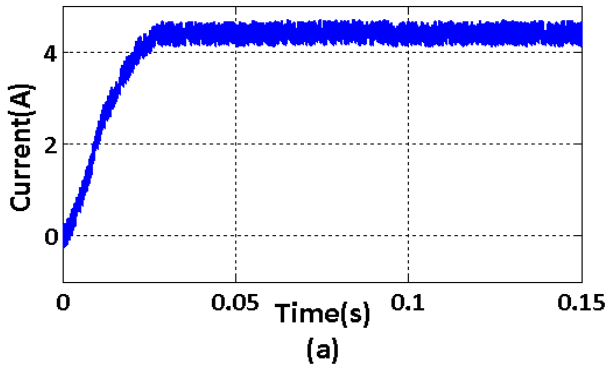
Furthermore, the performance of the planned topology with the RC-type nonlinear load is shown in Fig.10. The source currents are sinusoidal with a negligible harmonic component, Again, the overall dc-link voltage is maintained at 220 V (110 V across every capacitor). This confirms that the reduced dc-link voltage is comfortable to compensate the RC-type nonlinear load effectively.

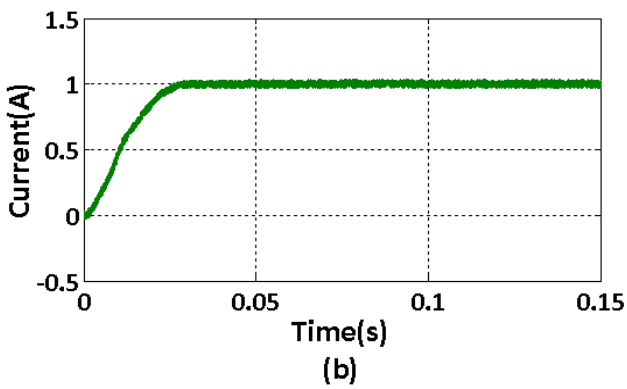
(a). *Reduction dc link voltage Rating*

The power rating of DSTATCOM, i.e., SC, is given as [21].

$$S_C = \sqrt{3}\,\frac{V_{dc}}{\sqrt{2}}\,I_{f1} \qquad (19)$$

The dc bus voltage demand has been reduced from 520to 110 V. The term If1 represents the rms current provided by the IGBT switch. Within the ancient DSTATCOM topology, the rms worth of If1 are a similar as that of the rms reactive and harmonics element of the load current. Within the following section, it is seen that the current drawn by the shunt branch of the LCL filter isn't abundant. Hence, these ratings of the IGBT switch in each topology are about the same.





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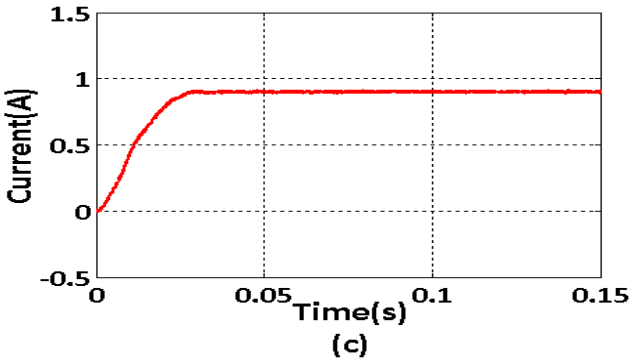

Figure. 9. Damping current.(a)With the *LCL* filter. (b) Proposed topology with VSI(c) Proposed topology with CHBI.

Therefore, the ratio of the power rating of the planned topology S_{CP} to the normal topology S_{CT} are the power rating of the planned topology are only 21.15% of the normal topology. The reduction in size of passive components and power rating can lead to higher potency, less switching ripple, and electromagnetic emissions.

$$\frac{S_{CP}}{S_{CT}} = \frac{110}{520} = 0.2115 \qquad (20)$$

Moreover, this through the shunt capacitance within the planned topology is reduced compared with the LCL filter-based DSTATCOM topology. It additional reduces the facility rating of the planned topology as compared with the LCL filter-based DSTATCOM.

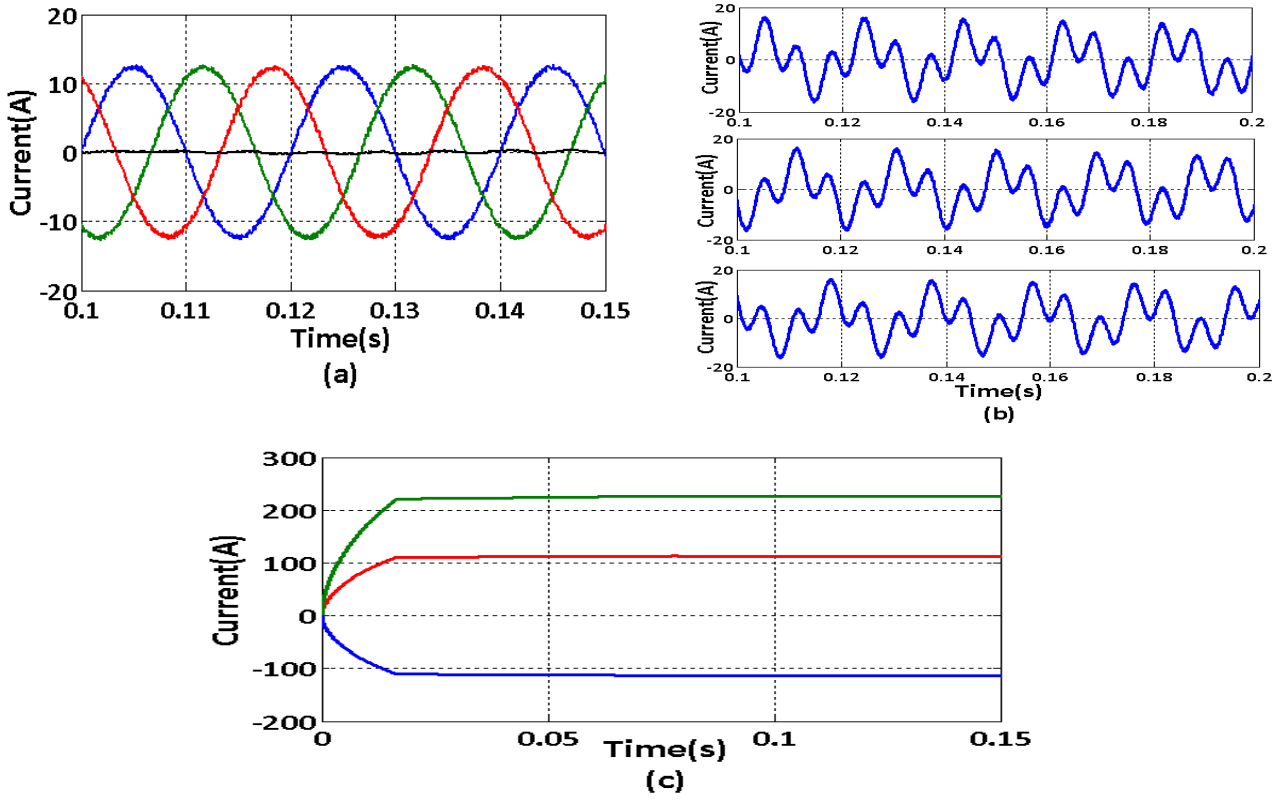

Figure.10. Simulation results for the proposed topology Using VSI with the *RC*-type nonlinear load.(a)Source currents.

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(b) Filter currents. (c) Voltages across the dc link

(a) Reduction in Damping Power Loss and its Effects

Passive damping is straight forward to implement and provides sensible resonance elimination capability; this additionally ends up in additional power loss within the damping resistor. However, in industrial applications where the necessities are to possess the minimum range of sensors with the smallest amount complex algorithm, passive damping is preferred whereas exceptive the power loss. The current through the damping resistor depends upon the voltage across the shunt a part of the LCL filter. Within the planned scheme, the dc-link voltage has been greatly reduced. Therefore, the voltage at the shunt a part of the LCL filter will scale back significantly. It'll scale back the current flowing through the damping resistor and, therefore, damping power also. Fig. 9(a) shows the filter current in phase-a when only LCL filter-based DSTATCOM is employed. The steady-state rms price of current within the damping resistor is found to be 4.5 A. The power loss within the damping resistor is obtained as follows:

$$P_{loss1} = 3 * R_d * I_{sh}^2 = 3 * 4.5^2 * 15 = 911.25W \qquad (21)$$

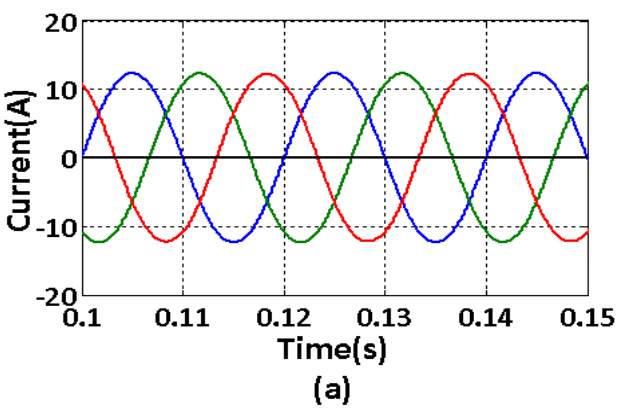
Fig. 9(b), 9(c) shows the current through the damping resistor in the projected DSTATCOM topology. The effect of reduced dc-link voltage (110 V during this case) will be clearly seen from the steady-state rms damping current, that is reduced to 1.05 A. the power loss will be computed as follows:

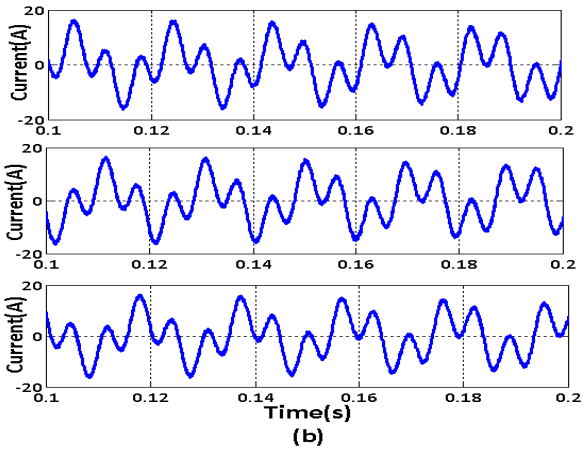
$$P_{loss2} = 3 * 1.05^2 * 15 = 48.61W \quad \mathbf{(22)}$$

The damping resistor power loss ratio of the projected DSTATCOM topology and therefore the DSTATCOM with only the LCL filter will be calculated as follows:

$$\frac{P_{loss2}}{P_{loss1}} = \frac{48.61}{911.25} = 0.0533 \qquad (23)$$

The damping power loss within the projected topology is merely 5.33% as compared with the DSTATCOM using the LCL filter. It leads to higher potency of the CHBI. The decrease in shunt capacitor current causes the decrease within the current supplied by the CHBI.Therefore, the loss within the CHBI and therefore the reactive power losses within the shunt capacitor and L_1 can decrease. Damping power loss is remunerated by drawing real power from the supply. Reduction in damping loss ensures that the supply currents are reduced.





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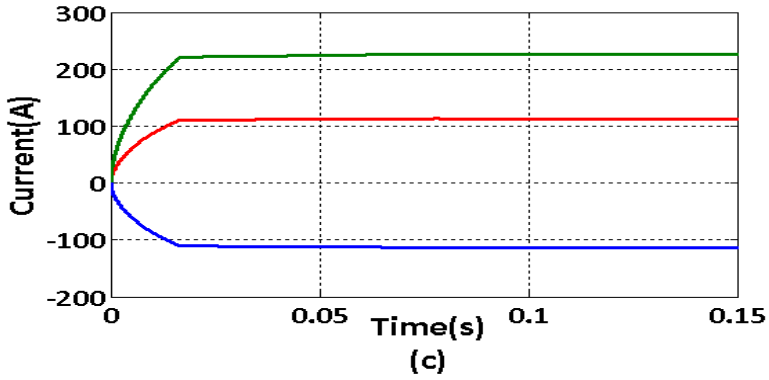

Figure.11.Simulation results of DSTATCOM with proposed topology using CHBI.(a) Source currents. (b) Filter currents. (c) Voltages across the dc link.

Table.4.Comparision of Inductor Parameter

DSTATCOM Topology	Inductance value	Voltage at dc link
Traditional With VSI	26mH	1040V
LCL FILTER With VSI	7.5mH	1040V
Proposed Topology With VSI	2.1mH	220V
Proposed Topology With CHBI	2.1mH	220V

Fig 12 shows the graphical representation of the % THD's with different compensation techniques by this comparison we can clearly understand the level of variation that had come over with different compensation technique's all these are recorded under extensive computer simulation under MATLAB Simulink (version 2009a).

Table.5. Comparison of % THD's with different compensations

System Configurations	% THD of Source current
Without Compensation	15.78
Using traditional Topology	5.78
Using LCL FILTER	2.68
Using Hybrid Topology	1.27
Using Hybrid Topology with RC-load	1.24
With cascaded H-Bridge	0.90

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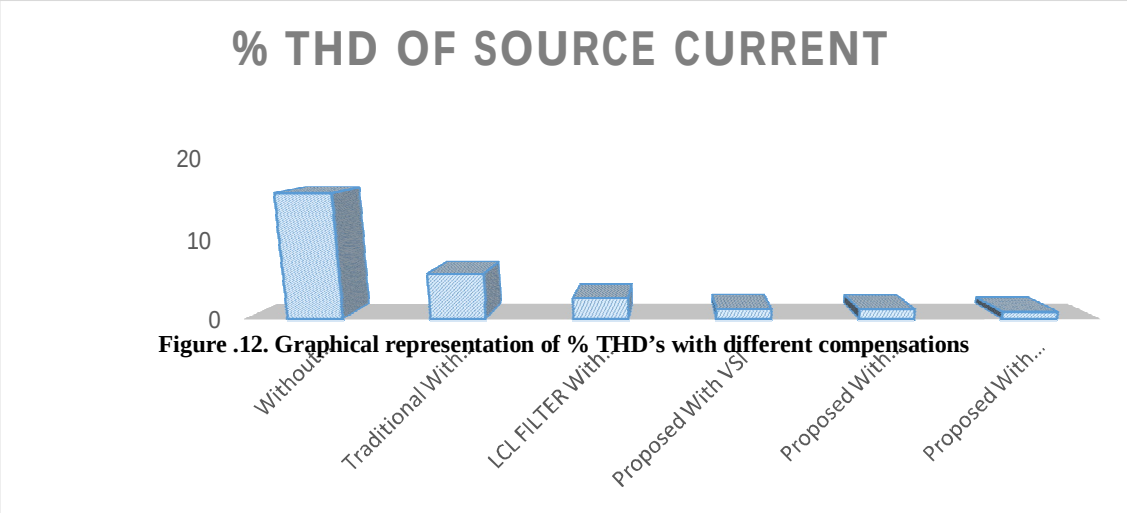

Figure .12. Graphical representation of % THD's with different compensations

VI. CONCLUSION

In this paper, design and operation of an improved hybrid DSTATCOM topology using CHBI is proposed to compensate reactive and harmonics loads. The hybrid interfacing filter used here consists of an LCL filter followed by a series capacitor. This topology provides improved load current compensation capabilities while using reduced dc-link voltage and interfacing filter inductance. Moreover, the current through the shunt capacitor and the damping power losses are significantly reduced compared with the LCL filter-based DSTATCOM topology. These contribute significant reduction in cost, weight, size, and power rating of the traditional DSTATCOM topology. Effectiveness of the proposed topology has been validated through extensive simulation.

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