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Simulation of an Efficient Cascaded Inverter with Reduced Number of Switches and Comparison of THD for Various Voltage Levels

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ABSTRACT: Multilevel inverter has gained popularity in various fields like photovoltaic systems, HVDC systems, FACTS devices, industrial drives etc. It has numerous advantages like lower harmonics, low switching losses, low stress on switches etc. There are different topologies available like neutral point or diode clamped inverter, flying capacitor inverter etc. each having its own advantages and disadvantages. The efficiency of this inverter is greatly improved by reducing the number of switches of inverter. The paper takes into account a cascaded topology to reduce the number of switches. To find the effectiveness of the cascaded topology in improvement of efficiency, a simulative study is done to evaluate the effect of topology with increasing voltage levels. Simulations are done in MATLAB.

KEYWORDS: Cascaded H bridge inverter, Multilevel diode clamped inverter, Multilevel Flying Capacitor Inverter, Total harmonic distortion.

I.INTRODUCTION

The Inverter is simply an electrical device which converts Direct Current (DC) to Alternate Current (AC).Well that being said, now we have lots of possibilities for this conversion. We have a variety of semiconductor configurations which have aided in the development of better waveforms in terms of quality and shape. Multilevel inverters have evolved from simple inverters to produce waveforms which are more AC like.The AC output could better approximate a sine wave, if more than two voltage levels were available to the inverter output terminals.Advantages of multilevel inverters are that they improve the output waveform quality greatly by reducing the harmonic distortion, they can work with higher or lower switching frequency than the fundamental frequency and reduce the stress on switches as they produce common mode voltage. Disadvantages of multilevel inverter are that they often use a large number of semiconductor switches making the system more bulky and costly. Also they require separate gate drive circuit for each switch. The most familiar use of inverter is for emergency backup power in a home. It has wide applications in HVDC system, FACTS devices, Industrial drives etc.

This paper focusses on an energy efficient configuration which can act as an effective replacement for existing topologies due to its main advantage of reduced number of switches. Reduced number of switches means reduction in driver circuit, better voltage levels, improvement in size,space,cost and thereby betterment of efficiency of inverter. This paper analyses the effectiveness of cascaded topology in improvement of efficiency. It can be used in photovoltaic applications. The configuration with reduced number of switches is analysed using Matlab-simulink.The following section discusses the various configurations used and later sections describes one particular topology which is of interest to reduce number of switches and presents simulative analysis using this topology with various voltage levels.

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II. DIFFERENT CONFIGURATIONS

1. Multilevel Diode Clamped/Neutral Point Inverter

One of the first configuration utilized in inverter applications is the multilevel diode clamped inverter. The inverter provides multiple voltage levels through connection of the phases to a series bank of capacitors. The advantage of this configuration is that diode transfers only a limited amount of voltage, thereby reducing the stress on other electrical devices. Also half of the input DC voltage is the maximum output voltage. This type of inverter gives high efficiency because the fundamental frequency is used for all the switching devices and it is a simple method, especially for back to back power transfer systems. The disadvantages of this configuration is it requires more number of clamping diodes is when number of output voltage level is high making it larger in size, cost and design. [4], [5].

2. Multilevel Capacitor Clamped/Flying Capacitor Inverter

In order to make the inverter more efficient another configuration was developed eventually. It uses capacitors instead of using clamping diodes to hold the voltages to the desired value. The main concept of this inverter is to use capacitors instead of diodes. For higher levels use of filter becomes necessary. The output is half of the input DC voltage just as in previous configuration. It is the main drawback of the flying capacitor multi-level inverter. It can control both the reactive and active power flow. But due to the high frequency switching, switching losses will be a disadvantage. Control and cost of system also becomes difficult with increase of voltage levels. Capacitor Clamped Multi level Inverter are widely used in induction motor control, FACTS devices, converters etc. [6], [7].

3. Cascaded Multicell Inverter, CMCI

Cascaded multilevel inverter is one of the most important and popular topology in the family of multilevel inverters. Multilevel inverters using this configuration do not need a coupling transformer to interface it with high power system. The cascaded H-bride multi-level inverter may use capacitors and switches and requires less number of components in each level which can be easily replicated. This topology consists of series of power conversion cells and power can be easily scaled and multiplied. The combination of capacitors and switches pair is called an H-bridge and requires separate input DC voltage for each H-bridge.One of the advantages of this type of multi-level inverter is that it needs less number of components compared with diode clamped and flying capacitor inverters making it more desirable. The price and weight of the inverter are less than those of the two inverters discussed before. Soft-switching is possible by some of the new switching methods which will reduce the losses. [1],[2],[3],[9].

4. Advanced H-bridge type inverter

Another configuration developed to compensate for the disadvantages is advanced H-Bridge configuration. Therefore at higher levels the overall cost and complexity of system reduces.This topology separates the circuit into two parts, one part is called level generation part and is used for generating output voltage levels in positive polarity. Level generation part requires high frequency switches to generate the required levels at the right time. The second part is named polarity generation part and is used for generating the negative polarity of the output voltage. This part is the low-frequency part and operating at line frequency or supply frequency.The main disadvantage is it uses isolated DC sources just as in cascaded topology. It should be noted that isolated power supplies avoid voltage balancing problems created by capacitors in previous two configurations. Advantages are that they have lesser number of switches compared to previous configurations and better harmonics elimination. Other disadvantages is that the system is bulky and need more space and is costly [1],[9], [8].

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5. Cascaded topology to reduce number of switches

Table 1. Switching States

State	Switch States					
	S_1	S_2	S_3	S_4	S_4	V_0
1	off	off	off	off	on	0
2	on	off	on	on	off	$V_1 + V_3$
3	on	on	on	on	off	$V_1 + V_2 + V_3$

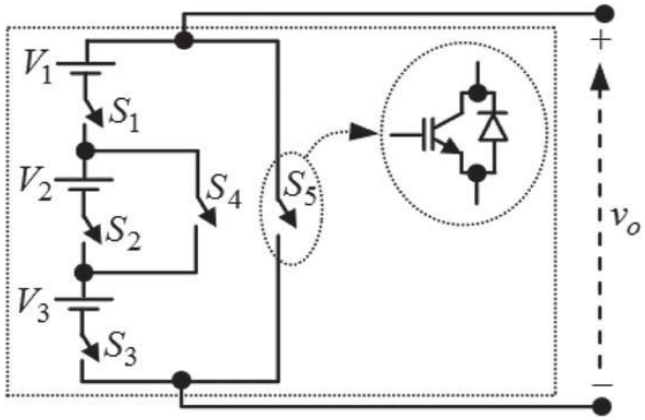

Figure 1: Basic unit of cascaded inverter [1]

An inverter topology has been used which has superior features over conventional topologies in terms of the required power switches and isolated DC supplies, control requirements, cost, and reliability. The basic unit for the cascaded multilevel inverter used is shown in Fig 1.The switching states for this unit is shown in Table 1. By the series connection of several basic units, a cascaded multilevel inverter that only generatespositive levels at the output is utilised. Therefore, an H-bridge is added to the proposed inverter to generate all voltage levels that is positive levels and negative levels. This inverter is called the developed cascaded multilevel inverter for convenience. By changing the magnitude of the dc voltage sources, we get different voltage levels at the output.

The developed proposed inverter has better performance and needs minimum number of power electronic devices that lead to reduction in the installation space and total cost of the inverter. It can be studied for various voltage levels by changing the magnitude of DC voltage sources. Next section discuss the details of this better topology to improve efficiency [9], [1].

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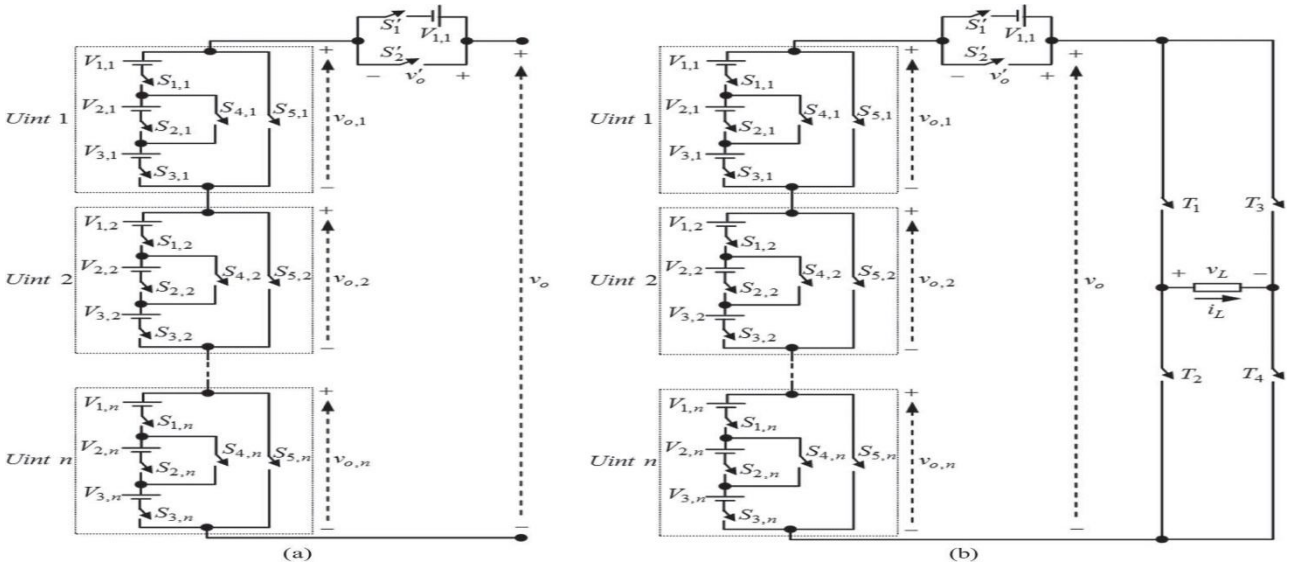

Figure 2: (a)n level cascaded topology (b)n level developed cascaded topology

III. CASCADED TOPOLOGY TO REDUCE SWITCH NUMBER

To overcome the disadvantages of conventional topologies, developed cascaded topology discussed above is used. As shown in Fig 1 the basic unit is comprised of three dc voltage sources and fiveunidirectional power switches. Fig 3 shows

v_o	S'_1	S'_2	$S_{1,1}$	$S_{2,1}$	$S_{3,1}$	$S_{4,1}$	$S_{5,1}$	$S_{1,2}$	$S_{2,2}$	$S_{3,2}$	$S_{4,2}$	$S_{5,2}$	⋯	$S_{1,n}$	$S_{2,n}$	$S_{3,n}$	$S_{4,n}$	$S_{5,n}$
0	off	on	off	off	off	off	on	off	off	off	off	on	⋯	off	off	off	off	on
V_1	on	off	off	off	off	off	on	off	off	off	off	on	⋯	off	off	off	off	on
$V_{1,1}+V_{3,1}$	off	on	on	off	on	on	off	off	off	off	off	on	⋯	off	off	off	off	on
$V_{1,1}+V_{2,1}+V_{3,1}$	off	on	on	on	on	off	off	off	off	off	off	on	⋯	off	off	off	off	on
$V_{1,2}+V_{3,2}$	off	on	off	off	off	off	on	on	off	on	on	off	⋯	off	off	off	off	on
$V_{1,2}+V_{2,2}+V_{3,2}$	off	on	off	off	off	off	on	on	on	on	off	off	⋯	off	off	off	off	on
$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,3}$	off	on	on	on	on	off	off	on	off	on	on	off	⋯	off	off	off	off	on
$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,2}+V_{2,3}$	off	on	on	on	on	off	off	on	on	on	off	off	⋯	off	off	off	off	on
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$\sum_{j=1}^{n}(V_{1,j}+V_{2,j}+V_{3,j})$	off	on	on	on	on	off	off	on	on	on	off	off	⋯	off	off	off	off	on
$V_{1,1}+\sum_{j=1}^{n}(V_{1,j}+V_{2,j}+V_{3,j})$	on	off	on	on	on	off	off	on	on	on	off	off	⋯	off	off	off	off	on

Figure 3: Generated output voltage levels based on states of power switches [1]

the voltage values and corresponding switching states.As this inverter is able to generate all voltage levels except V_1, it is needed to use an additional dc voltagesource with the amplitude of V_1 and two unidirectional switches that are connected in series with the cascaded topology. The developed cascaded inverter that is able to generate all levels is shown in Fig 2 (b). In this inverter, power switches S1 and S2 and DC voltage source have been used to produce the lowest output level V_1. The amplitude of this dc voltage source V_{dc} is considered $V_1 = V_{dc}$ which is equal to the minimum output level. The output voltage level of each unit is indicated by V_{01},V_{02}.,V_{03}…..V_{0n}.

The generated output voltage levels of the cascaded inverter are shown in Table 2. As aforementioned and according to Table 2, the cascaded inverter is shown in Fig 2 (a) is only able to generate positive levels at the output. Therefore, an H-bridge with four switches is added to the cascaded topology. This inverter is called the developed cascaded multilevel inverter and is shown in Fig. 2(b). If switches T1 and T4 are turned on, load voltage V_L.is equal to $+V_0$ and if power

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switches T2 and T3 are turned on, the load voltage will be $-V_0$.As unidirectional power switches are used in the developed cascaded multilevel inverter, the number of power switches is equal to the numbers of IGBTs, power diodes, and driver circuits. Another main parameter in calculating the total cost of the inverter is the maximum amount of blocked voltage by the switches. If the values of the blocked voltage by the switches are reduced, the total cost of the inverter decreases as is obtained using this configuration[1].

III.SIMULATIVE ANALYSIS AND COMPARISON OF DEVELOPED CASCADED TOPOLOGY FOR VARIOUS LEVELS

9 level,11 level, and 15 level inverter using the above discussed cascaded topology was done. Results are shown in Table III.Simulations were done in Matlab.Figures 8 to 10 shows the voltage output waveforms of nine level, eleven level, fifteen level, nineteen level and twenty one level inverter along with FFT report.

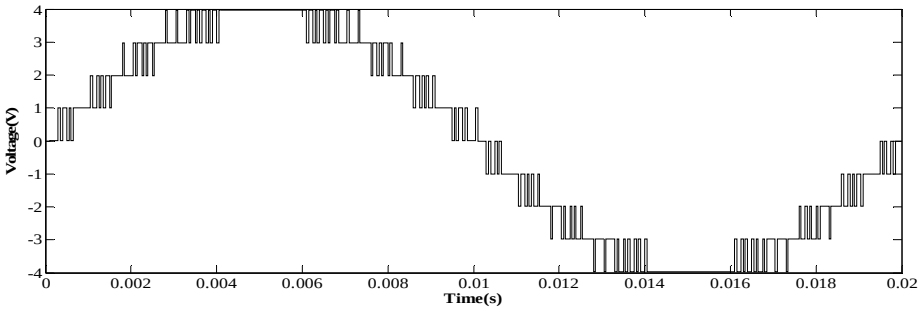

Fig 8(a): Nine level output waveform

Figure 8(a) shows the outputwaveform for nine level cascaded inverter configuration.

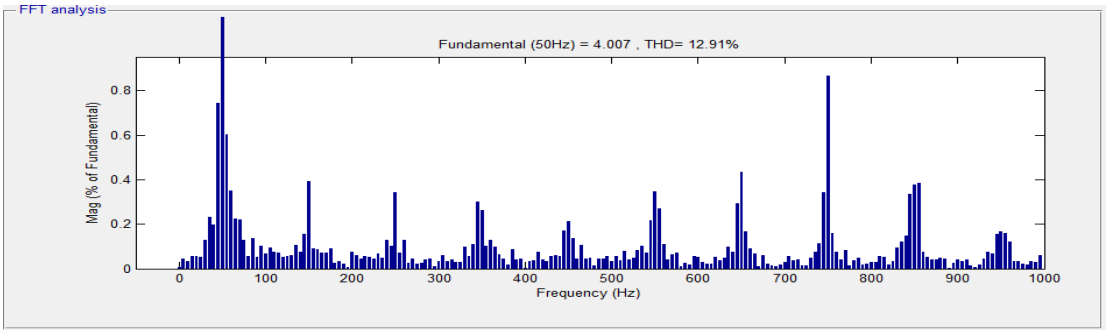

Fig 8(b): Nine level output THD

Figure 8(b) shows the THD report for nine level cascaded inverter configuration.

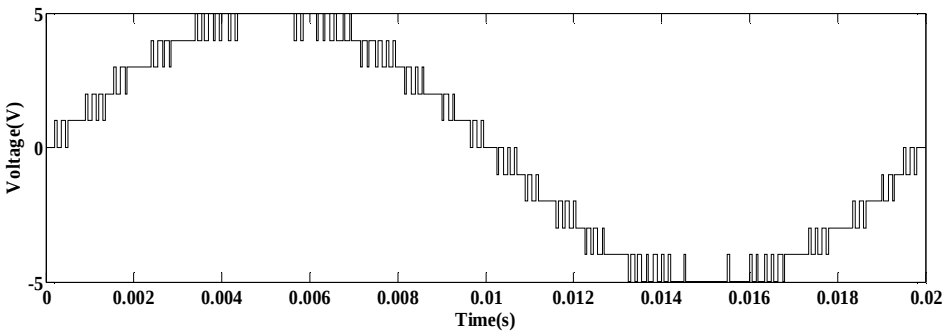

Fig 9(a): Eleven level output waveform and THD

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Figure 9(a) shows the output waveform for eleven level cascaded inverter configuration.

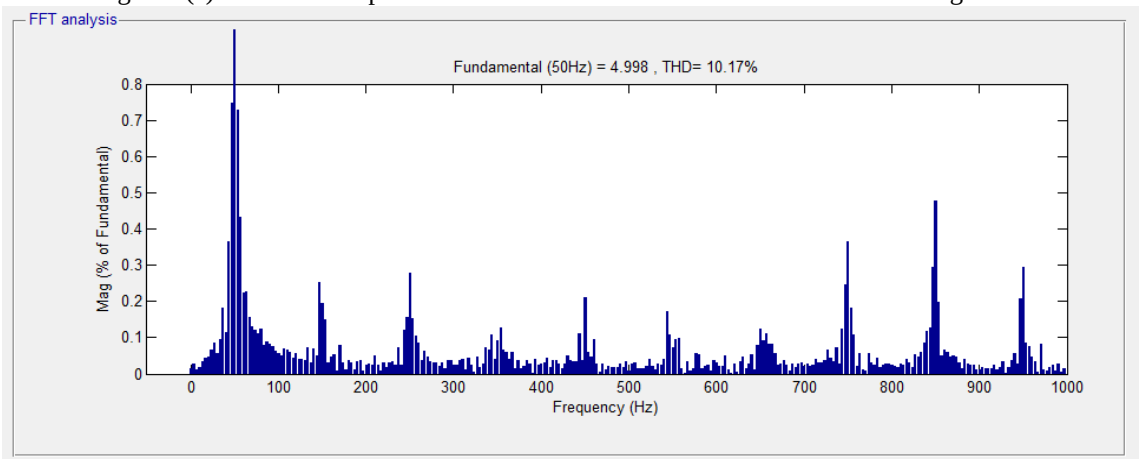

Fig 9(b):Eleven level output THD

Figure 9(b) shows the THD report for eleven level cascaded inverter configuration.

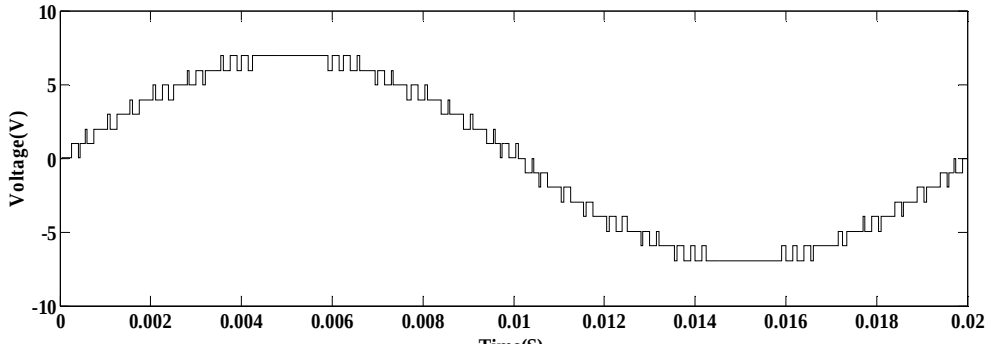

Figure10(a) Fifteen level output waveform and THD

Figure 10(a) shows the output waveform for fifteen level cascaded inverter configuration.

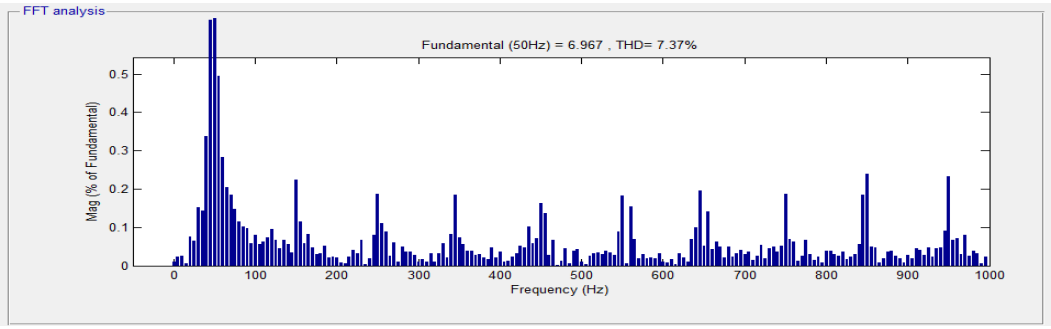

Figure10(b) Fifteen level output waveform and THD

Figure 10(b) shows the THD report for fifteen level cascaded inverter configuration.

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Table III: THD values for different voltage levels

Inverter	THD level
9-level	12.91
11-level	10.17
15-level	7.37

The table III shows the variation of THD with different voltage levels .As can be clearly seen from the table the THD value decreases with increasing voltage level. The load used in this analysis is a simple R load.

III.CONCLUSION

Multilevel inverters have been used in many industrial applications like HVDC, FACTS, PV systems, UPS and Industrial drive applications. Instead of using other inverter topology, proposed topology is better for all these applications because it has less control complexities, less size and cost. It also reduces the THD of output to a great extend thus reduces the size of filter. As the level increases THD of Output reduces. It can be used in applications where quality of output is primary requirement. The simulation results shows the improvement of quality of voltage waveform as voltage level increases.

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