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FPGA Implementation of a High Speed Matrix Multiplier for Use in Signal and Image Processing Applications

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ABSTRACT: The evolution of computer and internet has brought demand for powerful and high speed data processing, but in such complex environment fewer methods can provide perfect solution. Parallel Computing is a solution to handle above address issue. This will provide solution for the address issue of demand for high speed data processing. An effective implementation of the matrix multiplication using systolic architecture on reconfigurable systems (RS) like field programmable gate arrays (FPGA) is demonstrated. The systolic architecture increases the computing speed by combining the concept of parallel processing and pipelining into a single concept. The RTL code is written for matrix multiplication with systolic architecture and matrix multiplication without systolic architecture in Verilog HDL, compiled then finally the designs are compared to each other to evaluate the performance of the architecture. The Matrix Multiplication with systolic architecture will enhance the speed of matrix multiplication by twice of conventional method. Replacing PE (Processing element) by an efficient MAC in terms of speed, reduced complexity and also power.

KEYWORDS: *Systolic* Array Architecture, Processing Element, MAC Unit, Reconfigurable System, Matrix Multiplication.

I. INTRODUCTION

Earlier, the major concerns of the VLSI engineers were area, performance, Speed, cost and reliability. In computer architecture, a systolic architecture is a pipelined network arrangement of Processing Elements (PEs) called cells. It is a specialized form of parallel computing, where cells compute the data which is coming as input and store them independently. A systolic architecture is an array composed of matrix-like rows of cells. Here, the Processing Elements is similar to central processing units (CPUs) (except for the usual lack of a program counter, instruction register, control unit etc. since operation is transport-triggered, i.e., sensitive to arrival of a data object across it).Each cell shares the information with its neighbors immediately after processing. The systolic array is often rectangular where data flows across the array between neighbor Data Processing Units (DPUs), often with different data flowing in different directions. Systolic architecture is arrays of DPUs which are connected to a small number of nearest neighbor DPUs in a mesh-like topology. DPUs perform a sequence of operations on data that flows between them. In this research, DPU performs the Multiplication and Accumulation (MAC) and the systolic array concept is used for multiply the matrices to enhance its computation speed [1]. There will be demand for powerful and high speed data processing in the evolution of computer and internet. Only fewer methods can provide perfect solution in such complex environment. The issue is handled by parallel computing. Among different fields, we concentrate image and signal processing applications in which high speed matrix multiplication plays a role. We need a high-performance, special-purpose computer system to meet specific application. I/O and computation imbalance is a notable problem. The concept of Systolic architecture can map high-level computation into hardware structures Systolic system works like an automobile assembly line. Systolic system is easy to implement because of its regularity and easy to reconfigure. Systolic architecture can result in cost effective, high- performance special-purpose systems for a wide range of problems [3]. For every clock cycle all systolic processors are activated and the multiplication and addition operations

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are performed on matrix elements. Partial results are accumulated in a register array. Once the pipeline is completely filled, results are available and they are fed to output registers in row wise manner [2].

A run-time reconfigurable multiply-accumulate (MAC) architecture can be easily reconfigured to trade bitwidth for array size (thus maximizing the utilization of available hardware); process signed-magnitude, unsigned or 2's complement data; make use of part of its structure or adapt its structure based on the specified throughput requirements and the anticipated computational load [4]. The proposed architecture consists of a reconfigurable multiplier, a reconfigurable adder, an accumulation unit, and two units for data representation conversion and incoming and outgoing data stream transfer [14]. Reconfiguration can be done dynamically by using only a few control bits and the main component modules can operate independently from each other. We need a high-performance, special-purpose computer system to meet specific application. I/O and computation imbalance is a notable problem. The concept of Systolic architecture can map high-level computation into hardware structures. Systolic system works like an automobile assembly line [5]. Systolic system is easy to implement because of its regularity and easy to reconfigure. Systolic architecture can result in cost-effective, high-performance special-purpose systems for a wide range of problems.

II. LITERATURE REVIEW

a) Basic principle of systolic architecture

Systolic system consists of a set interconnected cells, each capable of performing some simple operation. Systolic approach can speed up a compute-bound computation in a relatively simple and inexpensive manner [12]. A systolic array in particular, is illustrated below. (We achieve higher computation throughput without increasing memory bandwidth).

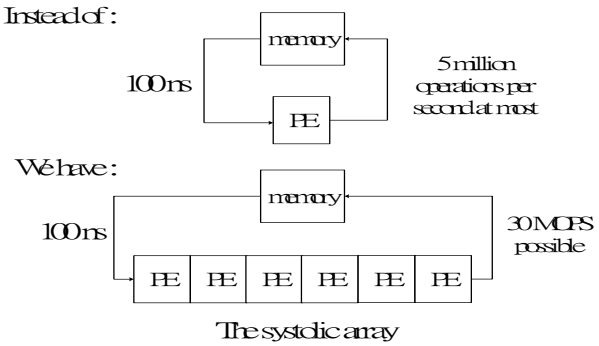

Figure1. Basic principle of systolic architecture

b) Systolic Array Architecture for Matrix Multiplication

A systolic architecture is an arrangement of processors i.e. PEs in an array (AB2 Architecture in [6]) where data flows synchronously across the array between neighbors, usually with different data flowing in different directions. PE at each step takes input data from one or more neighbors (e.g. Left and Top), processes it and, in the next step, outputs results in the opposite direction (Right and Bottom) [8]. The Proposed two dimensional systolic Architecture is given in the Figure. The array architecture given above takes input data in parallel into first PEs in the array and processes the Multiplication and Accumulation on them and then outputs result to the next level PEs of array. Systolic arrays do not lost their speed due to their connection like any other parallelism [9]. Where, each cell (PE) is an independent Processor (CPU) and has its own registers and Arithmetic and Logic Units (ALUs) i.e. Multiplication and Accumulation unit. The cells share the information with their neighbors, after performing the necessary operations on the data. Systolic Array Architecture (SAA) for Matrix Multiplication is shown in the Figure 2. Where each cell takes inputs from left and top, multiplies them and accumulates in the local register which is inside the each PE. After N2 clock pulses the result would be stored in each PE. The proposed systolic array architecture needs N2 magnitude Multipliers, 2N magnitude Accumulators and 4N registers are needed to compute matrix multiplication where N is order of matrix.

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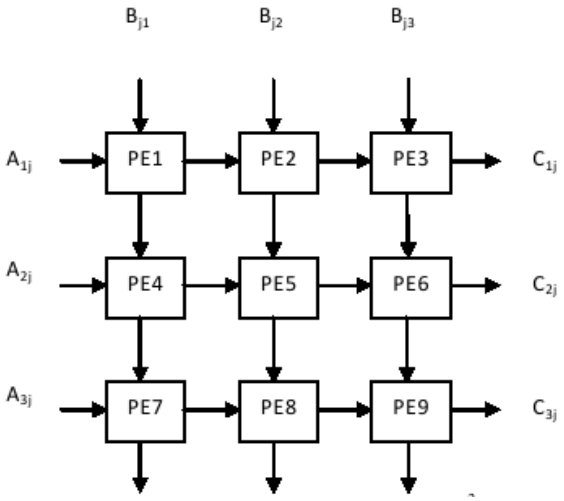

Figure2. Systolic Architecture for Matrix Multiplication

c) Parallel Matrix Multiplication Algorithms

The Singular Value Decomposition has been applied in a two dimensional adaptive FIR filtering technique. However, a two-dimensional adaptive algorithm based on a Singular Value Decomposition (SVD) method will be presented using systolic arrays that is applied in the area of image processing [11].The procedure may be implemented as a systolic array algorithm. The actual algorithm is to be combined out of partial linear algebra solutions presented above. Note that the array to perform singular value decomposition is almost identical to Eigen decomposition array. The simulation results show that the Wiener filtering principle can successfully be implemented in image restoration. Methods well known from the linear algebra theory that may be applied instead of classical methods based on Fourier transformation [10]. The effectiveness of the procedure may be improved using special updating techniques.

d) Reconfigurable MAC Unit

The proposed architecture consists of a reconfigurable multiplier, a reconfigurable adder, an accumulation unit, and two units for data representation conversion and incoming and outgoing data stream transfer [15]. Reconfiguration can be done dynamically by using only a few control bits and the main component modules can operate independently from each other. The architecture is composed mainly of three parts: a reconfigurable multiplication unit, a reconfigurable addition unit and an accumulation unit. The first two components are properly combined into a reconfigurable MAC unit, but they can function totally independent from each other. This ability is dependent on two configuration bits. The processor that will be presented here can operate 2 64-bit items, or 8 32-bit items, or 32 16-bit items, or 128 8-bit items, or 512 4-bit items, with items in unsigned, or signed, or 2's complement representation[13].In particular, the first two units include two similar logic modules, which manipulate the incoming operands, for multiplication and addition and the outgoing stream, i.e. the final result, and perform the data transfers from/to the bus. The ASU also includes a third module for internal data conversion [14]. Reconfiguration can be done dynamically using a few control bits. There are many possible combinations of the reconfiguration parameters, yielding a number of different modes of operation [16]. The architecture can be reconfigured with respect to the following parameters: i) the bit width of the operands, ii) the arithmetic system of computations (unsigned, sign-magnitude and 2's complement) and iii) various throughput rates. The architecture of the reconfigurable Multiplication Accumulation Component (MAC) is shown in Figure 2.18. It consists of: i) the Interface Unit (IU), ii) the Arithmetic Selection Unit (ASU), iii) the Multiplication Unit (MU), iv) the Addition Unit (AU) , v) the Accumulation Unit (AcU) and vi) the Reconfiguration Logic (RL).

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III. PROPOSED ARCHITECTURE

The Parallel Matrix Multiplication [7] has many different identifications, but all with the similar implementation. That is, they immediately multiplex a pair of matrix elements in special. Parallel Matrix Multiplication on Systolic Array (PMMSA) uses this approach. In [5], PMMSA is characterized by processing data input in pipeline and comprised of regularly arrayed PE. Where neighbor PEs are connected with each other by shortest line and therefore mass data has no need to be stored before processing. Decrease of distance between the PEs in an array greatly reduces the internal communication delay and improves the utility of processing units [17]. It also removes time consumption for controlling the establishment of data stream. In, this research, the PE is replaced with Multiplication and Accumulation (MAC) to enhance the speed and reduce the complexity of Systolic Architecture. The algorithm for the matrix multiplication of order N×N is shown bellow.

1. For I = 1 to N →Start of for loop 1
2. For J = 1 to N →Start of for loop 2
3. For K = 1 to N →Start of for loop 3
4. C[I,J] = C[I,J] + A[J,K] × B[K,J]
   →Computation of Matrix Multiplication and it will be Implemented by using systolic array
5. End →End of for loop1
6. End →End of for loop2
7. End →End of for loop3

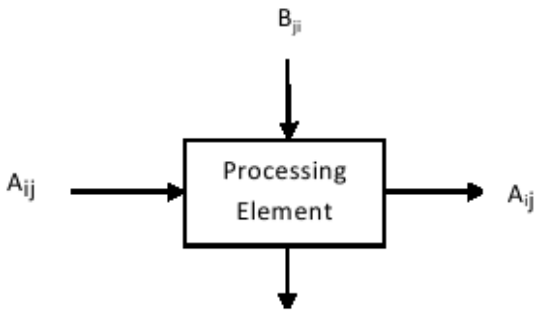
The above algorithm can be implemented in two methods

1. Conventional method (without Pipeline and Parallel Processing)
2. Systolic Architecture (Pipeline and Parallel Processing)

In this paper, we aim to compute the equation (1) with a two dimensional systolic array.

$$C_{m\times n} = A_{m\times k} \times B_{m\times k} \text{ ---------- (1)}$$

Where A, B and C are the matrices with order $m\times k, k\times n$ and $m\times n$ respectively. Each PE of systolic array computes the multiplication of elements and accumulates to the corresponding element and then elements will be passed to neighbor PE in the systolic array [18]. First elements $a_{i,j}$ in row i of matrix A are injected first into PE as pipeline with the sequence of $a_{i,k}$ and the input time to the element of $a_{i+1,j}$ is one time unit later than $a_{i,j}$. Similarly, elements $b_{i,j}$ in column j of matrix B are injected first into PE as pipeline with the sequence of $b_{k,j}$ and the input time to the element of the sequence of $b_{k,j+1}$ is one time unit later than $b_{k,j}$. The architecture of PE in this approach is shown in figure 3 which performs the Multiplication and Accumulation on data



.Figure 3, PE of Systolic Architecture

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IV. RESULTS & DISCUSSION

The implementation of Matrix Multiplication is done in both methods i.e. Conventional without pipeline and Conventional with pipeline, as described above, on FPGA. The RTL code is written in VHDL, verification of logic and simulation is done by ModelSim XE 6.4b [19]. The simulation results have given that, the conventional with pipeline implementation requires less number of clock cycles then Conventional method without pipeline and is shown in Figure given below. The simulation results in Figure given below.

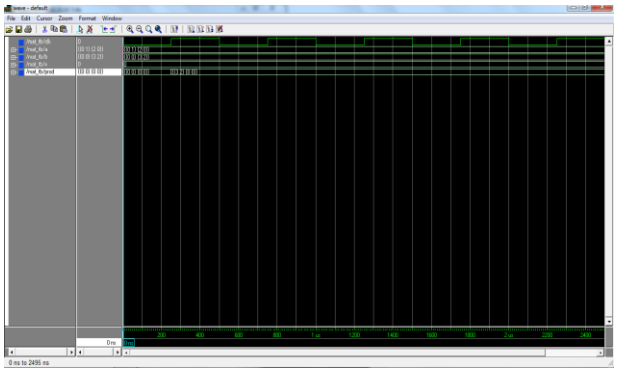

Figure 4, Simulation output for Conventional method without pipeline (Two even matrixes (2x2))

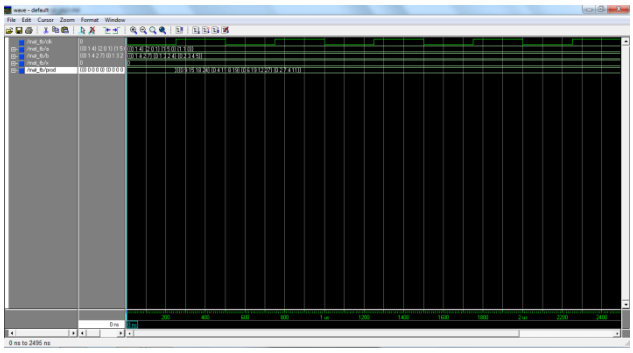

Figure 5, Simulation output for Conventional method without pipeline (Two uneven matrixes (4x3) and (3x5))

Figure 6, Simulation output for Conventional method without pipeline (Two even matrixes (8x8))

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Figure 7, Simulation output for Conventional method with pipeline (Two even matrixs (8x8))

Exposes the parallel processing and pipelining by the conventional with and without pipeline and also the input and output matrices, next step will be trying to write RTL code in VHDL for systolic array and respectively where the matrix elements are of 4 bit each. After simulation, the design is passed for synthesis onto the platform XILINX ISE 9.2i to convert RTL logic into gate level netlist and also the schematic diagram is captured.

V. CONCLUSION

The implementation of Matrix Multiplication is done in both methods i.e. Conventional and Systolic Architecture, The Systolic Array Architecture is designed for Matrix Multiplication and it is targeted to the Field Programmable Gate Array device. The parallel processing and pipelining is introduced into the systolic architecture to enhance the speed and reduce the complexity of the Matrix Multiplier for image and signal applications. To replacing the processing element of systolic architecture by efficient MAC (Multiplication and Accumulation) unit .The design is simulated, synthesized, and implemented on FPGA device.

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