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Closed Loop Control of Transformerless Interleaved High Step-Down Conversion Ratio DC-DC Converter

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ABSTRACT: This paper proposes closed loop control of transformerless interleaved high step-down conversion ratio dc-dc converter. The proposed converter utilizes two input capacitors which are series charged by the input voltage and parallel discharged by a new two phase interleaved buck converter for providing much higher conversion ratio without adopting an extreme short duty cycle. The proposed converter features uniform current sharing characteristic of the interleaved phases without adding extra circuitry. It also reduces the voltage stress of both switches and diodes. This will allow one to choose MOSFETs with low voltage rating to reduce both conduction and switching losses. Closed loop PI controller is used to control the error and finally achieves the desired output voltage. The operation principles, steady state analysis and comparison with other existing topologies are presented. Simulation results are presented to demonstrate the effectiveness of the converter.

KEYWORDS: High step down conversion ratio, Interleaved Buck Converter (IBC), Closed loop, PI controller.

I.INTRODUCTION

Nowadays, for the increasing high step down ratios with high output current applications such as battery chargers, distributed power systems and VRMs of CPU boards, high performance dc-dc converters have been used. The conventional IBC is required operating at higher switching frequencies for high-input and low-output voltage applications, that will increase both switching and conduction losses. It also experiences an extremely short duty cycle in the case of high-input and low-output voltage applications [1]. Many step-down converters have been proposed to overcome the drawbacks of conventional IBC.

II.LITERATURE SURVEY

A quadratic buck converter [2] is synthesized by cascading two dc-dc buck converters. It can operate with wider ranges of step-down conversion ratio than conventional IBC but the efficiency is very poor. A three level buck converter [3] possess higher efficiency and better performance than the conventional IBC due to reduced voltage stress across the switch (half of the input voltage). However, so many components are required for this converter. An IBC with single capacitor turn off snubber is introduced in [4].By using this the switching loss associated with turn-off transition can be reduced and the single coupled inductor implements the converter as two output inductors, still the voltage across all the elements is same as input voltage.

To reduce the switching losses, an active clamp IBC is introduced in [5], here all the switches are turned on with zero voltage switching (ZVS) whereas it requires additional passive elements and active switches, which increases the cost at low or middle levels of power applications. Recently, an IBC with two coupled inductors are introduced [6,7]. Moreover, a high step-down conversion ratio is obtained and the switching losses can be reduced. However, the leakage energy needs to recycle. A new extended duty ratio multiphase topology has been proposed to deal with a small duty cycle of the IBC in high-input and low-output voltage applications [8,9]. Extended duty ratio mechanisms are very efficient input voltage dividers which reduce the switching voltage and associated losses.

In this paper, transformerless interleaved high step-down conversion ratio dc-dc converter is proposed. This topology contains an input voltage divider circuit for storing energy in the blocking capacitors for increasing step-down conversion ratio and reducing voltage stresses of the active switches. The closed loop control is achieved by using

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Proportional Integral (PI) controller. First, the circuit topology and operation principle are given in Section III. The control scheme is presented in Section IV. The corresponding steady state analysis is made in Section V. Simulation model and it results are presented in section VI. Finally conclusion is presented in last section.

III.OPERATING PRINCIPLE

The proposed converter consists of two inductors, four active power switches, two diodes and four capacitors. The main objectives of the capacitors are 1) to store energy 2) to reduce the voltage stress of active switches as well as to increase the step-down conversion ratio. The operating principle of proposed converter can be classified into four operating modes. The gating signals are given with a phase shift of 180°. High step-down conversion ratio is achieved when the duty cycle is less than 0.5 and in CCM.

Mode 1 [$t_0 < t \leq t_1$]: During this mode, S_{1a}, S_{1b}, and D_1 are turned on, while S_{2a}, S_{2b}, and D_2 are turned off. The corresponding equivalent circuit is shown in Fig.1. From Fig.1, one can see that, during this mode, current i_{L1} freewheels through D_1, and L_1 is releasing energy to the output load. However, current i_{L2} provides two separate current paths through C_A and C_B. The first path starts from C_1, through S_{1a}, C_A, L_2, C_O and R, and D_1 and then back to C_1 again. Hence, the stored energy of C_1 is discharged to C_A, L_2, and output load. The second path starts from C_B, through L_2, C_O and R, and $S_{1b}$and then back to C_B again. In other words, the stored energy of C_B is discharged to L_2 and output load. Therefore, during this mode, i_{L2} is increasing, and $i_{L1}$is decreasing. Also, from Fig.1, one can see that V_{C1} is equal to V_{CA} plus V_{CB} due to conduction of S_{1a}, S_{1b}, and D_1. Since $V_{C1} = V_{in}/2$ and $V_{CA} = V_{CB} = V_{C1}/2 = V_{in}/4$, one can observe from Fig.1.that the voltage stress of D_2 is equal to $V_{CB} = V_{in}/4$ and the voltage stresses of $S_{2a}$and S_{2b} are clamped to $V_{C2} = V_{in}/2$ and $V_{C1} = V_{in}/2$, respectively. The corresponding state equations are given as follows:-

$$L_1 \frac{di_{L_1}}{dt} = -v_{C_o} \quad (1)$$

$$L_2 \frac{di_{L_2}}{dt} = v_{C_1} - v_{C_A} - v_{C_o} = v_{C_B} - v_{C_o} \quad (2)$$

$$(C_1 + C_2)\frac{dv_{C_1}}{dt} = -i_{C_A} \quad (3)$$

$$C_A \frac{dv_{C_A}}{dt} = i_{L_2} + i_{C_B} \quad (4)$$

$$C_B \frac{dv_{C_B}}{dt} = i_{C_A} - i_{L_2} \quad (5)$$

$$C_o \frac{dv_{C_o}}{dt} = i_{L_1} + i_{L_2} - \frac{v_{C_o}}{R} \quad (6)$$

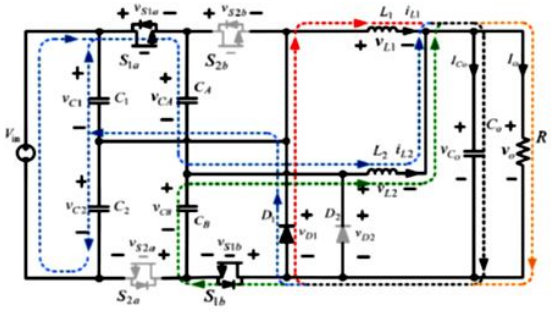

Fig.1.Equivalent circuit of the proposed converter in Mode 1 operation

Mode 2 [$t_1 < t \leq t_2$]: During this mode, S_{1a}, S_{1b}, S_{2a}, and S_{2b} are turned off. The corresponding equivalent circuit is shown in Fig.2. From Fig.2, one can see that both i_{L1} and i_{L2} are freewheeling through D_1 and D_2, respectively. Both V_{L1} and V_{L2} are equal to $-V_{CO}$, and hence, i_{L1} and i_{L2} decrease linearly. During this mode, the voltage acrossS_{1a}, namely, V_{S1a} is equal to the difference of V_{C1} and V_{CA}, and V_{S1b} is clamped at V_{CB}. Similarly, the voltage across S_{2a}, namely, V_{S2a} is equal to the difference of V_{C2} and V_{CB}, andV_{S2b} is clamped at V_{CA}. The corresponding state equations are given as follows:-

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$$L_1 \frac{di_{L_1}}{dt} = -v_{C_o} \quad (7)$$

$$L_2 \frac{di_{L_2}}{dt} = -v_{C_o} \quad (8)$$

$$(C_1 + C_2)\frac{dv_{C_1}}{dt} = 0 \quad (9)$$

$$C_A \frac{dv_{C_A}}{dt} = 0 \quad (10)$$

$$C_B \frac{dv_{C_B}}{dt} = 0 \quad (11)$$

$$C_o \frac{dv_{C_o}}{dt} = i_{L_1} + i_{L_2} - \frac{v_{C_o}}{R} \quad (12)$$

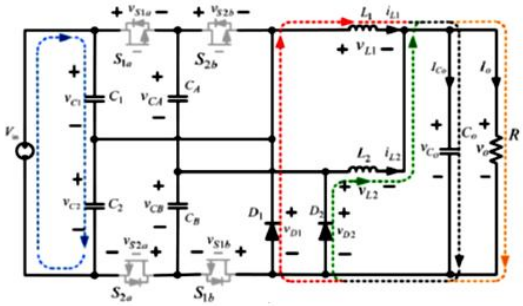

Fig.2.Equivalent circuit of the proposed converter in Mode 2 operation

Mode 3 [$t_2 < t \leq t_3$]: During this mode, S_{2a}, S_{2b}, and D_2 are turned on, while S_{1a}, S_{1b}, and D_1 are turned off. The corresponding equivalent circuit is shown in Fig.3. From Fig.3, one can see that, during this mode, current i_{L2} is freewheeling through D_2, and L_2 is releasing energy to the output load. However, current i_{L1} provides two separate current paths C_A and C_B. The first path starts from C_2, through L_1, C_O and R, D_2, C_B, and $S_{2a}$and then back to C_2 again. Hence, the stored energy of C_2 is discharged to C_B, L_1, and output load. The second path starts from C_A, through S_{2b}, L_1, C_O and R, and D_2 and then back to C_A again. In other words, the stored energy of C_A is discharged to L_1 and output load. Therefore, during this mode, i_{L1} is increasing, and i_{L2} is decreasing, as can be seen from Fig.2. Also, from Fig.3, one can see that V_{C2} is equal to V_{CA} plus V_{CB} due to conduction of S_{2a} and S_{2b}. Since $V_{C2} = V_{in}/2$ and $V_{CA} = V_{CB} = V_{C2}/2 = V_{in}/4$, one can observe from Fig.3.that the voltage stress of D_1 is equal to $V_{CA} = V_{in}/4$ and the voltage stresses of $S_{1a}$and $S_{1b}$are clamped to $V_{C1} = V_{in}/2$ and $V_{CB} = V_{in}/4$ respectively. The corresponding state equations are given as follows:-

$$L_1 \frac{di_{L_1}}{dt} = V_{in} - v_{C_1} - v_{C_B} - v_{C_o} \quad (13)$$

$$L_2 \frac{di_{L_2}}{dt} = -v_{C_o} \quad (14)$$

$$(C_1 + C_2)\frac{dv_{C_1}}{dt} = i_{C_B} \quad (15)$$

$$C_A \frac{dv_{C_A}}{dt} = i_{C_B} - i_{L_1} \quad (16)$$

$$C_B \frac{dv_{C_B}}{dt} = i_{C_A} + i_{L_1} \quad (17)$$

$$C_o \frac{dv_{C_o}}{dt} = i_{L_1} + i_{L_2} - \frac{v_{C_o}}{R} \quad (18)$$

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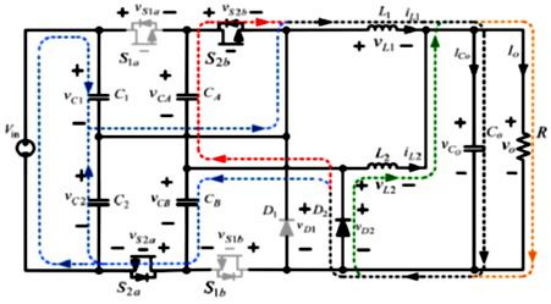

Fig.3.Equivalent circuit of the proposed converter in Mode 3 operation

Mode 4 [$t_3 < t \leq t_4$]: For this operation mode, as can be observed from Fig.2, S_{1a}, S_{1b}, S_{2a}, and $S_{2b}$are turned off. The corresponding equivalent circuit turns out to be the same as Fig.2, and its operation is the same as that of mode 2. From the aforementioned illustration of the proposed converter, one can see that not only the control is very simple but also the operations of two phases are both symmetric and rather easy to understand.

IV.CONTROL SCHEME

The closed loop PI controller is used in the proposed converter to achieve the desired output voltage. The PI controller continuously calculates an error value as the difference between a measured process variable and a desired set point. The controller attempts to minimize error over time by adjustment of a control variable. PI controllers are fairly common, since derivative action is sensitive to measurement noise.

PI controller is implemented here due to its several advantages. Steady state error resulting from P controller is easily overcome by the use of PI controller. However, the controller possess negative effect in terms of overall stability of the system, it has a negative impact. This controller is mostly employed in areas where speed of the system is not a matter of significance. It also serves the purpose of the converter by achieving voltage regulation. Fig.4 shows the block diagram of control scheme.

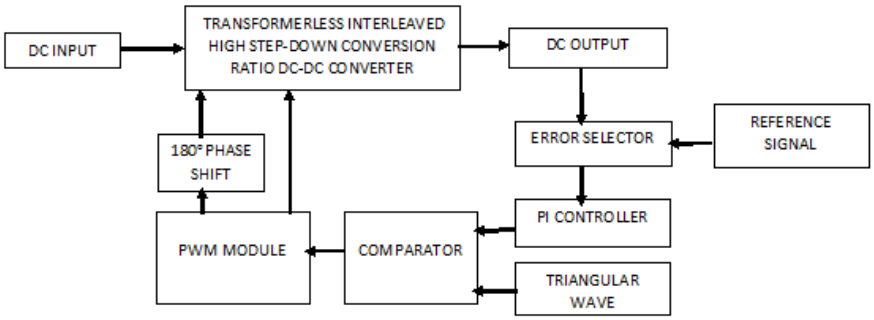

Fig.4.Block diagram of control scheme for the proposed converter

V.STEADY STATE ANALYSIS

For steady state analysis, some assumptions are made as follows:-

1) All components are ideal components.
2) The capacitors are sufficiently large such that the voltages across them can be considered constant. Also, assume that $C_1 = C_2$ and $C_A = C_B$.
3) The system is under steady state and is operating in CCM with duty ratio being lower than 0.5 for high step-down conversion ratio purposes.

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A. Conversion ratio

Referring to Fig.1 and 3, from the volt–second relationship of inductor L_1 (or L_2), one can obtain the following relations:-

$$(V_{C_B} - V_o)D = V_o(1-D) \quad (19)$$

$$(V_{C_A} - V_o)D = V_o(1-D) \quad (20)$$

Also, from the equivalent circuits in Fig.1 and 3, voltages V_{C1}, V_{C2}, V_{CA}, and V_{CB} can be derived as follows:-

$$V_{C_1} = V_{C_2} = \frac{V_{in}}{2} \quad (21)$$

$$V_{C_A} = V_{C_B} = \frac{V_{in}}{4} \quad (22)$$

The output voltage can be obtained by substituting (22) into (19) or (20) as follows:-

$$V_o = \frac{D}{4}V_{in} \quad (23)$$

Thus, the conversion ratio M of the proposed converter can be obtained as follows:-

$$M = \frac{V_o}{V_{in}} = \frac{D}{4} \quad (24)$$

B. Voltage Stresses on Semiconductor Components

To simplify the voltage stress analysis of the components of the proposed converter, the voltage ripples on the capacitors are ignored. From Fig.1 and 3, the voltage stresses on diodes D_1 and D_2 can be obtained directly as shown in the following equation:-

$$V_{D_{1,max}} = V_{D_{2,max}} = \frac{V_{in}}{4} \quad (25)$$

From (25), the voltage stress of the diodes of the proposed converter is equal to one fourth of the input voltage. Hence, the proposed converter enables one to adopt lower voltage rating devices to further reduce conduction losses. As can be observed from the equivalent circuits in Fig.1 and 3, the open circuit voltage stress of active power switches S_{1a}, S_{2a}, S_{1b}, and S_{2b}can be obtained directly as :-

$$V_{S_{1a,max}} = V_{S_{2a,max}} = V_{S_{2b,max}} = \frac{V_{in}}{2} \; ; \; V_{S_{1b,max}} = \frac{V_{in}}{4} \quad (26)$$

In fact, the maximum resulting voltage stress of the active power switches is equal to $V_{in}/2$. Hence, the proposed converter enables one to adopt lower voltage rating active switches to further reduce both switching and conduction losses.

VI.SIMULATION RESULTS AND DISCUSSION

The closed loop control of transformerless interleaved high step-down conversion ratio dc-dc converter is simulated by using MATLAB (Simulink) software. For simulation 400V input, 25V output and 400W rating model of the proposed converter is considered. The switching frequency is chosen to be 40KHz.

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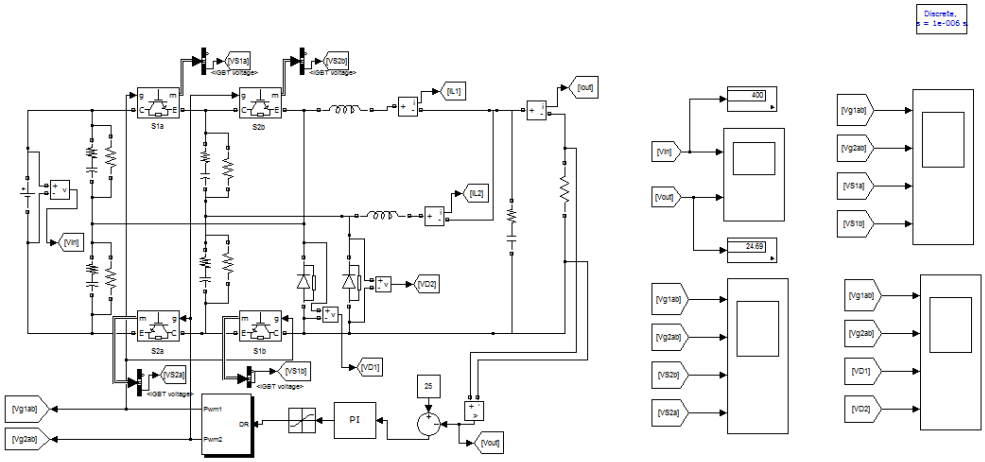

Fig.5.MATLAB Simulink model of the proposed converter

Fig.5 shows the MATLAB Simulink model of the proposed converter. The value of input and blocking capacitors are 250µF and 10µF respectively. The value of input inductors are chosen as 250µH.

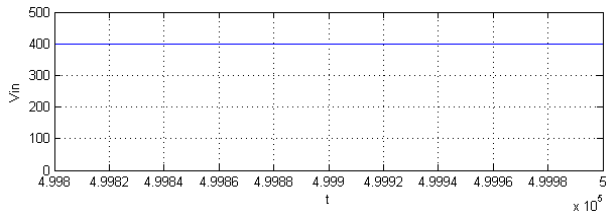

Fig.6.Input voltage waveform

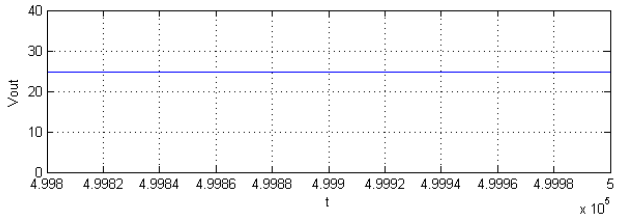

Fig.7.Output voltage waveform

Fig.6 and Fig.7 shows the input voltage and output voltage waveforms respectively. From these waveforms it is clear that the proposed converter possesses a very high step-down conversion ratio.

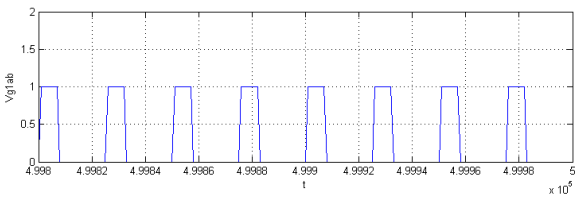

Fig.8.Gating signals to switches S_{1a} and S_{1b}

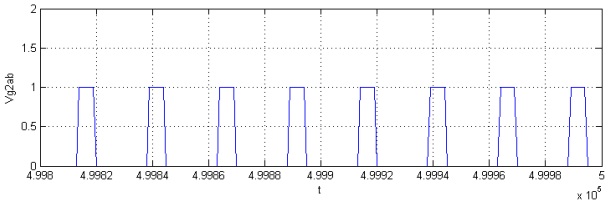

Fig.9.Gating signals to switches S_{2a} and S_{2b}

Fig.8 and Fig.9 shows the waveforms of gating signals to the active switches. Here the duty ratio is set to be 0.25 for continuous conduction mode of operation.

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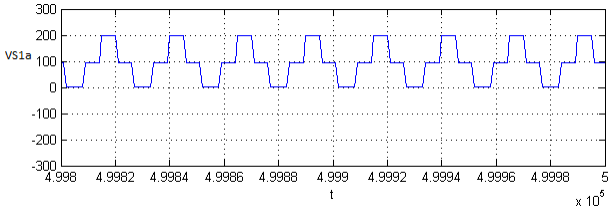

Fig.10.Voltage stress waveform of switch S_{1a}

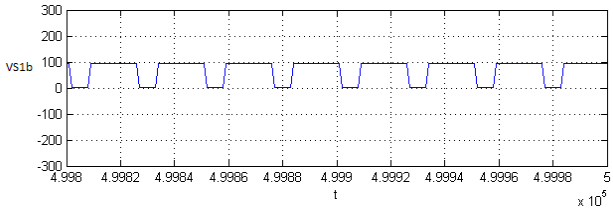

Fig.11.Voltage stress waveform of switch S_{1b}

From Fig.10 (waveform of voltage stress of switch S_{1a}) it is clear that the maximum voltage appears across the switch S_{1a} is half of the input voltage. Similarly from Fig.11 the maximum value of voltage appears across the switch S_{1b} is $(1/4)^{th}$of the input voltage.

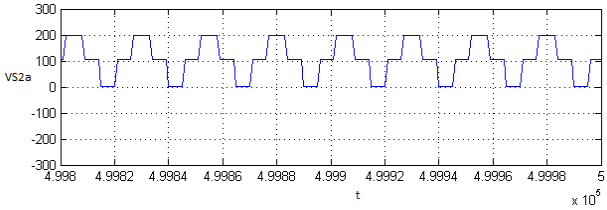

Fig.12.Voltage stress waveform of switch S_{2a}

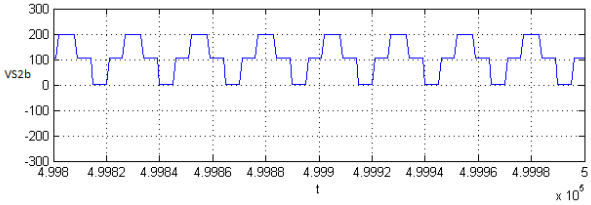

Fig.13.Voltage stress waveform of switch S_{2b}

It is found from Fig.12 and Fig.13, the maximum voltage appears across the switch S_{2a} and S_{2b} is half of the input voltage.

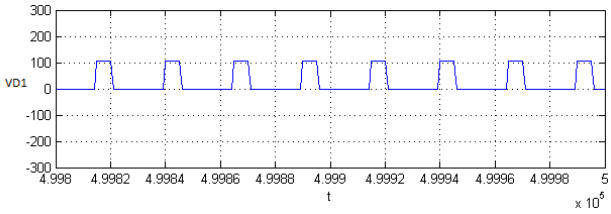

Fig.14.Voltage stress waveform of diode D_1

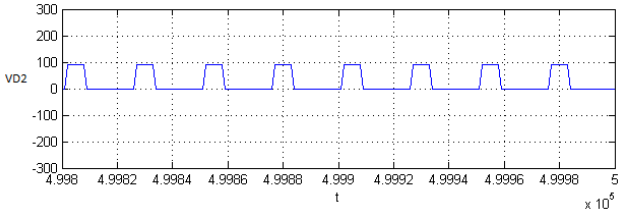

Fig.15.Voltage stress waveform of diode D_2

Fig.14 and Fig.15 shows the voltage stress of diodes D_1 and D_2 respectively. The maximum voltage across the diodes D_1 and D_2 is $(1/4)^{th}$ of the input voltage.

VII.CONCLUSION

The proposed converter topology possesses high step-down conversion ratio and low switch voltage stress characteristic. Low switch voltage stress characteristic will allow one to choose lower voltage rating MOSFETs to reduce both switching and conduction losses, and the overall efficiency is consequently improved. The closed loop PI controller controls the error effectively and gives the desired output voltage. Moreover, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the interleaved phases without extra circuitry or complex methods.

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