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Comparative Analysis of Area-Efficient Low Power 1-Bit Full Adders at 65-Nm Technology

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ABSTRACT: In this Paper we present Low power and Area-efficient 1-Bit Full adder designs featuring Conventional CMOS, CPL, PTL and XNOR-XNOR CMOS design styles. Area-efficiency is one of the most required features of the modern electronic System designed for high performance and Portable applications. We carried out a Comparison between these designs reported as in terms of Speed, Power dissipation and Area. The proposed full adders are area-efficient and outperform several standard Full adders without trading of driving capabilities and reliabilities. The new Full adders successfully operate at low voltage with excellent Signal integrity and Driving Capability. XNOR-XNOR based design full adder is more reliable in terms of Area, Power dissipation and Speed than other two proposed designs. All the Schematics and Layouts of these full adders were designed with a 65-nm CMOS technology using Micro wind 3.1.

KEYWORDS: Full Adder, Centralized, CPL, PTL, XNOR, Low Power

I. INTRODUCTION

CMOS VLSI circuits have been evolving into low voltage and low power regimes. In recent years VLSI design space has been focusing on high performance microprocessors. Demand for power sensitive, high speed, small area and low cost designs are increasing every day. This tremendous demand is due to fast growth of battery-operated portable applications such as personal computing devices (portable computers and real time audio and video based multimedia products), wireless communication systems (personal

Digital assistant and mobile phones), medical applications and other portable devices. Broad acceptance of new applications critically depends on the availability of compact and inexpensive hardware delivering the required high performance and longer battery life. Unfortunately battery capacity has not improved at the same pace as semiconductor performance and integration and it not expected to improve more than 30% every five years. Consequently, integrated circuits (ICs) designed for hand-held applications must increase performance at reduced energy per computation. Also low power designs reduce cooling cost and increases reliability especially for high density systems. This has pursuit the design engineers to develop a much more flexible design to overcome critical issues of low power consuming, small area and efficient designs. The single-bit full adder is one of the main components in almost all logic structures. The performance of logic structures is highly dependent on the adder cells. The wide use of this operation in arithmetic functions, have made many researchers eager to propose several kinds of different logic styles for implementing 1-bit Full Adder cell, in recent years. To perform arithmetic operation, a device can use up very low power by functioning at very low frequency but it may spend a very long time to finish the operation. The power-delay product can be used for first level comparison between the different building block designs. The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. The necessity and Popularity of portable electronics is driving designers to endeavor for smaller area, higher speed, longer battery life and more reliability. Power and delay are the premium resources a designer tries to save when designing a system.

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II. FULL ADDER (FA)

The low-power design has become a major design consideration [1]. The design criterion of a full adder (FA) cell is usually multi-fold. Adders are important components of all arithmetic units in digital domain circuits.

Addition is the most basic arithmetic operation and adder is the most fundamental arithmetic component of the processor. Two important attributes of all digital circuits, for most applications are maximizing speed and minimizing power consumption [2]. The speed of different modules used in the design will dominate the overall performance of the system. The basic binary adder is shown in figure 1,

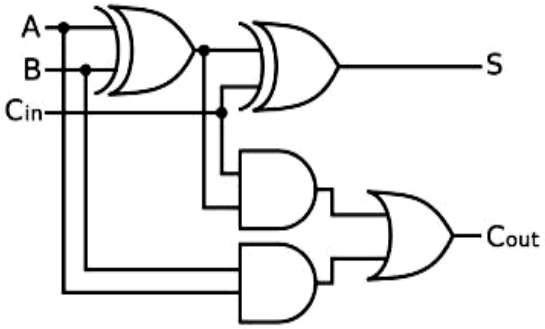

Fig.1: Block Diagram of Basic Full Adder

Depending on the delay and power consumption requirements, several adders can be implemented. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU).The truth table of full adder is shown in table 1.

TABLE1 Truth Table of Full Adder

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The speed of the design is limited by size of the transistors, parasitic capacitance and delay in the critical path [3]. The driving capability of a full adder is very important, because full adders are mostly used in cascade configuration, where the output of one provides the input for other.

In the last decade, the full adder has gone through substantial improvement in power consumption, speed and size, but at the cost of weak driving capability and reduced voltage swing. However, reduced voltage swing has the advantage of lower power consumption [4]. There is no ideal full adder cell that can be used in all types of applications. Hence novel architectures such as CMOS Transmission Gate (TG), Pass-Transistor Logic (PTL), and Complementary Pass-transistor Logic (CPL) are compared here.

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III. PREVIOUS FULL ADDER OPTIMIZATION

Many Papers have been published regarding the optimization of Low power full adders, trying different options for the Logic styles like standard CMOS logic, Differential cascade voltage switch (DCVS),Double pass-transistor logic (DPL), Swing restored CPL(SR-CPL),and hybrid styles [5]. Regarding this there is an alternative Logic structure for a full adder. Examining the full adder truth table, It can be seen that the Sum output is equal to the A⊕B value when C=0 and it is equal to (A⊕B)' value when C=1. Thus, a multiplexer can be used to obtain the respective value taking the C input as the selection signal. Following the same criteria, the Carry output is equal to the A.B value when C=0 and it is equal to A+B value when C=1. Again, C can be used to select the respective value for the required condition, driving a multiplexer. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the A⊕B and (A⊕B)' signals, another block to obtain the A.B and A+B signals, and two multiplexers being drive by the C input to generate the Sum and Carry outputs [6-7]. In these Adder designs use more one Logic Styles for their implementation which we call the Hybrid-CMOS logic design style, e.g a full adder is designed using a DPL logic design style to build the xor/xnor gates and a Pass Transistor based multiplexer to obtain Sum output [8].

IV. VARIOUS ADDER LOGIC COMPARISIONS

In recent years various types of adder using different logic styles have been proposed. Standard CMOS 28 transistor adder using pull up and pull-down network with 14 NMOS transistors and 14 PMOS transistors is most widely reported. Pass Transistor Logic (PTL) with 15T using 7NMOS and 4inverter using 4PMOS and 4NMOS is reported. Complementary pass-transistor logic (CPL) with 32 transistors having high power dissipation and better driving capability is reported [9].

A. Conventional 28t CMOS full adder

This adder was based on regular CMOS structure (pull-up and pull-down network) (Fig 2). Working principle: Cout is generated first $(A \cdot B) + (A+B) \cdot C_{in}$. Then the sum is derived from $(A \cdot B \cdot C) + (A+B+C_{in}) \cdot$ Complement C_{out}

Fig 4.2: 28T Conventional CMOS Full Adder

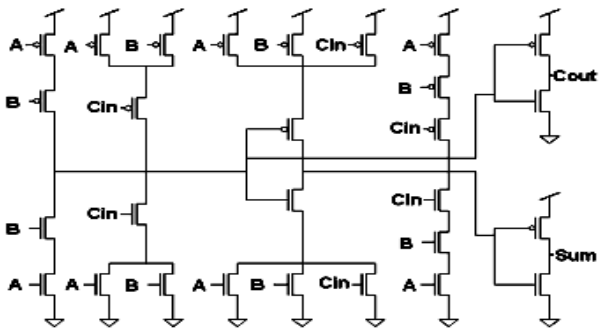

Fig.2. 28T Conventional CMOS Full Adder

Disadvantages: But the use of substantial number of transistors results in high input loads, more power consumption and larger silicon area.

B.*15T PTL logic full adder*

In this paper full adder circuit combines the MCIT for the sum operation and the Boolean reduction technique for the carry operation [10]. The sum and carry circuits were designed based on standard full adder sum and carry equations. In the multiplexing method, input Band its complement were used as the control signals of the sum circuit, as shown in Fig.3. The two-input XOR and combinational circuits were developed using the multiplexer method. The output node

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of the two-input multiplexer circuit is the differential node. According to equation the sum circuits require three inputs [11].

The A XOR B circuit is directly connected to input 'C'. The sum circuit is developed according to Equation. To avoid an increasing the number of transistors due to the addition of a third input, the XOR gate output is fed through the NOT gate from the differential node to C, and C is the input to the full adder; thus, the number of transistors is reduced to six in the sum circuit. The C and C out nodes are called the differential nodes of the circuit. The differential node output is a summing output.

Sum = A XOR (B XOR C)

Cout = AB + C (A XOR B)

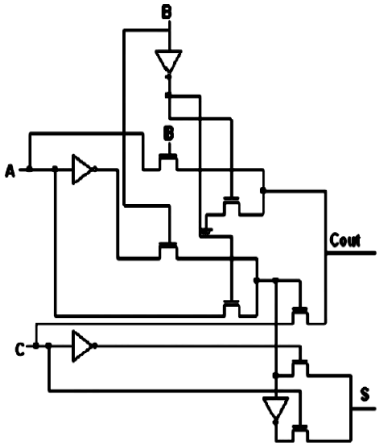

Fig.3. PTL full adder

The PTL adder circuit is shown in Fig.3, which contains 7 transistors and 4 inverters. The signal integrity is reduced in PTL adder due, because of he lower feature size (65nm) and fewer coupling capacitor adjacent wires. The proposed adder circuit used the minimum length of wire. The proper arrangement of the circuit is reduced the critical path in our proposed circuit. Our adder circuit minimizes the wire length by using a shorter connection of the common circuit of the sum and carry (A XOR B).

c. CPL logic full adder

In the absence of low-power design techniques such applications generally suffer from very short battery life, while packaging and cooling them would be very difficult and this is leading to an unavoidable increase in the cost of the product. So far several logic styles have been used to design full adders [13]. One example of such design is the standard static CMOS full adder. The main drawback of static CMOS circuits is the existence of the PMOS block, because of its low mobility compared to the NMOS devices. Therefore, PMOS devices need to be seized up to attain the desired performance. Another conventional adder is the complementary pass-transistor logic (CPL). Due to the presence of lot of internal nodes and static inverters, there is large power dissipation [14].

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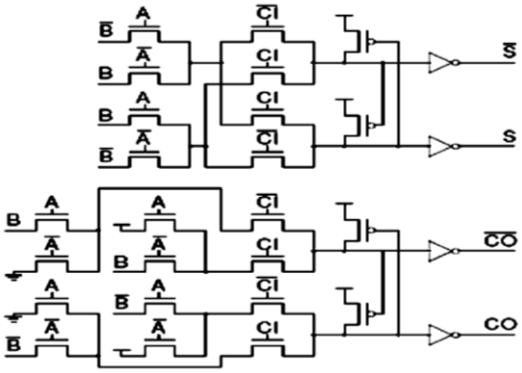

Fig.4.CPL Full Adder

V. PRIOR WORK

The full adder operation can be stated as follows: Given the three 1-bit inputs A, B, and Cin, it is desired to calculate the two 1-bit outputs Sum and Carry, where
Sum = (A **xor** B) **xor** Cin
Cout = A **and** B + Cin (A **xor** B)

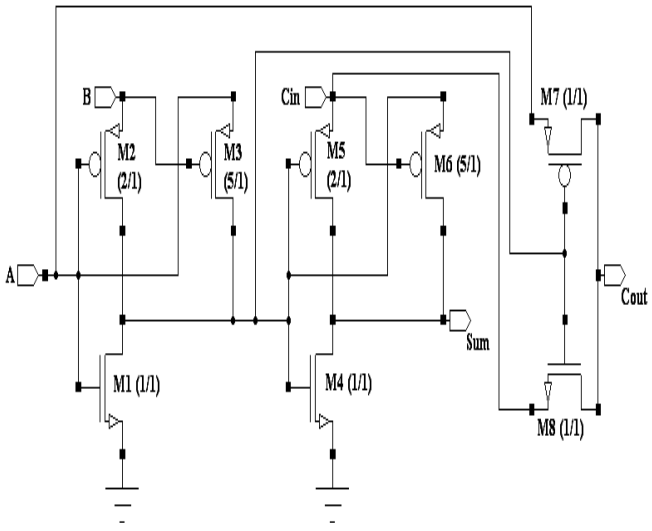

FIG.5. 1-Bit 8T Full Adder

Figure5 shows the circuit of eight tansistor 1-bit full adder cell. The Sum output is basically obtained by a cascaded exclusive OR of the three inputs. Cout module is implemented using 2T Multiplexer [12]. It is quite evident from Figure5 that two stage delays are required to obtain the sum output and at most two stage delays are required to obtain the carry output.

VI. FULL ADDER SCHEMATICS USING DSCH2 TOOL

Figure6 shows the schematics of PTL logic Full Adder. It's having 15 transistor counts.

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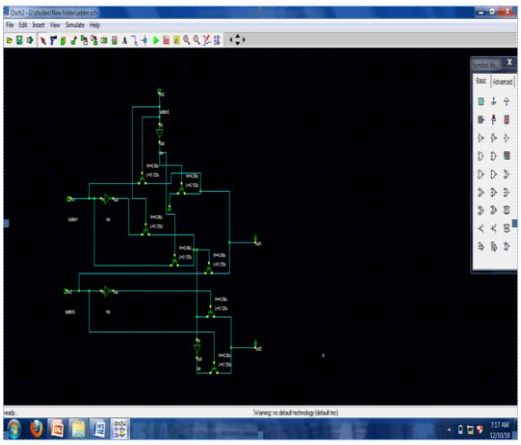

Fig6. PTL logic Full Adder

Figure7 shows the CPL logic full adder with 22 transistor counts. The schematics provide transistor counts and timing diagram of the circuit based on dsch2 tools.

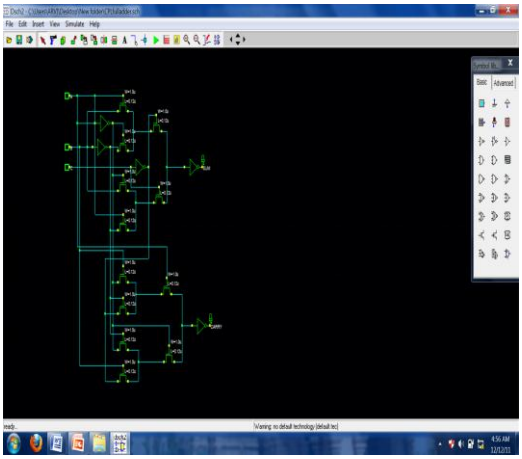

Fig7.CPL Logic Full Adder

VII.FULL ADDER LAYOUT USING MICROWIND3.1 TOOL

Microwind is a tool for designing and simulating circuits at layout level. The Microwind program allows the student to design and simulate an integrated circuit at physical description level.

Layout design using MICROWIND3.1 tool, provides the supply voltage, chip area with length and width also.

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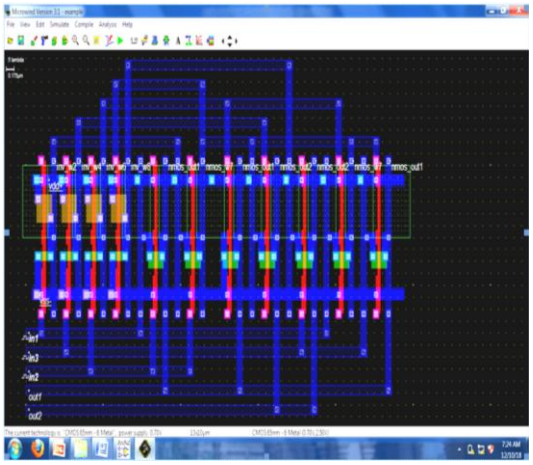

Fig8. Layout of PTL Logic Full Adder

Width 12µm
Length 9µm

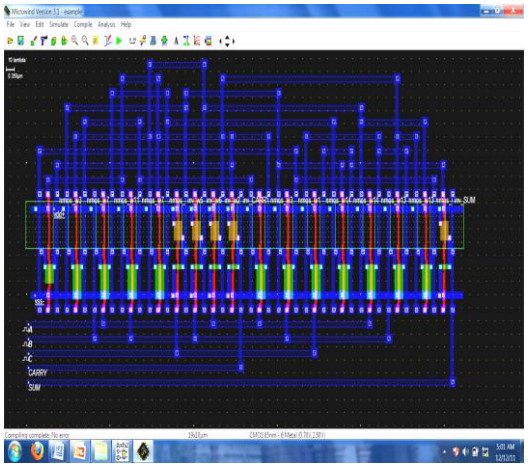

Fig9. Layout of CPL logic Full Adder

Width 19µm
Length 10µm

VIII.RESULTS AND CONCLUSION

Various adder logics like CMOS, CPL, DPL and XNOR-XNOR gate adder with hybrid logic is compared. The transistor count is produced with reduced power and provides long battery life also. The output waveforms are taken from MICROWIND 3.1 tool. It provides power, delay and PDP also. Reduced transistor count is reducing the chip area, supply voltage, power dissipation and so on. Following are the Full Adder outputs with different logic styles

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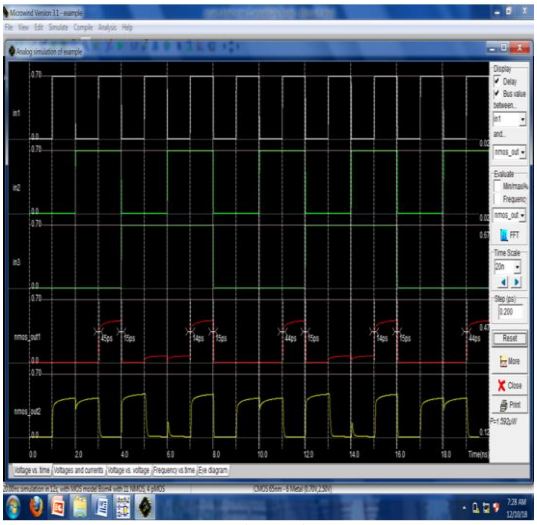

Fig10. Waveform of PTL Adder

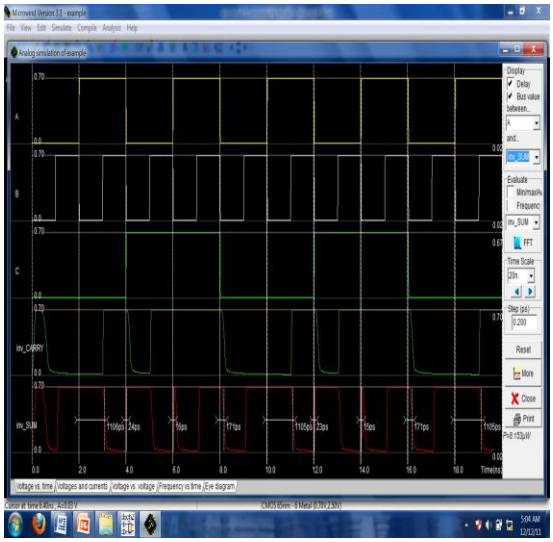

Fig11. Waveform of CPL Adder

IX.CONCLUSION

Various adders are compared with power, area and delay of most VLSI design parameters. In these different adders our proposed XNOR/XNOR adder-based cell achieves better performance in terms of power dissipation, propagation delay, area, due to less critical path compared to other logic circuits. Transistor count is also an important role of power dissipation and chip area. Reduced transistor count will reduce chip area, supply voltage, power dissipation, power delay product also calculated.

X.FUTURE WORK

In this paper, different Full Adder logics are compared using their transistor count. Future we used these adders and develop a square rooter circuit, because in square rooter circuit adder is an important part. Adder can do arithmetic operations.

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