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Variation in Parameters on Electrical Characteristics of FinFET with High-k dielectric

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ABSTRACT: The scaling of bulk CMOS faces significant challenges in the future due to fundamental material and process technology limits. Primary obstacles to the scaling of bulk CMOS to sub-45nm gate lengths include short channel effects, sub-threshold leakage, gate-dielectric leakage and device-to-device variations. Here, the effect of materials on leakage current and I_{on}/I_{off} ratio is evaluated using TCAD.

Rectangular fin shaped double gate(DG) and tri gate(TG) FETs are developed and their variations with different parameters are evaluated in these structures. Simulation results indicate that by using new materials on FinFET leakage current is improved further.

KEYWORDS: FinFET, DG FET, TG FET, Leakage

I.INTRODUCTION

Beyond 22nm technology node, multi-gate FETs such as FinFETs have emerged as the most promising candidates. FinFET is known to be the most manufacturable thin-body device due to self-aligned gate electrodes which are compatible with conventional planar bulk CMOS process. The strong electrostatic control over the channel originating from the use of multiple gates reduces the coupling between source and drain in the sub threshold region and it enables the multi-gate transistor to be scaled beyond bulk planar CMOS for a given dielectric thickness.

The main advantage of the FinFET is the ability to drastically reduce the short channel effect. In spite of his double gate structure, the FinFET is closed to its root, the conventional MOSFET in layout and fabrication. One of the major differences between a FinFET device and a planar device is the fact that the FinFET device consists of multiple small unit fins. FinFET circuits can achieve lower functional voltage supply and lower optimal energy consumption compared to CMOS circuits. In addition, FinFET has better immunity to soft error in sub-threshold region. The technology path is bulk-Planar MOSFET=)PDSOI(Partially Depleted Silicon On Insulator)=)FDSOI(Fully Depleted Silicon On Insulator)=)FinFET (double gate devices). The ultra-thin-body fully depleted (UTBFD)SOI and the non-planar FinFET device structures promise to be the potential future technology/device choices[3].In these device structures, the short-channel effect is controlled by geometry, and the off-state leakage is limited by the thin Si film.

Recent studies on High-k dielectrics for silicon MOSFETs by ALD and MOCVD techniques has prompted activities to develop GeMOSFETs implementing High -k dielectrics such as ZrO2 , HfO2 (Binary metal oxides). Melting point of Ge is low. Conventional polySi gate electrodes where high-temperature (>900°C) dopant activation is required cannot be used. Metal materials such as Al, W, Pt, TiN, and TaN are among the most popular metal electrodes reported for Ge MOSFETs. The metal gate electrodes are chosen considering their interaction with the Ge gate dielectric.

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Table 1 Properties of Ge and Si

Property	Ge	Si
Bandgap (Eg) eV	0.66	1.1
Electron mobility (cm^2/Vsec)	3900	1500
Hole mobility (cm^2/Vsec)	1900	450
Melting temperature (^{0}C)	934	1410

HfO2 and ZrO2 have reasonably high dielectric constants and band gaps. Both ZrO2 and HfO2 devices have demonstrated a many orders of magnitude reduction in gate leakage with an EOT around 1.0 nm and well-behaved transistors. However, they have high O2 and dopant diffusivity due to their crystalline microstructure. ZrO2 has a relatively stronger interaction with polysilicon gates than HfO2.

II.LITERATURE REVIEW

2.1 FinFET

The most promising and closer-to-application devices today are double-gate and tri-gate FinFETs, due to their superior scalability and ease of fabrication processing. The first article on the double-gate MOS (DGMOS) transistor was published by T. Sekigawa and Y. Hayashi in 1984. That paper shows that one can obtain significant reduction of short channel effects by sandwiching a fully depleted SOI device between two gate electrodes connected together. The device was called XMOS because its cross section looks like the Greek letter Ξ (Xi). The first fabricated double-gate SOI MOSFET was the "fully Depleted Lean-channel TrAnsistor (DELTA, 1989)", where the device is made in a tall and narrow silicon island called "finger", "leg" or "fin". The FinFET structure is similar to DELTA, except for the presence of a dielectric layer called the "hard mask" on top of the silicon fin. The hard mask is used to prevent the formation of parasitic inversion channels at the top corners of the device Even though current conduction is in the plane of the wafer, it is not strictly a planar device. Rather, it is referred to as a quasi-planar device, because its geometry in the vertical direction (viz. the fin height) also affects device behavior. The gate wraps around the body from three sides, and this is responsible for higher gate-channel control and therefore reduced SCE.

2.2 Double Gate FET

The double-gate concept was first reported in 1984 [21] and has been fabricated by several groups since then. The use of a double gate results in enhanced trans-conductance, due to the volume inversion effect and better subthreshold slope. There are two types of DG FETs, they are symmetric and asymmetric.

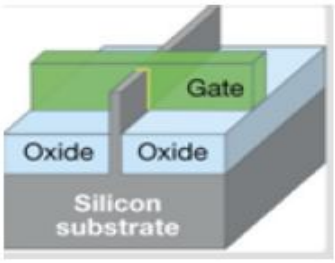

Fig. 1 DG MOSFET[13]

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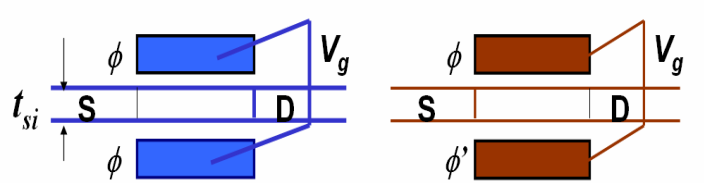

Symmetric Asymmetric

Fig. 2 Symmetric and Asymmetric DG MOSFET[12]

Symmetric DG MOSFET is with two gates of identical work functions and asymmetric DG MOSFET with two gates of different work functions. To fully exploit the benefits of DG MOSFETs, the body of DG MOSFETs is usually undoped or lightly doped. There are two operation modes for DG MOSFETs: three-terminal and four-terminal driven (or independently driven) mode. The three-terminal mode refers to the situation where the two gates of DG MOSFET are electrically connected and switched simultaneously. When operated in four-terminal driven mode, the two gates are biased differently with only one gate switching .The four-terminal driven mode enables the possibility of dynamic threshold voltage adjustment in circuit design and thus enlarges circuit design space [13, 14]

2.3 Trigate FinFET

In contrast to planar transistors where the Gate electrode was (usually) above the channel, the Gate electrode "wraps" the channel from three sides in FinFETs[2]. The current capability of the transistor may be increased by employing the "vertical dimension" - the transistor's height affects its current capability. The channel can be depleted fully because the electric field permeates in 3 directions (top and both sides) rather than just from the top as in a planar gate. The tri gate FinFET provides a symmetric device architecture where the channel is controlled by gate from three sides of the Si film. Since the gate control is increased, the requirements on the Si film thickness are relaxed as compared to single gate or double gate FinFET. Compared to FDSOI MOSFET or double gate FinFET[4], the Tri gate FinFETs are better because due to increased the gate control over the channel. So we can efficiently control the short channel effects and also further scaling is possible to meet the ITRS trends.

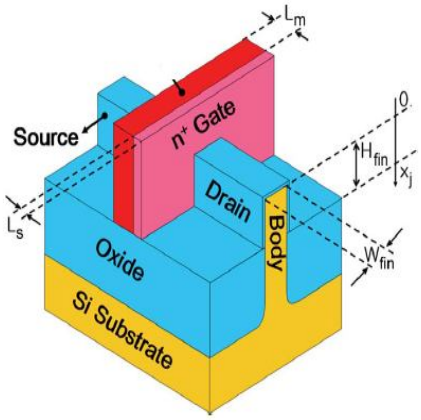

Fig. 3 Trigate FinFET [13]

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III.PROPOSED STRUCTURES

3.1 Double Gate MOSFET with high-k dielectric

Here a DG MOSFET with rectangular fin shape is designed. Usually the dielectric used is SiO2 and polysilicon gate. Here used ZrO2 as the dielectric and platinum metal as the gate material. The main advantage is that the OFF current can be decreased than the conventional DG MOSFET.

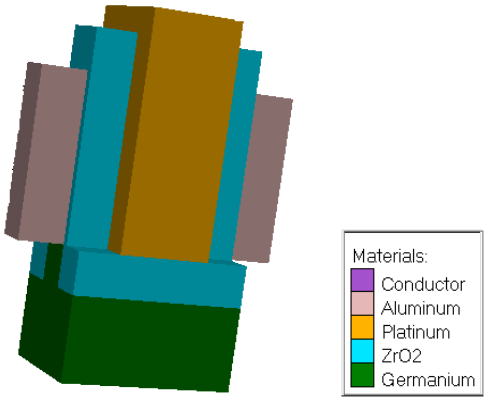

Fig. 4 DG MOSFET with high-k dielectric

Germanium offers higher mobility for both electrons (factor of 2) and holes (factor of 4) compared with Silicon. Smaller optical band-gap of Ge broadens the absorption wavelength spectrum allowing optoelectronic integration to enhance. Because of the low melting point of Ge, it is desirable to use metal gate electrodes rather than conventional polySi gate electrodes where high-temperature (>900°C) dopant activation is required.

3.2 Trigate FinFET with high-k dielectric

Here a TG FinFET with rectangular fin shape is designed. Here used ZrO2 as the dielectric and platinum metal as the gate material. The main advantage is that the OFF current can be decreased than the conventional TG FinFET.

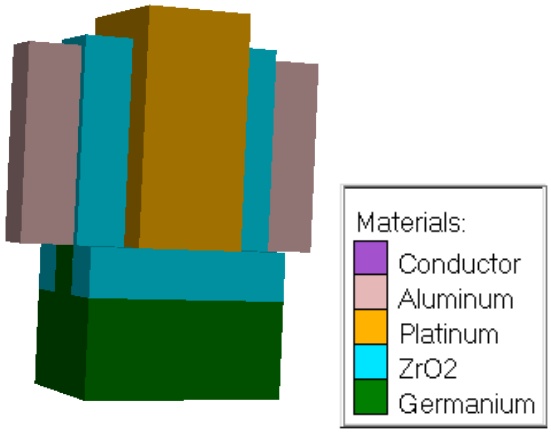

Fig. 5 Trigate FinFET with high-k

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IV.RESULTS AND DISCUSSION

Here Simulations are done by TCAD. Dimensions are given in the tale below.

Table 1 Dimensions of gate structures

Parameter	Description	DG-FET	TG-FET
L_g(nm)	Gate Length	22	22
t_{ox}(nm)	Oxide thickness	2	2
W_{fin}(nm)	Width(Thickness) of fin	10	10
H_{fin}(nm)	Height of fin	40	40
L_s(nm)	Length of source	11	11
L_D(nm)	Length of drain	11	11
$N_{S,D}$ (cm^{-3})	Doping conc. of source and drain	$5*10^{20}$	$5*10^{20}$
N_{ch} (cm^{-3})	Doping conc. of channel	$1*10^{15}$	$1*10^{15}$

4.1 Variation with fin width

MOSFET's drain leakage current or off-state current (I_{off}) is the drain current when no gate voltage is applied. It is the drain to source current which is extracted when V_{gs}=0 and V_{ds} = V_{dd}.

For the comparison graph here fin width is varied as 10nm, 15nm, 20nm, 25nm, 30nm. Leakage current also increases with increase in fin width due to reduced control of the gate over the channel. I_{off} current also decreases as the fin width decreases because the leakage current occurs at the middle of the fin, which is the more remote area from the gate. But as fin width decreases, the middle part of the fin has more control from the gate, so the leakage current decreases.

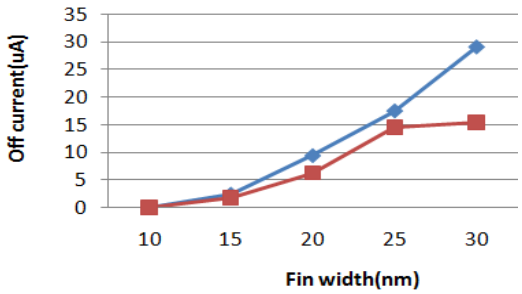

Fig. 1 Off current comparison of DG MOSFET(blue) and TG FinFET(red) as a function of fin width

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From the ouput graph above we can see that as the number of gates increased, leakage current is reduced. The graph shows the variation of leakage current for both DG and TG FET with the fin width.

4.2 Variation with fin height

Here for the comparison the fin height is varied as 10nm, 15nm, 20nm, 25nm, 30nm. As fin height decrease, leakage current decreases because of increase in its parasitic resistance (Rp). In order to decompose the Rp value into three components, namely, SD sheet resistance R_{SD}, contact resistance R_{cnt}, and extension resistance R_{ext}, R_{SD} and R_{cnt} were directly measured from the test element group of each wafer, R_{ext} with a tall fin was almost two times that with a short fin.

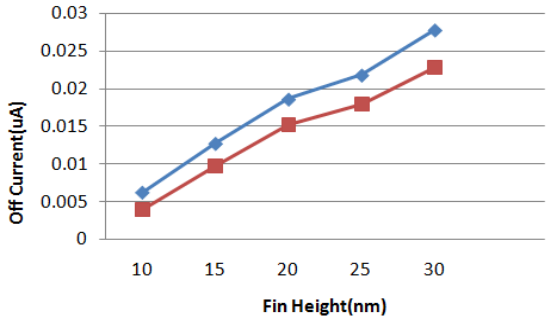

Fig. 2 Off current comparison of DG MOSFET(blue) and TG FinFET(red) as a function of fin height

The graph shows the variation of leakage current for both DG and TG FET with the fin height. As the fin height is increased the leakage current is decreased for both DG and TG FET. There is much reduction for TG FET.

4.3 Variation with gate length

Here the gate length is varied as 16nm, 18nm, 20nm, 22nm, 24nm, 26nm. With increase in gate length the gate control over the channel increases hence leakage current decreases.

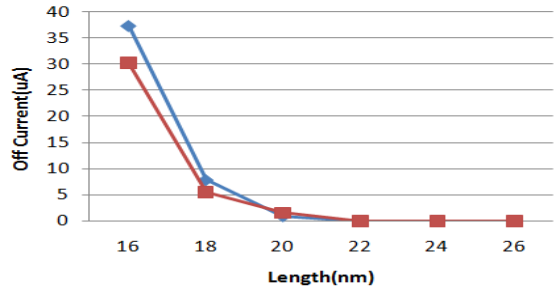

Fig. 3 Off current comparison of DG MOSFET(blue) and TG FinFET(red) as a function of gate length

The graph shows the variation of leakage current for both DG and TG FET with gate length. As the gate length is increased the leakage current is decreased for both DG and TG FET. There is much reduction for TG FET.

4.4 Variation with channel doping

When the doping increases, mobility degradation occurs, hence I_{on} decreases. As we increase the channel doping drive current reduces almost linearly, but off state current decreases exponentially. This leads to increase in I_{on}/I_{off} ratio very sharply. In addition, if the width of the device is also not large, the small volume of the device channel region will just hold a few hundred or fewer impurity atoms. Hence channel doping higher than $1*10^{17}$ cm^{-3} is good option to reduce the SCEs.

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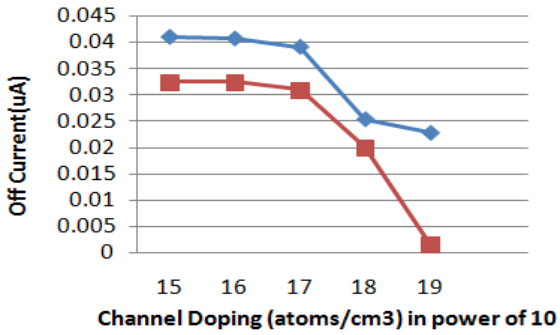

Fig. 4 Off current comparison of DG MOSFET(blue) and TG FinFET(red) as a function of gate length

The graph shows the variation of leakage current for both DG and TG FET with the change in channel doping. As the channel doping is increased the leakage current is decreased for both DG and TG FET. There is much reduction for TG FET.

From these results we can conclude that as the number of gates increased there is better control of the gate and thereby much reduction in leakage current. By changing the channel material as Ge, use ZrO2 as gate dielectric and platinum metal as the gate electrode, simulations on the same tool gives a much reduced leakage current for both DG and TG finFET.

VI.CONCLUSION

The work of this paper related to SCEs for different device structures with significance of variation in parameters. Extraction of I_{off} has been done using SILVACO ATLAS simulator. The I_{off} current is decreasing with reduction in height of fin but for channel length reduction it will increase. Also for increase in width of fin the leakage current increases but with the increase in channel doping the leakage current is reduced. With the help of results obtained in this paper we can set the dimensions of the device and its other parameters to reduce the power consumption and increases the reliability. Triple-gate FinFET devices are one of the most assuring successors of conventional MOSFET devices. Material property and also with the different gate structure there is much impact on leakage performance.

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