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Impact of Novel Fin Shaped Structures on Various Parameters

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ABSTRACT: Beyond 22 nm technology, FinFETs have become prominent device inorder to reduce the short channel effects. Here, the effect of fin shape on threshold voltage, subthreshold swing, leakage current and I_{on}/I_{off} ratio is evaluated using TCAD.

The fin shape can be changed by varying the top width of the fin. There was a reduction in leakage current by 92% in the case of triangular fin when compared with rectangular fin of same base width. Here, novel fin shaped structures like concave and convex FinFETs are developed and their variations with different parameters are evaluated in these structures. Simulation results indicate that by using concave and convex fin structures, all the parameters are improved further.

KEYWORDS: FinFET, Threshold Voltage, Subthreshold Swing, Leakage

I.INTRODUCTION

For many years now, the idea of scaling leads to the shrinking of MOSFETs [6]. By scaling, large transistor is scaled down to smaller transistor with similar behaviour by a scaling factor. Due to material used and process technology limits, scaling of CMOS leads to significant challenges in the future. Short channel effects, sub-threshold leakage, gate-dielectric leakage and device-to-device variations are the main obstacles to the scaling of bulk CMOS to sub-50nm gate lengths [1].

Alternate device structures like silicon-on-insulator (SOI) technology have become prominent as an effective means of increasing MOS scaling beyond the bulk limits for high-performance or low-power applications. The technology path is bulk-Planar MOSFET => PDSOI (Partially Depleted Silicon on Insulator) => FDSOI (Fully Depleted Silicon On Insulator) => FinFET (double gate devices). The ultra-thin-body fully depleted (UTBFD) SOI and the non-planar FinFET device have become a promise to be the future technology/device choices [3]. In these structures, device geometry can control the short-channel effects, and the thin silicon film can limit the off-state leakage. As scaling approaches the physical limits, unique and new circuit design issues need to be continued.

Beyond 22nm technology node, multi-gate FETs such as FinFETs have emerged as the most promising candidates. FinFET is known to be the most manufacturable thin-body device due to self-aligned gate electrodes which are compatible with conventional planar bulk CMOS process. The use of multiple gates provides strong electrostatic control over the channel which minimizes the coupling between source and drain in the sub threshold region.

II.LITERATURE REVIEW

2.1 FinFET

The FinFET is a transistor design, first developed by Chenming Hu and colleagues at the University of California at Berkeley, which aims to control the short channel caused by deep submicron transistors, such as Drain Induced Barrier Lowering (DIBL) [1]. A parallel transistor pair, consists of two transistors with their source and drain terminals tied together. By lifting up the channel above the wafer surface instead of making the channel just below the surface, the gate can wrap around by three sides, providing much greater electrostatic control over the carriers within it. The main feature of FinFET is the fin thickness, which needs to be smaller than or equal to the gate length. Their scaling does not

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depend on oxide thickness, which is a big advantage because it's the lithography process that defines the FET characteristics at each new process node. Furthermore, only one extra mask is required to create the silicon fin. Designers also have a choice of extending the width in third dimension in tri-gate FinFET without affecting layout area. As a result, the effective channel width can be significantly enhanced relative to a planar transistor.

2.2 Corner Effect

In the corner region of the adjacent gates, sharing of charges occurs due to the close proximity of gates. This will leads to premature inversion at the corner regions. The gate-to-channel electric field is concentrated at the fin corners. Therefore, at the corners of the fin, there will be a larger concentration of subthreshold leakage current, when the gate to- source input voltage rises toward the device threshold. This effect is called as corner effect [5]. This effect occurs in triple gate FinFET. The subthreshold characteristics of the FinFET are degraded due to the premature inversion at the corners which causes greater off state leakage current.

2.3 Partially Cylindrical FinFET

The figure 1 shows Partially Cylindrical FinFET (PC-FinFET) [8]. When the corners get rounded, the heat flow will be very easy, so that the self heating phenomenon gets reduced and thereby the mobility of the carriers is improved. This will also cause the reduction of the series resistance in the PC-FinFET that will results in rise of on-state current. Therefore, PC-FinFET leads to larger I_{on}/I_{off} ratio by the increase of on-state current. The corner rounding will also helps in the off-state leakage current reduction, because of the lack of premature inversion.

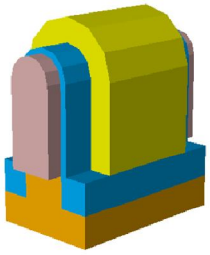

Fig.1 Partially Cylindrical FinFET [8]

The figure 2 shows Conventional FinFET (C-FinFET).

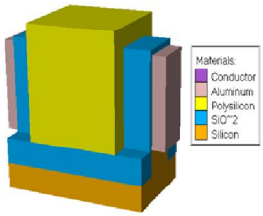

Fig. 2 Conventional FinFET [8]

Because of the overlapping of charges in the corner areas C-FinFET suffers corner effects and it results in self heating. The corners are rounded in PC-FinFET as seen in figure1. This rounding will decreases the self heating effect by allowing the heat flow easily [4]. Hence, the temperature is reduced. Further, it will increases carrier mobility and also the on-state current of the device (I_{on}). The PC-FinFET has better subthreshold slope, off-state current, on-state current, and Drain Induced Barrier Lowering than the C-FinFET. The gate capacitance of the PC-FinFET is lesser than that of C-FinFET thus lowering the intrinsic delay in PC-FinFET.

2.4 FinFET with tapered fin

Stress simulations [7] indicate that sloped sidewalls as in the figure 3 are mechanically more stable than the straight ones while influencing electrical performance minimally.

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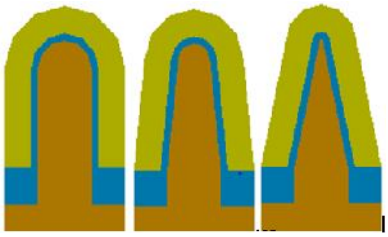

Fig. 3 PC-FinFETs with tapered fin [11]

The leakage usually happens in the middle region of the fin structure regardless of the fin shape. This is because the gate has more control over the fin periphery region as it is close to the gate. The region which is far away from the gate is the middle of the fin. So the gate has less control over this region. The leakage in the tapered fin [10] is 90% lower than in the rectangular fin because of the greater control of gate over the mid-fin. The on-state current follows the fin perimeter for all FinFET shapes. The 15 nm wide rectangular fin has 24% higher on-current than for the tapered fin. This is due to the combination of several factors, with 14% coming from the larger perimeter length, and the remaining 10% due to no overlapping electron distributions and no thin- layer induced mobility degradation that hamper the 5 nm wide fin top of the tapered FinFET. The greater gate control of the tapered fin improves DIBL and reduces Subthreshold Slope (SS) .Because of improved gate-to-channel controllability in the tapered FinFET, both the subthreshold swing and drain-induced barrier lowering were improved, and the OFF-state leakage current was lowered [11].

III.PROPOSED STRUCTURES

3.1 Inverse Triangular fin Structure

The triangular fin structure is kept upside down to get inverse triangular structure as shown in figure 4. Here the main advantage is that the ON current can be increased as the area at the top is increased. This top region is surrounded by gate.

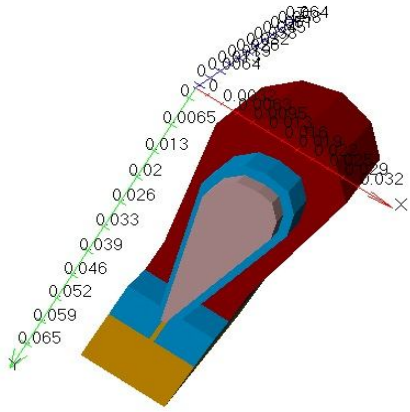

Fig. 4 Inverse triangular FinFET

3.2 Concave and Convex fin Structures

To reduce the leakage current in FinFETs, different fin structures have developed. The rectangular fin shaped structure has changed to partially cylindrical fin to reduce the corner effect. Later, trapezoidal FinFET and triangular FinFETs have developed. Figure 5 shows convex and concave FinFETs.

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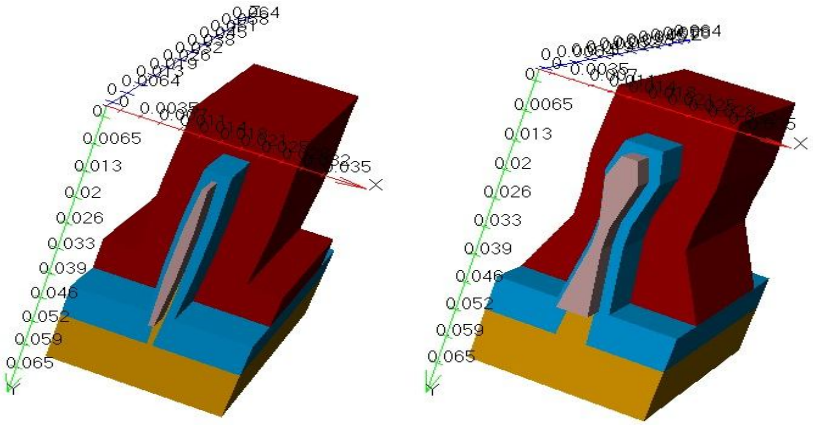

(a) (b)

Fig. 5 (a) Convex FinFET (b) Concave FinFET

The proposed concave and convex FinFETs provide better leakage control than the normal bulk-Si FinFETs or tri-gate devices with rectangular or trapezoidal fins. It is due to the formation of quasi-surrounding gate electrodes on concave and convex fins by a special Si etch process. Concave structure is curving in structure whereas; convex structure is curving out structure. The sharp edges are rounded to avoid the corner effect. I_{on}/I_{off} ratio is also improved. The difficulty lies in the fabrication of these structures because of the curved structure.

Concave structure can be formed by placing two triangular FinFETs, bottom one is placed straight and the top one is inversed. Convex fin is obtained by placing an inverse triangle at the bottom and the straight one at the top. So the fabrication of both structures is similar.

IV.RESULTS AND DISCUSSION

The analysis is done on 22nm bulk FinFET Technology model. Simulations are done by TCAD.

4.1 Threshold Voltage

Threshold voltage, V_{th} is extracted using the maximum transconductance method with V_d = 0.05 V. The variation of V_{th} with top width and doping concentration is studied [9].

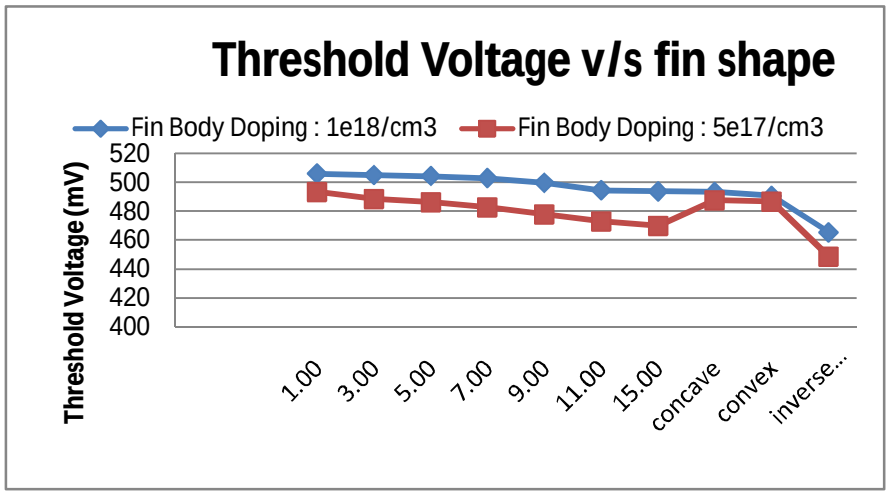

Fig. 6 Threshold voltage comparison of nFinFET as a function of fin shape

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From the figure 6, it is observed that threshold voltage increases when W_{top} decreases from 15 nm to 1 nm. V_{th} is within the range 496 mV to 506 mV when W_{top} varies from 15 nm to 1 nm. This is due to quantum confinement. In the case of concave and convex FinFETs, the threshold voltage has taken an optimum value, whereas in the case of inverse triangular FinFET, the value has lowered to 450 mV. Threshold voltage increases with increase in doping concentration. For an intrinsic semi conductor the threshold voltage will be negative.

4.2 Subthreshold Swing

The Subthreshold swing, SS decreases when W_{top} decreases and increases when doping concentration increases [2]. The SS is extracted at a gate voltage (V_g) of 0.3 V.

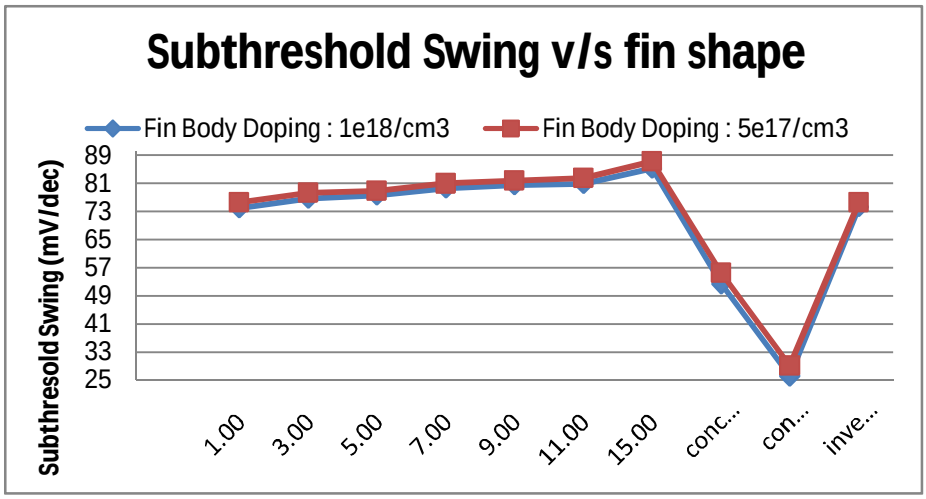

Fig. 7 Subthreshold Swing comparison of nFinFET as a function of fin shape

From the figure 7, it is clear that SS is directly proportional to the top width of the fin. Subthreshold swing total range is 11 mV/decade by fin shape variation from rectangular (W_{top} = 15 nm) to triangular (W_{top}=1 nm). Subthreshold swing is less than 85 mV/decade. In the case of concave and convex FinFETs, the SS is lowered below 60 mV/decade.

4.3 I_{on} Current

I_{on} current is extracted when V_{gs} and V_{ds} is V_{dd}.

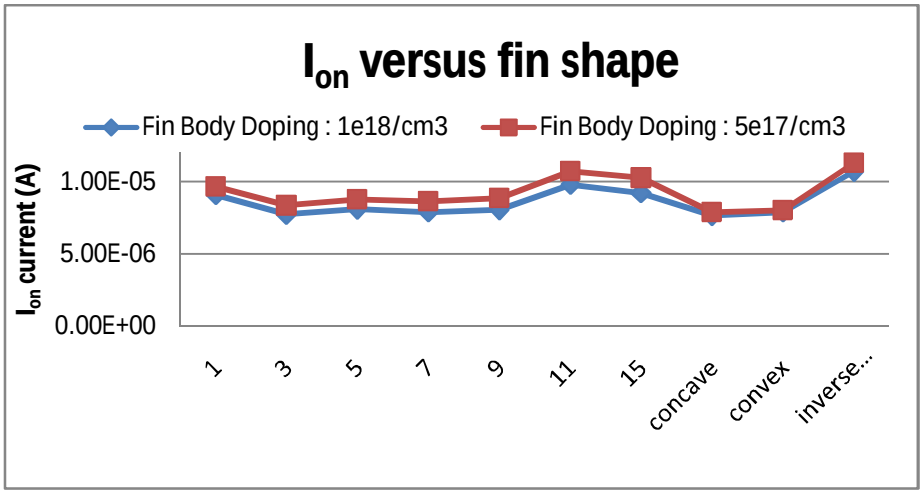

Fig. 8 I_{on} comparison of nFinFET as a function of fin shape

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Figure 8 shows that I_{on} current decrease as the fin width decreases. It is because of the decrease in charges per area. As doping is increased, I_{on} decreases due to mobility degradation.

4.4 Leakage Current and I_{on}/ I_{off} Ratio

MOSFET's drain leakage current or off-state current (I_{off}) is the drain current when no gate voltage is applied. It is the drain to source current which is extracted when V_{gs}=0 and V_{ds} = V_{dd}.

I_{off} current also decreases as the fin width decreases because the leakage current occurs at the middle of the fin, which is the more remote area from the gate. But as fin width decreases, the middle part of the fin has more control from the gate, so the leakage current decreases.

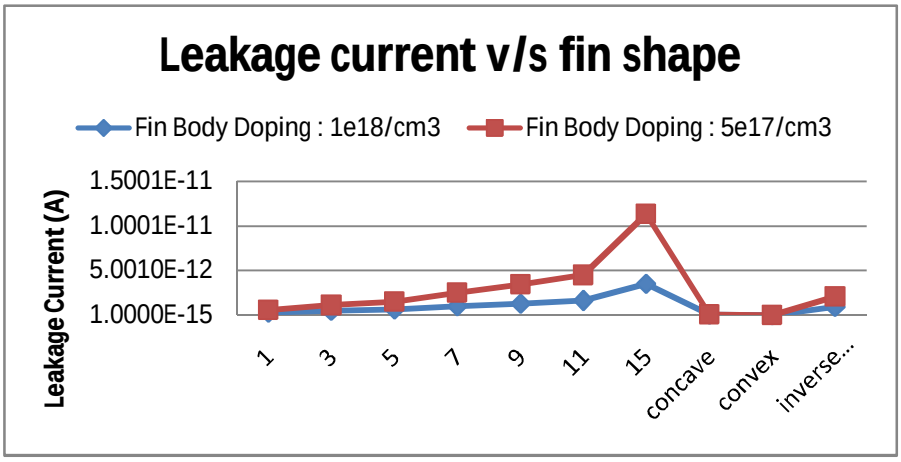

Fig. 9 Leakage current comparison of nFinFET as a function of fin shape

Figure 9 indicates as width increases, leakage increases. But in concave and convex FinFETs leakage is reduced more. Therefore, varying W_{top} between 1 nm to 15 nm produces a multitude of transistor design choices.

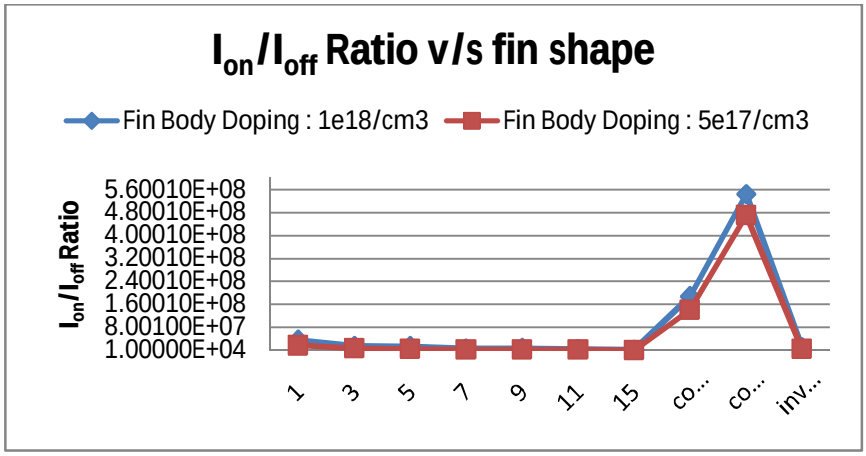

Fig. 10 I_{on}/I_{off} ratio comparison of nFinFET as a function of fin shape

The reduction in I_{on} with respect to the decrease in width is less compared to the reduction in I_{off}. Therefore, I_{on}/I_{off} monotonically increases as W_{top} decreases as seen in figure 10. Concave and convex FinFETs has better I_{on}/I_{off} as compared with triangular and rectangular FinFETs. When the doping increases, mobility degradation occurs, hence I_{on}

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decreases. As we increase the channel doping drive current reduces almost linearly, but off state current decreases exponentially. This leads to increase in I_{on}/I_{off} ratio very sharply.

Table 1 shows the comparison results of partially cylindrical, triangular, concave, convex and inverse triangular FinFETs in response with parameters like threshold voltage, subthreshold swing, leakage current, I_{on} current and I_{on}/I_{off} ratio.

Table 1 Comparison results

Parameters	Partially cylindrical	Triangular	Concave	Convex	Inverse triangular
Threshold Voltage (mV)	496.797	505.993	493.395	490.757	465
Subthreshold Swing (mV/dec)	85.29	74.04	52.41	26.20	74.30
Leakage current (pA)	3.511	0.2576	0.04085	0.01450	0.9154
I_{on} current (µA)	9.216	9.066	7.631	7.889	10.68
I_{on} / I_{off} ratio	2.624E+06	3.518E+07	1.867E+08	5.440E+08	1.167E+07

From the table 1 it is clear that the threshold voltage is in the range of 465 mV to 495 mV. Subthreshold swing is within the range of 26 mV/decade to 85 mV/decade. The leakage current is reduced in triangular by 90% when compared to partially cylindrical FinFET. It has reduced further to 94% in case of convex FinFET and 84% in case of concave FinFET. The ON current has reduced to 15% in concave and convex FinFETs when compared with triangular FinFET. It has increased to 15% in inverse triangular FinFET when compared to triangular FinFET.

VI.CONCLUSION

Triple-gate FinFET devices are one of the most assuring successors of conventional MOSFET devices. It is observed that rounding the corners of the fin reduces leakage current.

Fin shape has considerable impact on leakage performance. There is 90% reduction in leakage if the fin shape changes from rectangular to triangular. There is further 94% reduction in leakage current from triangular to concave and convex fin shapes. By using inverse triangular FinFET large drive current can be achieved. It has increased to 15% in inverse triangular FinFET when compared to triangular FinFET. The threshold voltage is in the range of 465 mV to 495 mV. Subthreshold swing is within the range of 26 mV/dec to 85 mV/dec.

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