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Modelling of Multi-Stacked Voltage Equalizer for Photovoltaic Array under Partial Shaded Conditions

M. S. Anandhi[1], R. Ramaprabha[2]

PG Student, Dept. of EEE, SSN Engineering College, Chennai, Tamilnadu, India[1]

Associate Professor, Dept. of EEE, SSN Engineering College, Chennai, Tamilnadu, India[2]

ABSTRACT: Photovoltaic (PV) systems have been developed into mature technology that has been used in specialized applications. Partially shaded photovoltaic system result in reduction of power generation and produces multiple maximum power points (MMPP) in the characteristics. In this paper, multi-stacked voltage equalizer is employed to solve this issue. Multi-stacked voltage equalizer is designed by incorporating inductor, capacitor, diode and filters in traditional SEPIC converter. Single Switch in this voltage equalizer reduces the complexity of the circuit. This equalizer receives the unbalanced voltages from PV array and makes it balanced by converter operation itself. Small amount of power generated is transferred from the un-shaded PV to shaded PV so that the entire PV array is operating at the same voltage. It is observed that voltage imbalance is slowly eliminated by this equalizer.

KEYWORDS: SEPIC converter, Partially shaded PV, Voltage equalizer, Power improvement.

I. INTRODUCTION

Renewable energy resources exist over wide geographical areas. Hence there is a strong support for promoting renewable sources such as solar power and wind power. Among those solar PV becomes popular for considering its advantages. The major issue in large arrays, building integrated PV systems, roof-top systems, etc is partial shading. This is more dominant in series connection of PV panels/arrays compared to other connections. Anyhow, series connection cannot be avoided as it is required for getting usable voltage ranges. Partially shaded PV array results in reduction in power generation and produces multiple maximum power points. When a panel/group of panels is shaded, then it is incapable of producing current and it experiences reverse bias voltage due to other currents produced by unshaded panels. Hot spots may be produced due to this. Hence bypass diode is connected in anti-parallel across each panel. But the introduction of bypass diode causes multiple peaks in the characteristics [1]. Improved maximum power point tracking algorithms are required to track the true peak power [2]. This problem can be solved by using voltage equalizer.

In this paper, a single switch voltage equalizer is used based on multi-stacked SEPIC converter. SEPIC converter can also be replaced by CUK, ZETA, Buck-Boost converters. The following sections describe the modelling of the equalizer.

II. OVERVIEW OF THE SYSTEM

Depending upon the requirement, 'N' number of PV panels is connected in series to obtain the desired voltage, called string. Group of panels receiving same illumination is called a substring. When each panel in a string/substring is equally illuminated/shaded, then the characteristics of P-V curve will have single peak. Conventional maximum power point tracker (MPPT) can be used to track the maximum power. In partially shaded PV array, due to the presence of multiple peaks, conventional MPPTs fail to track the true peak. The PV equalizer is used to solve the problems due partial shading [3]. Equalizer receives the unbalanced voltages from PV string and balances the voltage due to its unique operation.

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The block diagram of the partially shaded PV array with equalizer is shown in Fig. 1. For this paper, a PV array consists of 3 PV substrings are considered. For the equalizer circuit, single switch multi-stacked voltage equalizer is used in series with PV array as shown in Fig. 2.

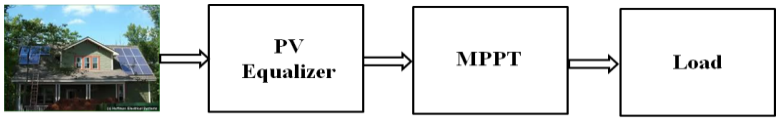

Fig. 1. Block diagram of the system

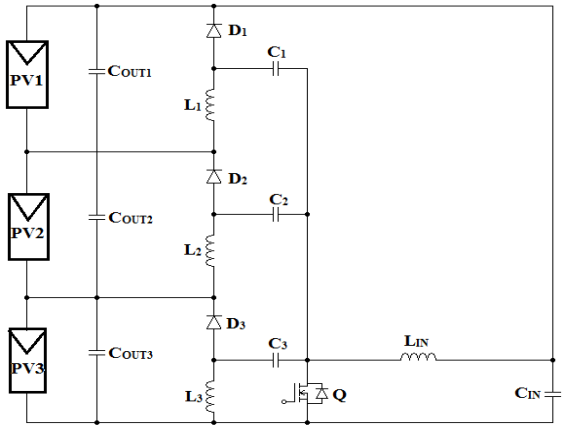

Fig. 2. Schematic of multi-stacked voltage equalizer

Voltage equalizer is derived by stacking capacitor, inductor, diode [CLD] filters in traditional SEPIC converter. The converter can also be any type of buck-boost such as CUK, ZETA etc. [4-5]. CLD filters have different voltage levels. SEPIC based converter is chosen because it does not require floating-gate driver and transformer compared to ZETA and CUK. Any number of substrings can be used but according to that number of CLD filters have to be increased. Thus component rating will be increased. Single switch used in this equalizer reduces the circuit complexity greatly [6-8]. The equalizer supplies the equalization current to all the substring so that all the voltages are balanced. Hence voltage equalizer eliminates the multiple peaks and voltage imbalance problem, consequently power output is increased.

III. OPERATION OF THE EQUALIZER

The system consists of shaded PV array, blocking diode and voltage equalization circuit based on SEPIC converter as shown in Fig. 1. Input voltage of the equalizer circuit is obtained from the output of the PV string voltage. The multi-output of this circuit is connected across each PV panel. The circuit shown in Fig. 2 consists of PV string capacitance (C_{IN}), input inductor (L_{IN}), MOSFET switch (Q), energy transfer capacitor (C_3), output inductor (L_3) and output filter capacitor (C_{OUT3}). The equalizer circuit is equivalent to that of conventional SEPIC converter and filter components. The three set of filter components namely, (C_{OUT1}, L_1, D_1, C_1), (C_{OUT2}, L_2, D_2, C_2) and (C_{OUT3}, L_3, D_3, C_3) represent the multi stage configuration. The advantages of this circuit include the usage of single switch, simple and easy to control. This circuit can be operated either in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). In this work, DCM mode is used as it eliminates the feedback control and limits the currents in the circuit with desired level.

Voltage equalization circuit performs a dc conversion function similar to the SEPIC converter. It can either increase or decrease the magnitude of the dc voltage. For analysing the configuration, consider three series connected PV panels with irradiation levels of 1000 W/m^2, 800 W/m^2 and 600 W/m^2 respectively. The equalizer configuration is operating in DCM for eliminating the feedback loop. The circuit operates in three modes which are explained below:

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MODE-1(T_{ON}): During mode-1(Fig. 3), the switch (Q) is in ON position; the output of series connected PV panels supply the power to the voltage equalization circuit. During this period, currents of all inductors (L_1, L_2 and L_3) in equalization circuit increases and the inductors store the corresponding energies. The current flowing through L_{IN} and C_{IN} also flows towards the switch (Q).

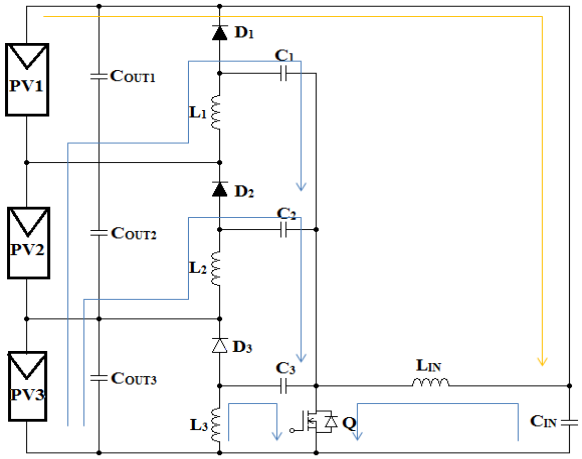

Fig. 3. Flow of currents in Mode 1

MODE-2(T_{OFF} -a): During mode-2 (Fig. 4), the switch (Q) is OFF. During this period, the diode corresponding to lowest voltage PV panel-3 will get forward biased. Hence, the stored energies in the inductors (L_1, L_2 and L_3) transferred to that PV module.

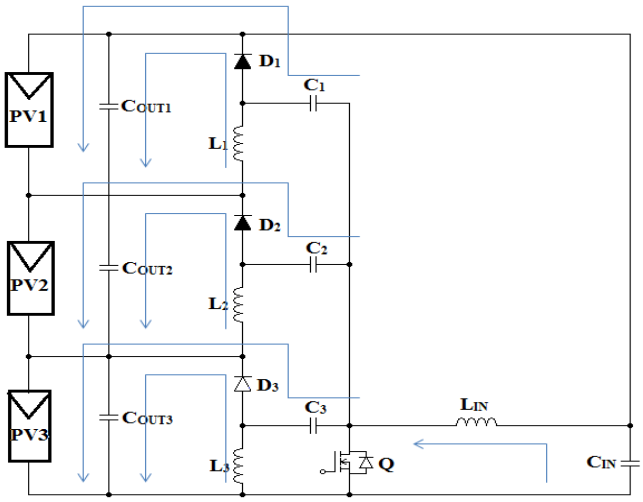

Fig. 4. Flow of currents in Mode 2

MODE-3(T_{OFF} -b): During mode-3 (Fig. 5), switch (Q) and diodes (D_1, D_2 and D_3) are in OFF position. During this period, inductor currents are constant and equal to zero and therefore the inductor voltage must be zero. After the current of diode (D_3) falls to zero, the currents in the equalizer inductors become constant or zero. In multi-stage SEPIC circuit, the average currents of D_1, D_2 and D_3 are equal to average currents of I_{L1}, I_{L2} and I_{L3} respectively. Therefore, the average currents of L_1, L_2 and L_3 are zero and only ripple current will flow through these inductors. As the large power generated by unshaded panels is transferred to the low illuminated panel through multi-stage SEPIC equalizing circuit, slowly imbalance of PV panel voltages vanishes.

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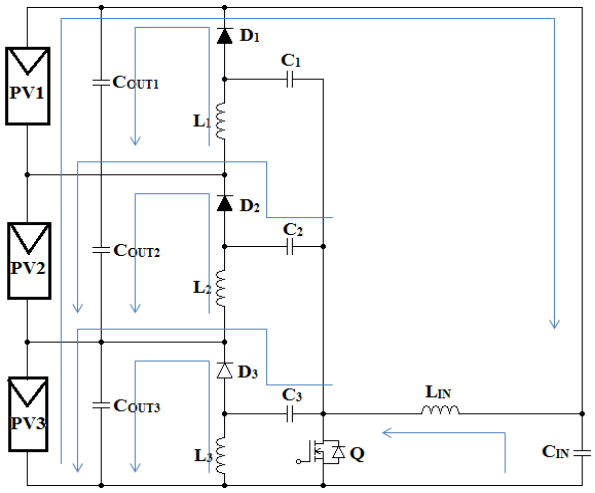

Fig. 5. Flow of currents in Mode 3

IV. SIMULATION RESULTS AND DISCUSSION

The components of the PV array with equalizer are modelled using MatLab-Simulink. The modelling circuits and results are discussed in this section.

A. MODELLING AND SIMULATION OF PV ARRAY

Fig. 6 shows the MatLab simulation model of partially shaded PV array (size of 3×1). Modelling has been carried out as per equations and procedures given in [9]. The parameters of PV array are listed in Table I.

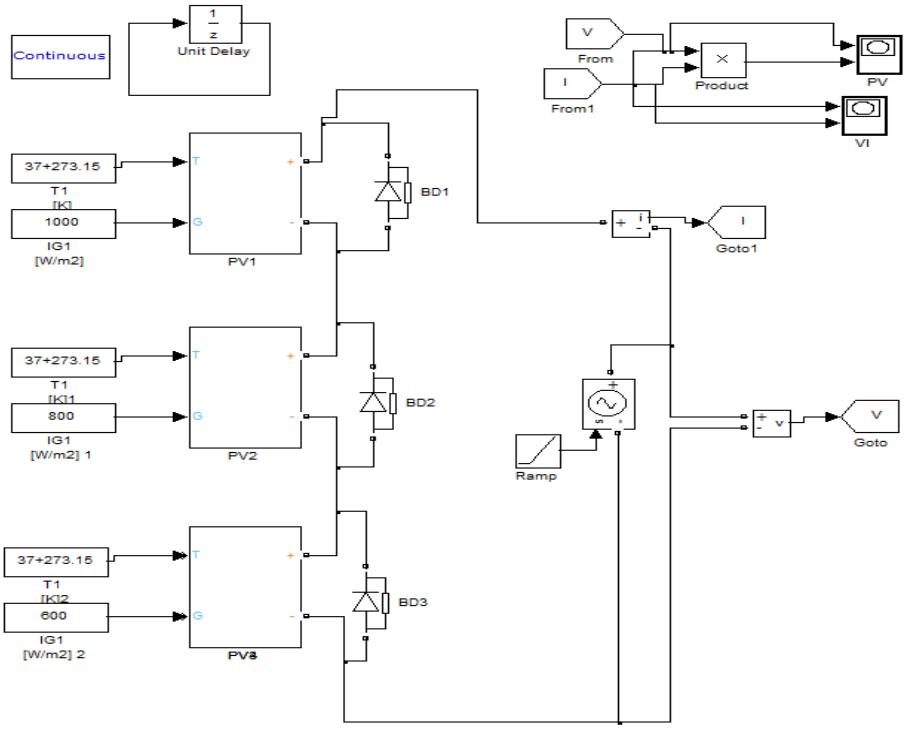

Fig. 6. MatLab model of photovoltaic array

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Table I. Parameters of SOLKAR SPV panel given in datasheet

S. No.	Parameters	Specifications
1	Rated Power (P_{max})	37.08 W
2	Voltage at Maximum power (V_{mp})	16.56 V
3	Current at Maximum power (I_{mp})	2.25 A
4	Open circuit voltage (V_{oc})	21.24 V
5	Short circuit current (I_{sc})	2.55 A
6	Size of solar panel	990 mm × 440 mm
7	Total number of cells in series	36 numbers
8	Cell arrangement (row × column)	6 × 6
9	Array size	3 × 1

Fig. 7 shows the I-V and P-V characteristics of PV array under equal illumination. The maximum power obtained with no shading condition is observed as 110 W with single peak.

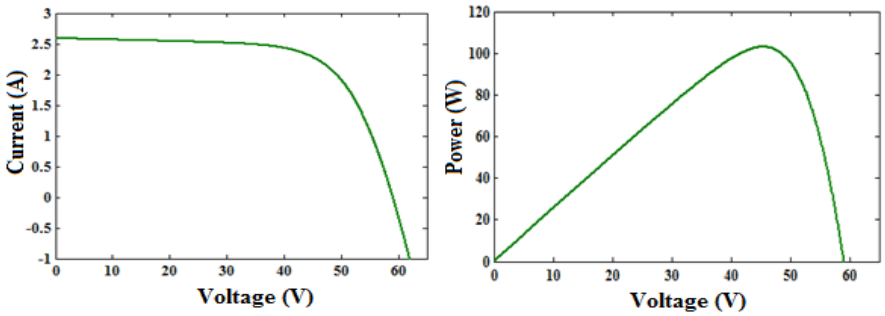

Fig. 7. V-I and P-V characteristics under equal insolation

Fig. 8 shows the I-V and P-V characteristics of partially shaded PV array. It is observed that multiple peaks are present in partial shading and number of peaks in the characteristics depend on the shading patterns. The peak power is observed as 75 W.

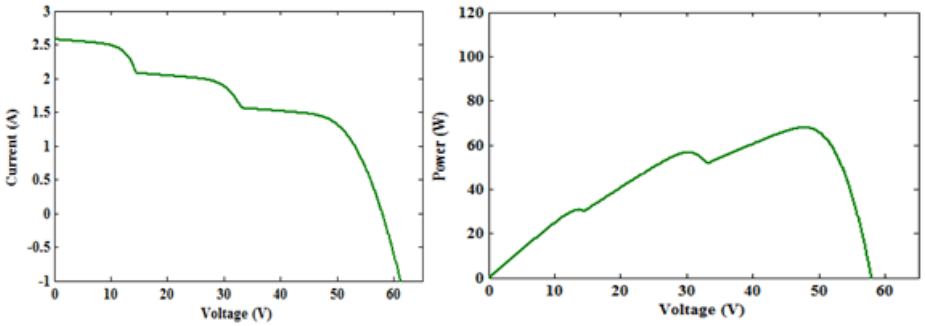

Fig. 8. V-I and P-V characteristics under partial shading

Fig. 9 shows the PV array characteristics without bypass diode and with same shading conditions. Here the multiple peaks are absent but power is reduced.

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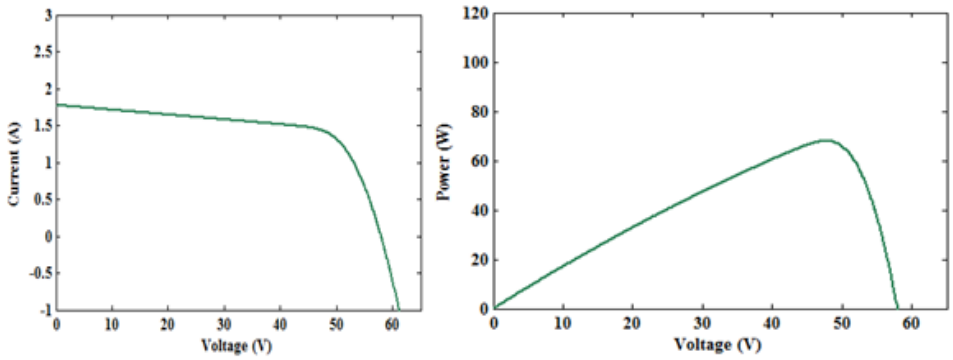

Fig. 9. V-I and P-V characteristics without bypass diode

B. SIMULATION OF EQUALIZER

The parameters of the multi-stacked voltage equalizer are given in the Table II. The parameters are designed as per the procedure given in [4-5, 10]. Fig. 10 shows the simulation model of multi-stacked voltage equalizer interfaced with PV.

Table II. Simulation Parameters

S. No.	Parameters	Specifications
1	Input capacitance	66µF
2	Input inductor	150µH
3	Switching frequency	200kHz
4	Coupling capacitor C_1,C_2, C_3	22µF
5	Inductance L_1, L_2, L_3	33µH
6	Smoothing Capacitor C_{OUT1},C_{OUT2}, C_{OUT3}	200µF

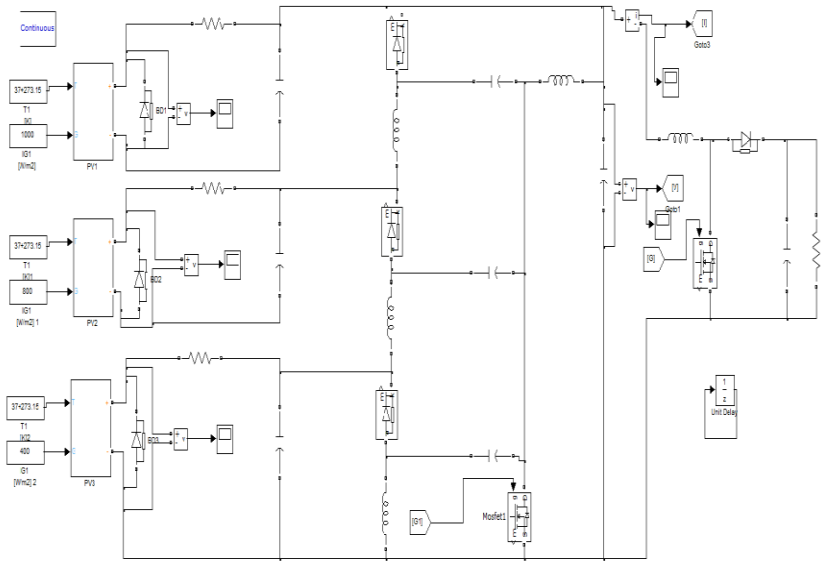

Fig. 10. MatLab model of voltage equalizer

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Fig. 11 shows the inductor currents of multi-stacked voltage equalizer where the current increases when the switch is turned ON and decreases when the switch is under the period T_{off-a}. It drops to zero for the period, T_{off-b}. Fig. 12 shows the coupling capacitor currents C_1, C_2, C_3 which increases along with the inductor current and reaches negative value before it starts to increase again. Fig. 13 shows the diode currents D_1, D_2, D_3 which starts conducting during T_{off-a} and reaches zero during T_{off-b}. Fig. 14 describes about switch voltage and input inductor current. Inductor current rises when switch is ON and falls when switch is OFF.

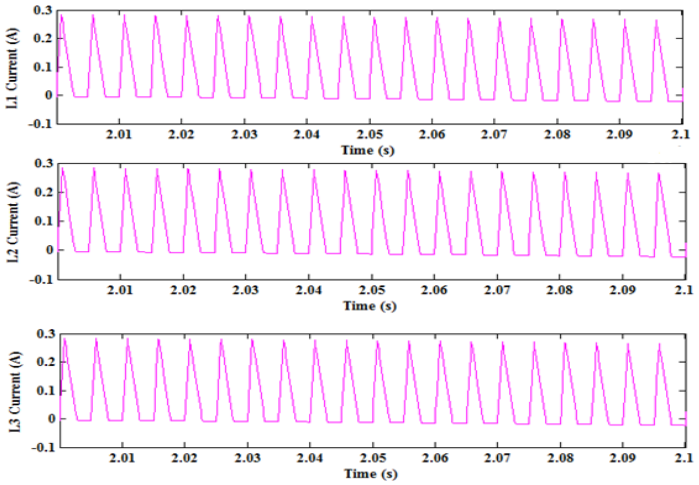

Fig. 11. Equalizer Inductor currents

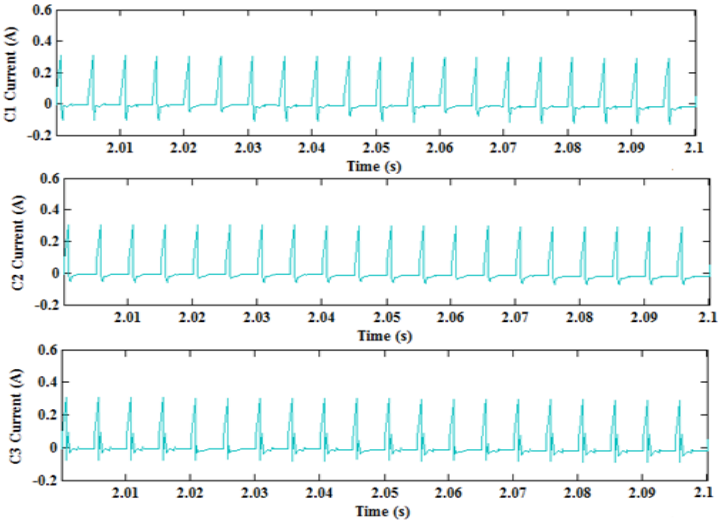

Fig. 12. Equalizer Capacitor currents

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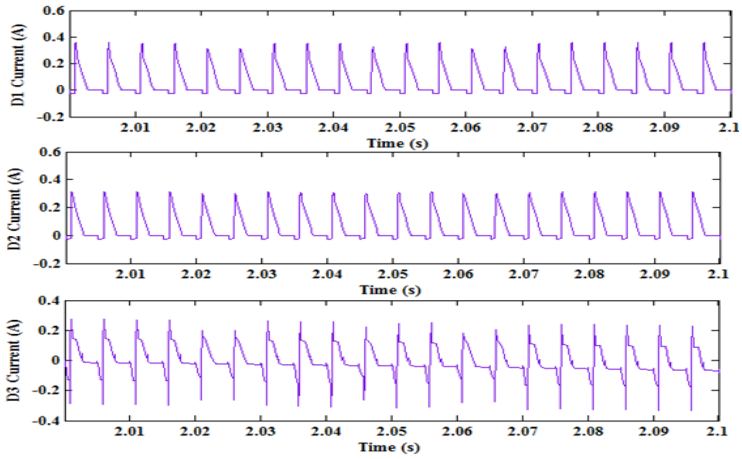

Fig. 13. Equalizer diode current

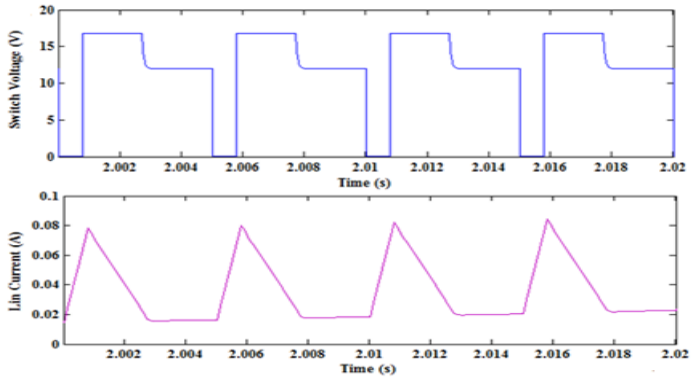

Fig. 14. Equalizer switch voltage and input Inductor current

Fig. 15 presents the comparative characteristics of partially shaded PV array to indicate the useful working of the voltage equalizer to improve power output. Power P_1 is obtained under equal illuminated condition. In the case of partial shading with bypass diode the power P_3 is less and multiple peaks are present. Power P_4 shows drastic reduction without using bypass diode. Compared to P_3 and P_4, power P_2 is better and also eliminates voltage imbalance with the help of equalizer.

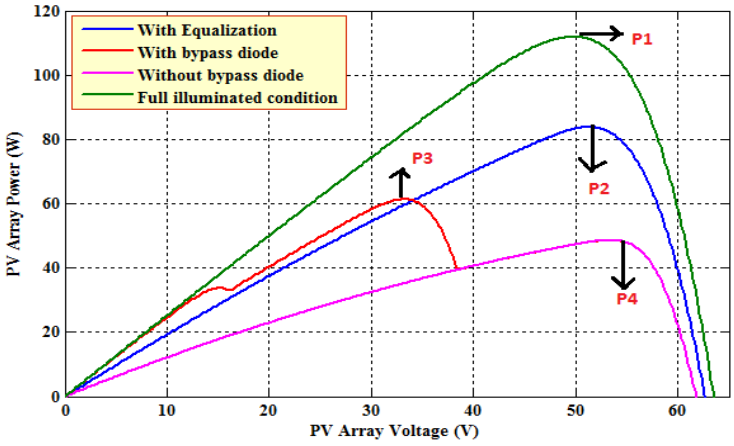

Fig. 15. Comparison of PV array characteristics

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Table III consolidates the results of PV array output at different scenarios.

Table III. Comparison of PV Array results

Methods	Voltage, V_{MPP} (V)	Power, P_{MPP} (W)	Power output
Full illuminated condition	49.86	111.90	100 % (Expected power)
Without bypass diode	53.37	48.60	43.43 % of expected power
With bypass diode	33.13	61.33	54.80 % of expected power
With Equalization	51.29	83.84	74.92 % of expected power

V. CONCLUSION

Multi-stacked voltage equalizer under partial shaded conditions have been modelled and simulated to obtain voltage equalization strategy. Single switch arrangement in this topology has reduced the circuit complexity to a greater extent compared to conventional multi-stacked converters. Photovoltaic system characteristics under partial shaded conditions are obtained for equalization and without equalization strategy. There is around 20% power improved when using equalizer compared to PV array with bypass diode strategy and 32% power improvement compared to PV array without bypass diode. Moreover, no multiple peaks present hence conventional MPPT can be used. The SEPIC based equalizer can be realized using any other derived converter to implement the equalization technique.

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