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Design of Low Power Aging Aware Multiplier Using Adaptive Hold Logic

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ABSTRACT: Digital multipliers are among the most arithmetic functional units in many applications, such as Fourier transform, discrete cosine transforms, and digital filtering. These applications depends on multipliers, if the multipliers are slow, the performance of entire circuits will be reduced. The proposed aging-aware multiplier design is implemented with a novel adaptive hold logic (AHL) circuit. The multiplier is based on variable-latency technique and adjust the AHL circuit to achieve reliable operation using NBTI and PBTI effects The AHL circuit can decide the input patterns require one or two cycles to adjust the judging criteria to ensure the minimum performance degradation after considerable aging occurs. Comprehensive analysis and comparison of the multipliers performance under different cycle periods to show the effectiveness of our proposed architecture. The performance in 16- and 32-bit multipliers, can be easily extended to large designs. It can provide reliable operations even after the aging effect occurs. The Razor flip-flops detect the timing violations and re-execute the operations using two cycles. The architecture will adjust the percentage of one-cycle patterns to minimize performance degradation due to the aging effect. When the circuit is aged, and many errors occur, the AHL circuit uses the second judging block to decide if an input is one or two cycles. The multiplier is adjust the AHL to mitigate performance degradation due to increase delay.

KEYWORDS: Adaptive hold logic (AHL), variable latency, negative bias temperature instability (NBTI), razor flip flop

I.INTRODUCTION

Multiplication is an essential arithmetic operation for common DSP applications, such as filtering and fast Fourier transform (FFT). To achieve high execution speed, array multipliers are widely used. To increase the operating voltage to compensate for then NBTI induced delay degradation. The voltage scaling also increases the dissipation of dynamic power quadratically, which in turn increases the temperature of circuit, it ultimately accelerates the NBTI effect.. The fastest types of multipliers are parallel multipliers. The Wallace multipliers are also fastest. High-performance and low power are primary concerns, Booth multipliers tend to be the primary choice. The Modified Booth algorithm achieves a performance improvement through the radix-4 encoding. The binary array multiplier follows the same strategy as the Booth architecture, the reduction of the partial product terms, while keeping the regularity of an array multiplier. The optimized array multipliers present reduction in terms of delay and power consumption, to improve the efficiency of the array multiplier.

Negative bias temperature instability (NBTI) occurs when a pMOS transistor is under negative bias (Vgs = −Vdd). Traditional circuits use critical path delay as the overall circuit clock cycle in order to perform correctly. The probability that the critical paths are activated is low. The path delay is shorter than the critical path. For noncritical paths, using the critical path delay as overall cycle period will result in timing waste. The variable latency design was proposed to reduce the timing waste of traditional circuits. It divides the circuit into two parts: 1)shorter paths 2)longer paths. Shorter paths can execute in one cycle, whereas longer paths uses two cycle to execute the operation. When shorter paths are activated frequently, the variable latency is better than traditional designs.

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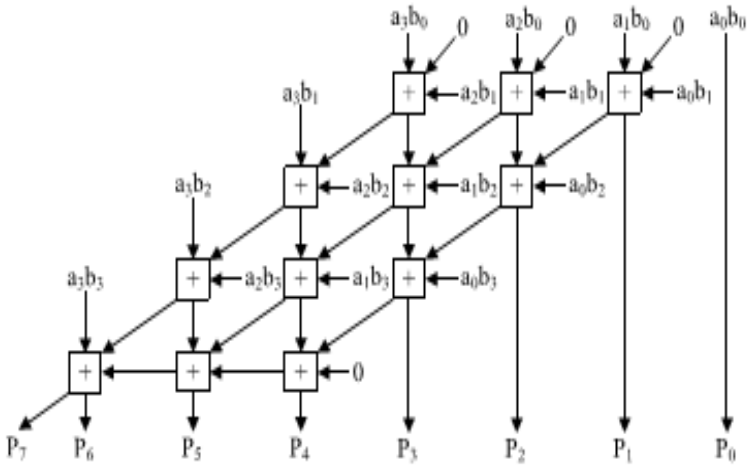

Fig. 1. 4x4 Array Multiplier.

II. PRELIMINARIES

A. Column-Bypassing Multiplier

The NBTI, forward body biasing (FBB), and voltage scaling (VS), they affect the values of design parameters which include threshold voltage, leakage power, dynamic power, temperature, and delay. A column-bypassing multiplier is an improvement of the normal array multiplier (AM). The AM is a fast parallel AM and is shown in Fig. 1. The multiplier array consists of (n−1) rows of carry save adder (CSA), in which each row contains (n − 1) full adder (FA) cells. Each FA in the CSA array has two outputs: 1) the sum bit goes down and 2) the carry bit goes to the lower left FA. The last row is a ripple adder for carry propagation. The FAs in the AM are always active regardless of input states. A low-power column-bypassing multiplier design is proposed in which the FA operations are disabled if the corresponding bit in the multiplicand is 0.

B. Row-Bypassing Multiplier

The row-bypassing multiplier is also used to reduce the activity power of the AM. The operation of the row-bypassing multiplier is similar to the low-power column-bypassing multiplier, but the selector of the multiplexers and the tristate gates use the multiplicator.

C. Variable-Latency Design

The variable-latency design is used to reduce the timing waste occurring in traditional circuits that use the critical path cycle as an execution cycle period. To execute a shorter path using a shorter cycle and longer path using two cycles. Since most paths execute in a cycle period that is much smaller than the critical path delay, the variable latency design has smaller average latency.

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III.PROPOSED WORK

The proposed aging-aware Multiplier design introduces the overall architecture and the functions of each component and design AHL circuit when significant aging occurs.

A. Proposed Architecture

Aging-aware multiplier architecture includes two m-bit inputs (m is a positive number), one 2m-bit output, one column- or row-bypassing multiplier, 2m 1-bit Razor flip-flops, and an AHL circuit.

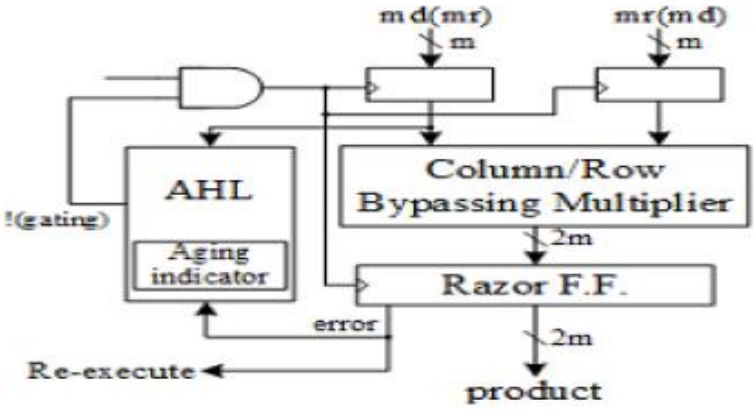

Fig. 2.Proposed architecture (md means multiplicand; mr means multiplicator).

B. Razor Flip Flop

Razor flip-flops can be used to detect the timing violations occur before the next input pattern arrives. A 1-bit Razor flip-flop contains a main flip-flop, shadow latch, XOR gate, and multiplexer. The main flip-flop catches the execution result for the combination circuit using a normal clock signal, and the shadow latch catches the execution result using a delayed clock signal, which is slower than the normal clock signal. If errors occur, the Razor flip-flop will set the error signal to 1 to notify the system to re-execute the operation and notify the AHL circuit that an error has occurred.

C. Adaptive Hold Logic

The AHL circuit is the key component in variable-latency multiplier. When input patterns arrive, the column- or row-bypassing multiplier, and the AHL circuit execute simultaneously. According to the number of zeros in the multiplicand or multiplicator, the AHL circuit decides the input patterns require one or two cycles. If the input pattern requires two cycles to complete, the AHL will output 0 to disable the clock signal of the flip-flops. The AHL will output 1 for normal operations. When the column- or row-bypassing multiplier finishes the operation, the result will be passed to the Razor flip-flops.

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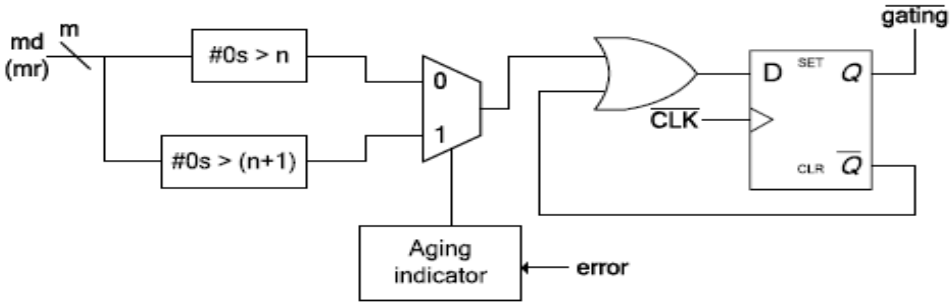

Fig.3.Novel Agaptive Hold Logic

IV. SIMULATION RESULT

The below figure shows the Simulation output waveform of the 4 x 4 multiplier.

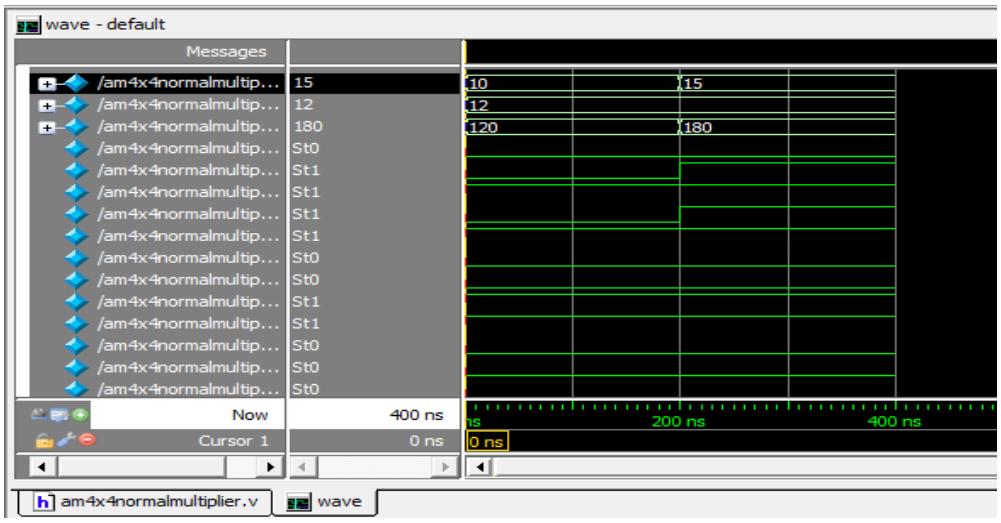

Fig.4. 4x4 Array Multiplier

IV.CONCLUSION

In this paper, an aging-aware variable latency multiplier design with the AHL. The multiplier is able to adjust the circuit to mitigate performance degradation due to increased delay. Multipliers have less performance degradation due to less timing waste, but traditional multipliers need the degradation. The experimental results show the architecture with 4x4 multiplication it will decrease the delay and improve the performance.

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