ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

Dual Supply Based Low Power 10T SRAM Cell Structures (DS10T)

Manish Shrivas[1], Saima Ayyub[2], Paresh Rawat[3]

PG Student [VLSI], Dept. of ECE, Truba Engineering College, Madhya Pradesh, India[1]

Assistant professor, Dept. of ECE, Truba Engineering College, Madhya Pradesh, India[2]

HOD , Dept. of ECE, Truba Engineering College, Madhya Pradesh, India[3]

ABSTRACT: This paper presents a novel scheme for designing a low power SRAM cell. The cell achieves low power dissipation due to its stack transistors connected to two different supplies driven by headline and its complement. This paper investigates the impact of process on read access time, write access time, write power and layout area. And finds appreciable improvement in write access time and write power dissipation. This method obtains 34.3% and 73.2% improvement in writing power compare to WRE8T and 6T respectively. Similarly, write access time reduced up to 91.4% reduction in write access time as compare to LP10T. The layout area of proposed cell is same as WRE8T. This article presents the simulation of 6T, 9T, LP10T, WRE8T and proposed SRAM cells. All the simulations have been carried out on 90nm at Microwind EDA tool.

KEYWORDS: Cache Memory, CMOS, Read Access Time, Read Power.

I.INTRODUCTION

In the memory hierarchy L1 and L2 SRAM is the workhorse of the processor designs. High speed portable devices require primary memory that responds faster. For that purpose, static random access memory (SRAM) is used, which is faster and refreshing is not needed again and again. Dynamic power dissipation is the main issues of high speed SRAM cells because this unwanted power dissipation reduces the battery backup life of portable devices. So it is required to have a SRAM cell design, having both faster read, faster write and low dynamic power dissipations.

As the CMOS process technology continues to scale to the nanometer regime, process variation and leakage current of transistors become more severe, which are further aggravated by the fluctuation of the operation conditions such as the variation of the supply voltage and/or the temperature leads to a higher chance of device malfunctioning. For example, as indicated in [1], the impact of the threshold variation could be exponential.

An on/off current ratio is often used as a gauge for this issue, where the on-current refers to the cell current drawn by an accessed cell during the read operation from the sensing bitline while the off-current refers to the leakage current drawn by all the other unaccessed cells from the other complementary bitline on the same column[2]. Typically, a rule of thumb demands that this on/off ratio is greater than 10 so that there will be adequate voltage swing between the bitline pair at the moment when the sense amplifier is activated to ensure reliable read operation.

To avoid these short channel effects, oxide thickness scaling and higher and non uniform doping need to be incorporated [3] as the devices are scaled. The low oxide thickness gives rise to a high electric field, resulting in considerable direct tunnelling current [4]. Higher doping results in a high electric field across the reverse biased p–n junctions (source-substrate or drain substrate) which cause significant band to band tunnelling (BTBT) of electrons from the valence band of the p region to the conduction band of the n region. Peak halo doping (P+) is restricted such that the BTBT component is maintained reasonably small compared to the other leakage components. In another technique [5], a low area overhead adaptive body bias (ABB) circuit is proposed to compensate for aging and process variations to improve the SRAM reliability and yield. The p ABB circuit consists of a threshold voltage sensing circuit and an on chip analog controller for power reduction. A multi threshold complementary metal oxide semiconductor (MTCMOS) technology provides low leakage and high performance operation by utilizing high speed, low threshold

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

voltage (LVT) transistors during active mode and low leakage, high threshold voltage (HVT) transistors during sleep mode, which reduces the static power dissipation of the SRAM circuit [6,7].

In this proposed work, low power SRAM cell topologies are studied and simulated. 6T SRAM cell suffer with severe power dissipation. To avoid this problem 9T, LP10T and WRE8T was proposed with stack transistor introduced. Now, Proposed work on dual supply based low power 10T SRAM cell(DS10T) perform better performance than existing SRAM cell.

The remaining part of paper is organized in the following order. Section II presents proposed design and device sizing. Simulation results and discussion are considered in Section III. Finally, the concluding remarks are provided in Section IV.

II. REVIEW ON DIFFERENT SRAM DESIGN ARCHITECTURE

It considers This article presents the simulation of 6T, 9T, LP10T, WRE8T and Proposed SRAM cells. All the simulations have been carried out on 90nm at Microwind EDA tool.

1. 6T SRAM cell

The basic 6T SRAM cell was proposed by Kim TH et al, 2008[8] on Fig.1 shows the circuit diagram of a conventional SRAM cell [8]. Before the read operation begins, the bit line (BL) and bitbar line (BLB) are precharged to as high as supply voltage Vdd. When the word line (WL) is selected, the access transistors are turned on. This will cause a current to flow from supply voltage (Vdd) through the pull up transistor TP1 of the node storing ‘‘1’’. On the other side, current will flow from the precharged bitbar line to ground, thus discharging bitbar line. Thus, a differential voltage develops between the BL and BL. This small potential difference between the bit lines is sensed and amplified by the sense amplifiers at the data output. Here, TP1/TP2 is used as pull up transistor, TN1/TN2 is used as pull-down transistor and TN3/TN4 are used as access device for read and write.

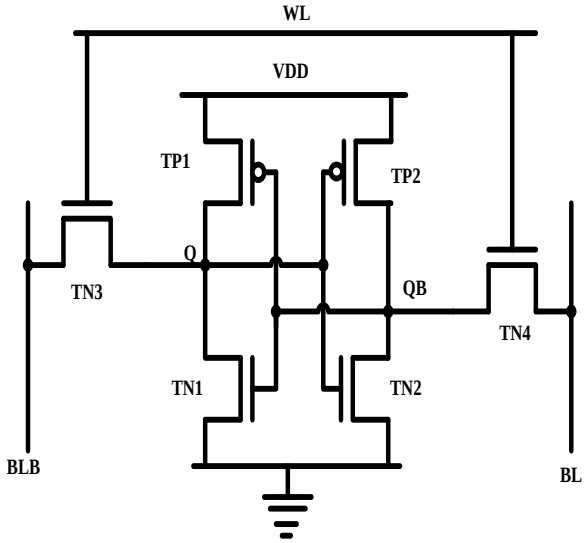

Fig.1 Conventional 6T SRAM cell[8]

.

2. 9T SRAM cell

The modified 9T was introduced by Liu Z et al, 2008[9] is shown in Fig.2. Write occurs just as in the 6T SRAM cell. Reading occurs separately through N5, N6 and N7 controlled by the read signal (RWL) going high. This design has the problem of the high bit line capacitance with more pass transistors on the bit line. Here, P1/P2 is used as pull up transistor, N1/N2 is used as pull-down transistor and N3/N4 is used as access device for write only.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

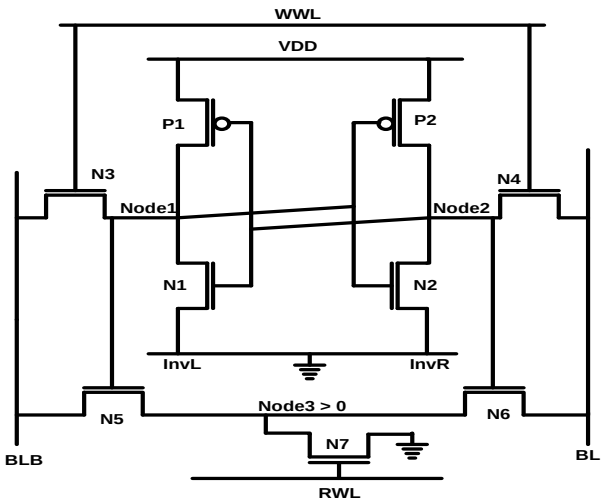

Fig.2 9T SRAM Cell[9]

3. *Fully Differential Low Power 10T SRAM*

Singh S et al, 2012 proposes the fully differential low power 10T SRAM [10] bit cell is shown in Fig.3. The design strategy of cell is the series connection of a tail transistor. The gate electrode of this device is controlled by the output of an XOR gate, inputs of which are tapped from write word line (WWL) and read word line (RWL) control signals coming from the WWL and the RWL drivers. The XOR gate and the tail transistor are shared by all the cells in a row. The tail transistor has to be appropriately up sized for sinking currents from all the cells in the row. Without this read buffer, a cell with such small drivers and series connected tail transistor would exhibit unacceptably low read static noise margin (RSNM), resulting in read instability. Here, MP1/MP2 is used as pull up transistor, MN1/MN2 is used as pull-down transistor, MN3/MN4 is used as access device for write only and MN5 used as leakage controlling transistor during read and write.

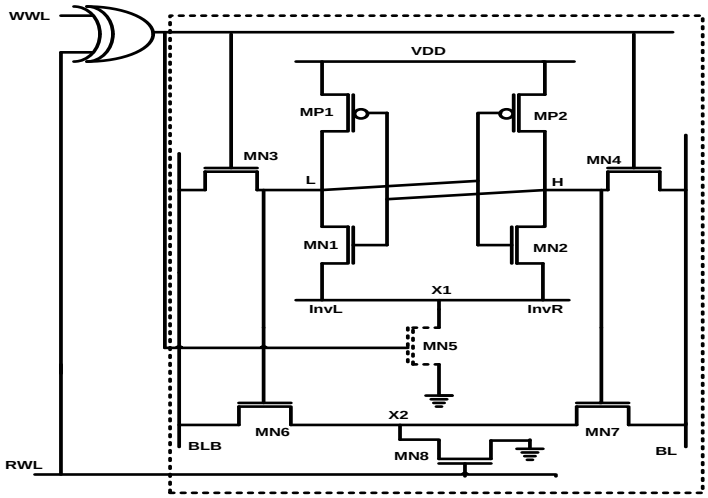

Fig.3. Fully Differential Low Power 10T SRAM (LP10T)[10]

4. *Write and Read Enhanced 8T SRAM cell (WRE8T)*

Recently, new WRE8T proposed by Ghasem Pasandi et al, 2014 on Fig. 4 shows circuit diagram of 8T SRAM cell[12]. In this cell, M5 is write access transistor and M6 is for read access. Having individual access transistors in our cell, it is

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

possible to increase size of write access transistor to improve write-ability and choose minimum size for read access transistor to enhance read stability, whereas in 6T there is a conflict while sizing the access transistors. In the proposed SRAM cell, the added PMOS and NMOS transistors (M7, M8) become OFF during write operation. This interrupts VDD and GND connections of the left inverter in the cell. Thus, left inverter becomes weaker during write operation, and a relatively stronger write access transistor can easily write the input to our cell.

In WRE8T, before read operation bit-line of read (BLT) is precharged to VDD, and then by asserting RWL signal, M6 (Fig. 4) becomes ON and according to the stored data at node q, the capacitance of BLT bit-line is discharged or remains unchanged. Here, M3/M4 is used as pull up transistor and M1/M2 is used as pull-down transistor.

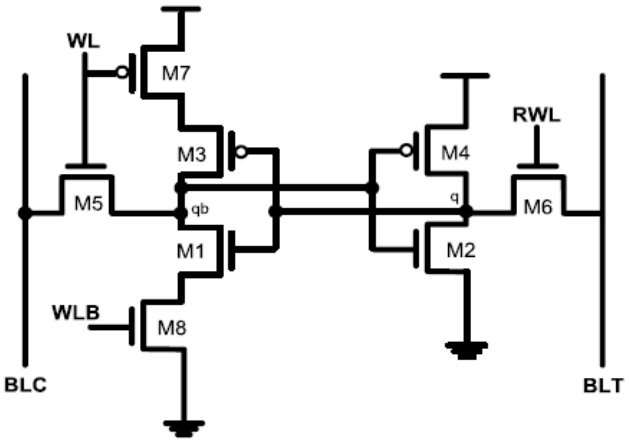

Fig.4 Write-And-Read-Enhanced 8T SRAM cell (WRE8T)[12].

III. PROPOSED SRAM DESIGN

In this scheme, In proposed cell, M5 is write access transistor and M6 is for read access. Having individual access transistors in our cell, it is possible to increase size of write access transistor to improve write-ability and choose minimum size for read access transistor to enhance read stability, whereas in 6T there is a conflict while sizing the access transistors. In the proposed SRAM cell, the added pMOS and nMOS transistors (M7, M8) become OFF during write operation and transistors (M9, M10)are used to control dynamic power supply which is controlled by WL/WLB(Fig.5).

In proposed, before read and write operation WL/WLB is used to control two kind of supply VddL and VddH for right sided inverter. Supply VddL connected to right sided inverter during standby mode, while VddH connected to right sided invereter during read or write. The flow chart of proposed design methodology shown in Fig.6. Here also, M3/M4 is used as pull up transistor and M1/M2 is used as pull-down transistor.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

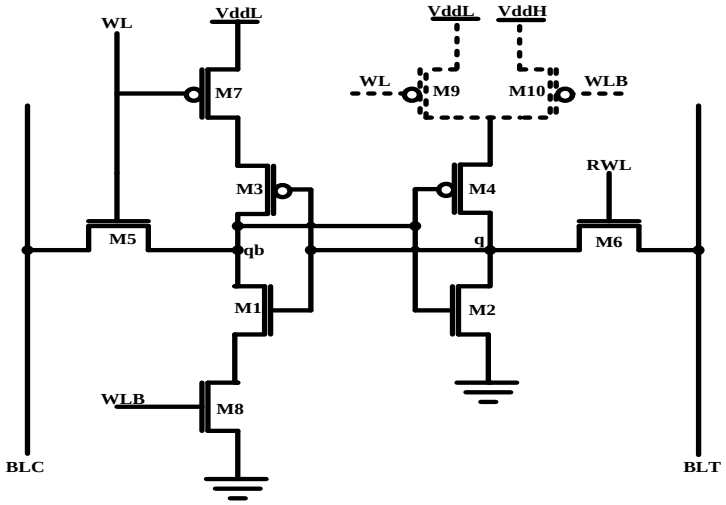

Fig.5 Dual Supply Based Low Power 10T SRAM Cell (DS10T)

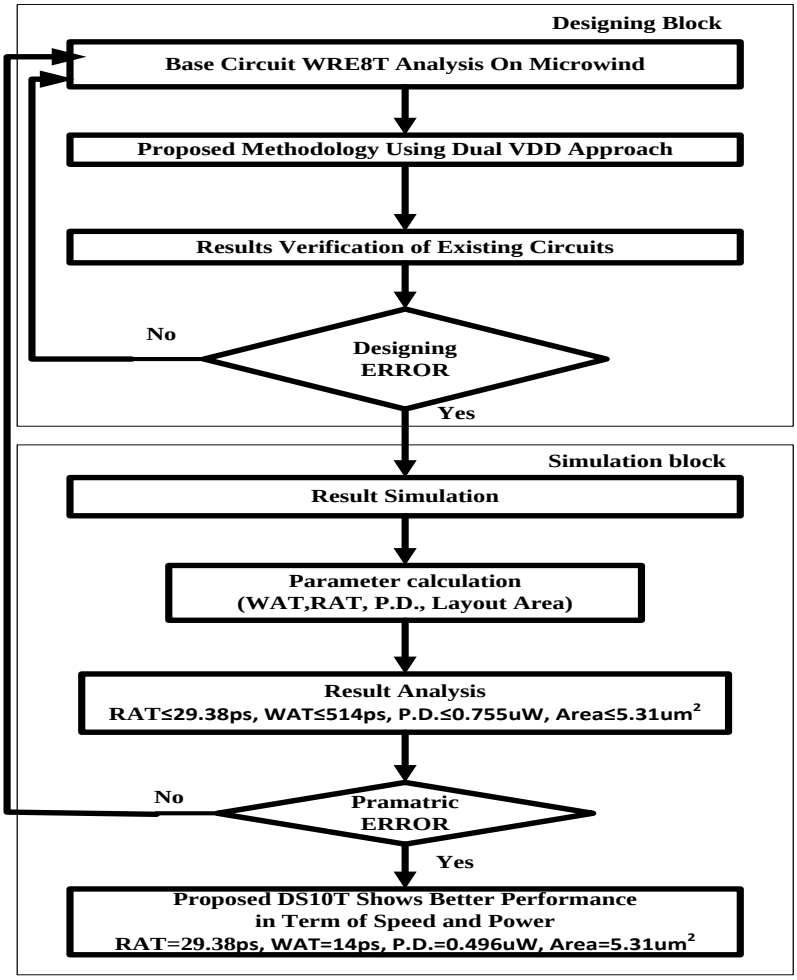

Fig.6 Design Flow

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

IV. SIMULATION RESULTS AND DISCUSSION

Spectrum sensing: All the circuits have been simulated using 90 nm technology on MicroWind tool. To make the impartial testing environment all the circuits has been simulated on the same input patterns.

1. *Write Power*

Fig. 7 shows comparision of write power dissipation. Write power depends on the write delay. Similarly, the standby leakage in embedded cache is an alarming issue in deep-submicrometer technology. The leakage current is one of the major contributors to the total power dissipation in an SRAM cell because a major part of the cache remains idle most of the time except for the row being accessed. The total leakage current in an SRAM cell mainly (ignoring other minor leakage components such as I_{GIDL} and *I*punchthrough) consists of the subthreshold leakage current (I_{sub}), the gate leakage current (I_g), and the BTBT (band-to-band tunneling) or junction leakage current (I_{JN}) through different devices. It is observed that LP10T consume lowest power. Proposed technique consumes lowest write power among the existing low power SRAM cell. Proposed cell consume 73% smaller write power as compare to 6T. The write power govern by following expression mentioned below:

$$P_{write}=C.f.\ (V)^2 \quad \ldots\ldots(1)$$

Where, C internal node capacitance, f operating frequency and V is power supply voltage.

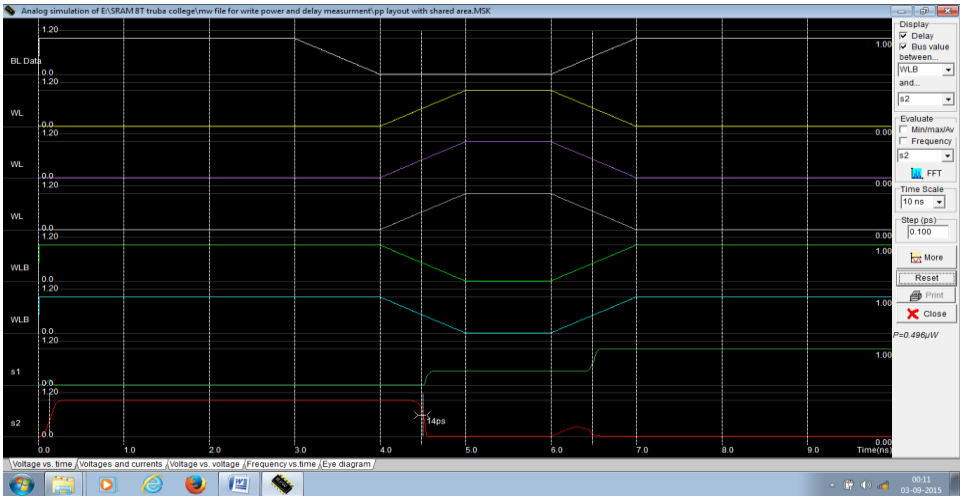

Fig. 7(a) Write Delay measurement on microwind

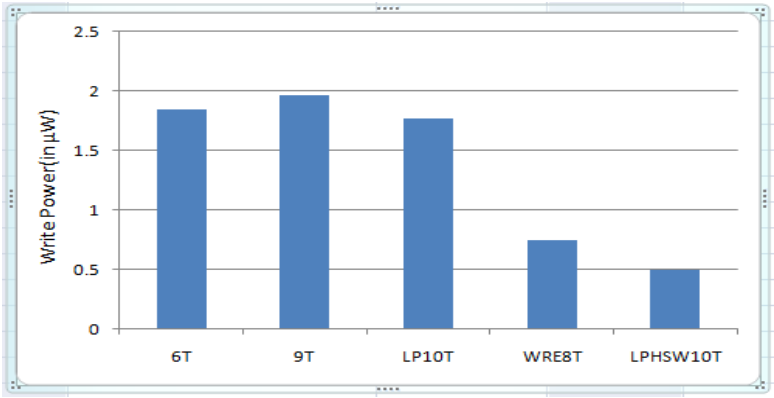

Fig. 7(b) Comparison of write power

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

2. *Read Access Time(RAT)*

Fig. 8 shows comparision of read access time. *T*RA (read access time or read delay) is estimated from the time when RWL (WL) (wordline) is activated to the time when bitline (BL)/bitline bar(BLB) is discharged by 50 mV from its initial high level [13]. The 50-mV differential between BL and BLB is good enough to be detected by a sense amplifier, thereby avoiding misread [13], [14]. It is observed that Proposed SRAM cell has equal read access time like WRE8T and 24.5%(1.35%) higher than 6T(LP10T).

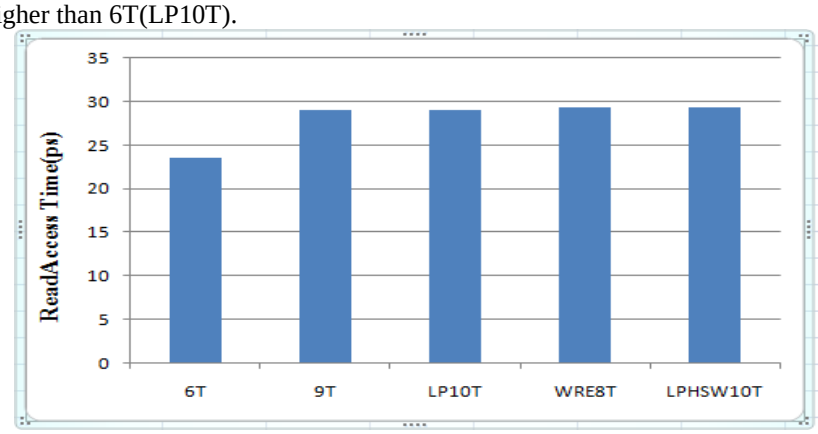

Fig. 8 Comparison of read access time

3. *Write Access Time(WAT)*

Fig. 9 shows comparision of write access time. *T*WA (write access time or write delay) is estimated as the time required for writing "0" to storage node "L" from the time when WWL(WL) is activated to the time when "L" falls to 10% of its initial high level (i.e., its 90% swing). Similarly, *T*WA for writing "1" to "L" is estimated from the time when WWL (WL) is activated to the time when "L" rises to 90% of its full swing from its initial low level. This avoids miswrite. Proposed cell offers faster write as compare to existing cell like 6T, 9T, LP10T and WRE8T.

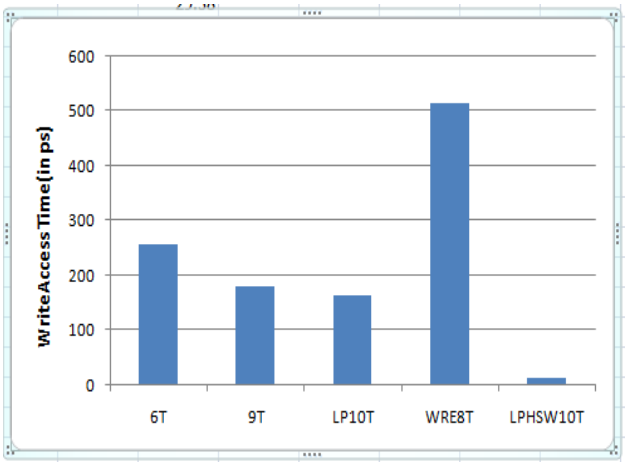

Fig. 9 Comparison of write access time

4. *Layout Area*

Fig. 10 shows comparison of layout area. It is observed that proposed SRAM occupies similar area like WRE8T and occupies 5% more area than LP10T. Additionally, proposed cell occupy 2% more area due to transistors M9and M10, Which is common for pair of cell in single row. Layout area provide information about bit line capacitance, internal node capacitance, read access time, write access time and packaging density of SRAM. Proposed cell layout shown in

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

Fig. 11. The width over length ratio of layout used to calculate layout area according to λ rule. Where λ is design parameter.

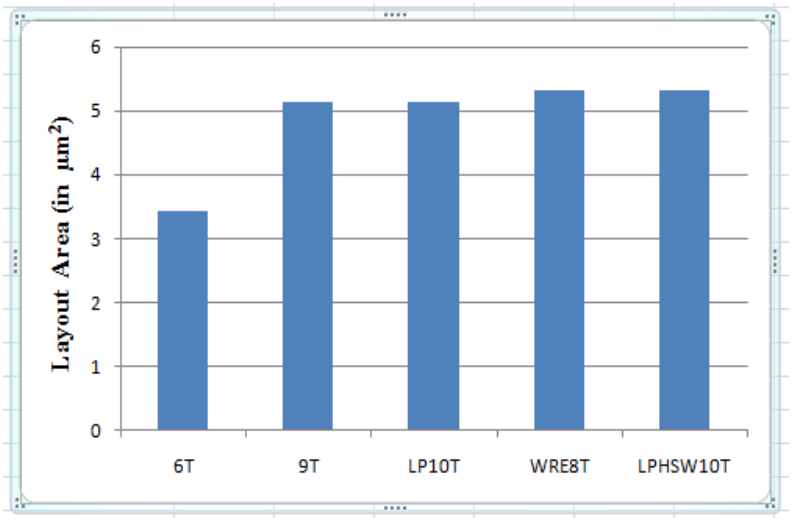

Fig. 10 Comparison of various SRAM cell layout area.

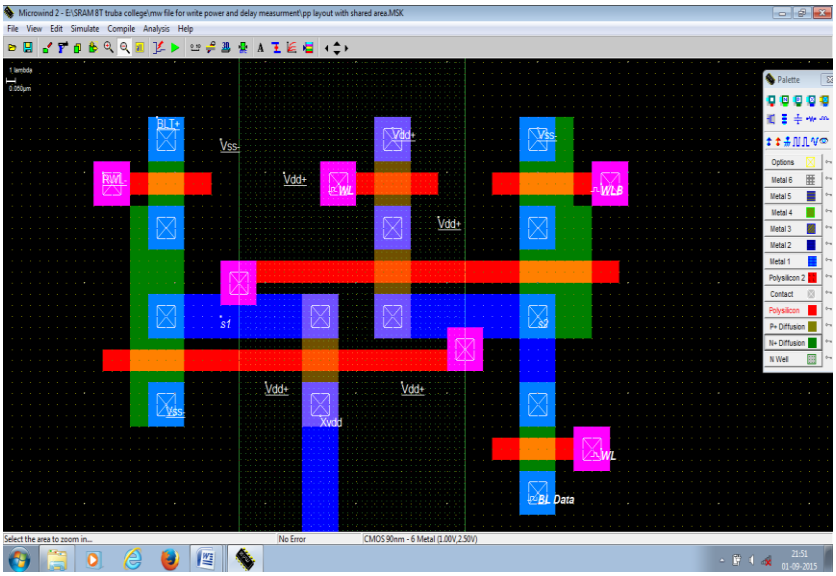

Fig.11 Layout of proposed cell

5. *Parameter Comparison*

Complete characterization on microwind performed at 90nm MOS technology. SRAM cells are compared on the basis of following parameter like Read Access Time(RAT), Write Access Time(WAT), Write Power and Layout Area as shown in table-1.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

Table-1: result analysis on microwind

SRAM Parameters	6T	9T	LP10T	WRE8T	Proposed
Write Power(µW)	1.84	1.96	1.773	0.755	0.496
Read Access Time(psec)	23.6	28.9	28.99	29.38	29.38
Write Access Time(psec)	257	181	164	514	14
Layout Area(μm^2)	3.42	5.13	5.13	5.31	5.31

Proposed work obtain 75% reduction in write power as compare to 6T and 65% reduction in write power as compare to WRE8T. Similarly write access time reduced up to 8% by the used of dual voltage logic. While other two parameters read access time and layout area remains same as WRE8T.

V. CONCLUSION & FUTURE SCOPE

Write access time, read access time and power dissipation are the major issues in high speed SRAM cells. In this paper, a novel low power 10T dual VDD CMOS based SRAM has been proposed, which dissipates less write dynamic power during write operation due to stack transistor M9 and M10, Which is dynamically controlled by WL/WLB. Low static power and low dynamic power obtained by proposed design using two supply VDDH and VDDL. VDDL provide the supply to inverter during standby mode, while VDDH provide the supply to inverter during read/write mode. The simulation shows that the proposed SRAM cell dissipates lesser dynamic power during write; has better write access time; dissipates lesser current leakage during the mode transitions than the other existing SRAM cells. This cell occupies similar area like WRE8Tbut shows better performance in term of write access time and writes power. This proposed 10T SRAM cell can be used to provide low power solution in high speed devices like laptops, mobile phones, programmable logic devices, etc.

REFERENCES

[1] Borkar S. Design challenges of technology scaling. IEEE Micro 1999;19(4):23.
[2] Brews J. High speed semiconductor devices. New York: Wiley; 1990. pp. 139–210.
[3] Roy K, Prasad SC. Low power CMOS VLSI circuit design. New York: Wiley Interscience Publications; 2000. p. 27–29.
[4] Taur Y, Ning TH. Fundamentals of modern VLSI devices. New York: Cambridge University; 1998. pp. 285–286.
[5] Mostafa H, Anis M, Elmasry M. Adaptive body bias for reducing the impacts of NBTI and process variations on 6T SRAM cells. IEEE Trans Circ Syst – I 2011;58(12):2859–71.
[6] Kao J, Chandrakasan A, Antoniadis D. Transistor sizing issues and tool for multi threshold cmos technology. In: IEEE 34th design automation conference (DAC); 1997. p. 409–14.
[7] Kao J, Narenda S, Chandrakasan A. MTCMOS hierarchical sizing based on mutual exclusive discharge patterns. In: IEEE 35th design automation conference (DAC); 1998. p. 495–500.
[8] Kim TH, Liu J, Keane J, Kim CH. Circuit techniques for ultra-low power subthreshold SRAMs. In: IEEE international symposium on circuits and systems (ISCAS); 2008. p. 2574–77.
[9] Liu Z, Kursun V. Characterization of a novel nine-transistor SRAM cell. IEEE Trans Very Large Scale Integr (VLSI) Syst 2008;16:488–92. No. 4.
[10] Singh S, Arora N, Gupta N, Suthar M. Leakage reduction in differential l0T SRAM cell using gated VDD control technique. In: International conference on computing, electronics and electrical technologies; 2012. p. 610–4.
[11] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based subthreshold SRAM," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.
[12] Ghasem Pasandi and Sied Mehdi Fakhraie, "An 8T Low-Voltage and Low-Leakage Half-Selection Disturb-Free SRAM Using Bulk-CMOS and FinFETs," *IEEE TRANSACTIONS ON ELECTRON DEVICES*, VOL. 61, NO. 7,pp. 2357-2363, JULY 2014.
[13] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based subthreshold SRAM," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.
[14] H. Noguchi, S. Okumura, Y. Iguchi, H. Fujiwara, Y. Morita, K. Nii, H. Kawaguchi, and M. Yoshimoto, "Which is the best dual-port SRAM in 45-nm process technology?—8T, 10T single end, and 10T differential," in *Proc. IEEE ICICDT*, Jun. 2008, pp. 55–58.