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Novel Cascaded Multilevel Inverter with Reduced Number of Switches

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ABSTRACT: Nowadays multilevel inverters has been introduced as an alternative in high power and medium voltage applications. A multilevel inverter not only achieves high power ratings, but also improves the performance of the whole system in terms of harmonics, dv/dt stresses etc. Unfortunately, multilevel inverters has several disadvantages. One particular disadvantage is the need for a large number of power semiconductor switches as the number of levels increases, which makes the overall system to be more expensive and complex. This paper presents a new class of multilevel inverters, hybrid cascaded multilevel inverter to reduce the number of switches and other components. In this topology, each battery cell can be controlled to be connected into the circuit or to be bypassed by a half- bridge converter. All half bridges are cascaded to output a staircase shape dc voltage. Then, an H-bridge converter is used to change the direction of the dc bus voltages to obtain ac voltages. When we compare with the conventional multilevel inverter topologies, the proposed inverters can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases. We can further reduce the switch and battery count by making the new topology an asymmetrical one. Simulation and experimental results are included to verify the operating principles of the hybrid cascaded multilevel inverter.

KEYWORDS: Multilevel inverters; cascaded H bridge multilevel inverter; hybrid cascaded multilevel inverter.

I.INTRODUCTION

Multilevel power conversion has found wide acceptance in various applications for its capability of high-voltage and high-efficiency operation[1]. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. Compared with the traditional two-level voltage converter, the primary advantage of multilevel converters is better output voltage step with lower THD, which results in high power quality,lower switching frequency and lower switching losses[2].

The most common application of multilevel converters has been in traction, both in locomotives and track-side static converters , applications for power system converters for VAR compensation and stability enhancement , high-voltage motor drive , high-voltage dc transmission , etc. As a cost effective solution, multilevel inverter not only achieves high power ratings, but also enables the use of low power application in renewable energy sources such as photovoltaic, wind, and fuel cells which can be easily interfaced to a multilevel inverter system for a high power application.

Three well-known multilevel topologies are diode clamped multilevel inverter[3], flying capacitor multilevel inverter[4], and cascaded or H-bridge multilevel inverter[5]. The main advantages of cascaded multilevel inverter are

i. The regulation of the DC buses is simple.

ii. Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.

iii. Clamping diodes not required

iv. Flying capacitors are not required

Unfortunately, multilevel inverters do have some disadvantages. One particular disadvantage is the need for a large number of power semiconductor switches. As the number of voltage level increases THD(Total Harmonic Distortion) decreases, but the number of components increases and the system becomes more and more complex. Several complex topologies have arisen for greater number of voltage levels with reduced number of switches[6]-[9] .This paper presents a new multilevel inverter topology[10] to reduce the number of switches, clamping diodes, or

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capacitors. In the proposed topology, each battery cell can be controlled to be connected into the circuit or to be bypassed by a half-bridge converter. All half bridges are cascaded to output a staircase shape dc voltage. Then, an H-bridge converter is used to change the direction of the dc bus voltages to obtain ac voltages. The outputs of the converter are multilevel voltages with less harmonics and lower dv/dt , which is helpful to improve the performance of the motor drives. As the number of voltage levels m grows, the number of active switches increases according to 2(m - 1) for the cascaded H- bridge, diode-clamped, and flying-capacitor multilevel inverters. In addition, for each phase, the diode-clamped inverter requires (m -1) (m - 2) clamping diodes and (m-1) capacitors for dividing the dc voltage, and the flying-capacitor inverter needs (m -1)(m- 2)clamping capacitors. For a given 'm' number of voltage levels, the inverter hybrid cascaded multilevel inverter requires only m+3 active switches. When compared with the existing multilevel inverters, the new multilevel inverter can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases. Hybrid cascaded multilevel inverter with unequal voltage sources is being proposed which further reduces the number of switches and sources as the number of levels increases.

II. HYBRID CASCADED MULTI LEVEL INVERTER

In this paper a multilevel inverter topology, hybrid cascaded multilevel inverter topology to reduce the number of switches is introduced which is shown in the figure(1).

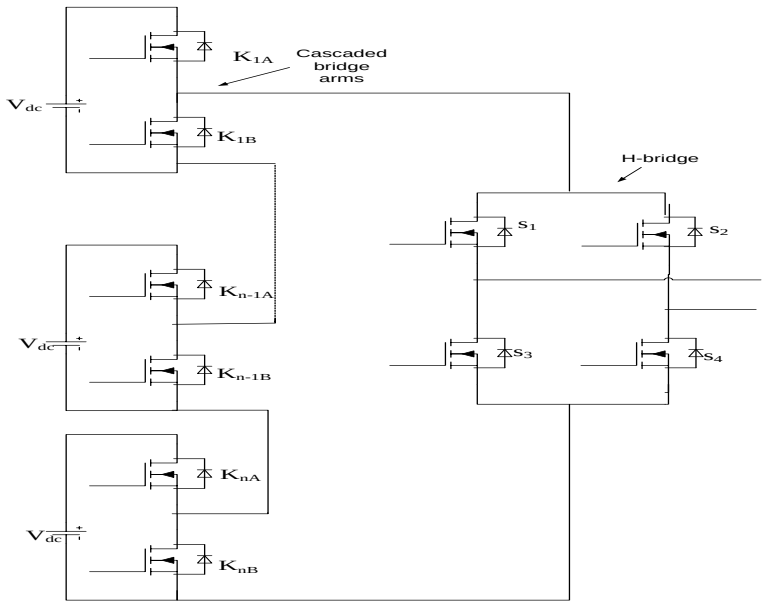

Fig 1: Hybrid cascaded multilevel inverter

This topology requires only m+3 switches for m levels where as for conventional inverters we require 2(m-1) switches. As shown in the figure this topology consists of two parts : cascaded bridge arms on the right and H bridge on the left. All half bridges are cascaded to output a staircase shape dc voltage. Each battery cell can be connected in to the circuit or bypassed from the circuit by controlling the switches in each half bridge. Thus a staircase shaped DC voltage is obtained at the output of cascaded bridge arm which is given to the H bridge. H bridge inverter is used to change the direction of DC voltage. For getting positive voltage switches S_1 and S_4 are to be turned ON and for getting negative voltage switches S_3 and S_2 are to be turned ON thus we can get multilevel AC voltage at the output. A seven level hybrid cascaded inverter is shown in the figure(2) .

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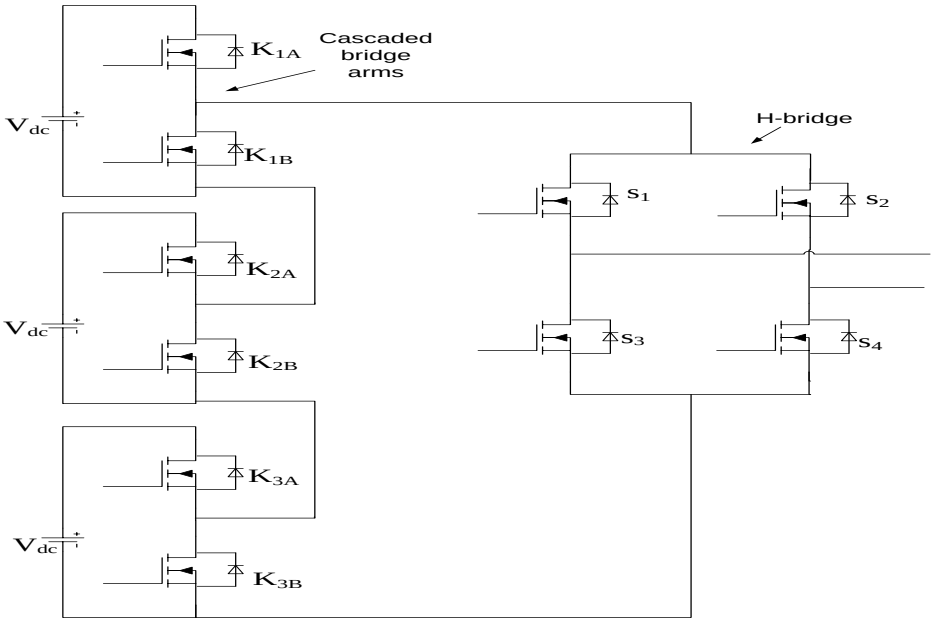

Fig 2 : Hybrid cascaded 7 level inverter

The seven level inverter of the above topology can be converted to a fifteen level inverter without any change in the circuit but to the sources, that is by using an asymmetrical topology . voltage sources of V_{dc} , 2 V_{dc} and 3 V_{dc} are used as shown in figure 3, and its switching scheme is shown in table 1. The proposed inverter requires just (m+8) switches, where m takes the values 0, 2, 4, 6, 8,.., for 7, 15, 31, 63,.., switching levels respectively.

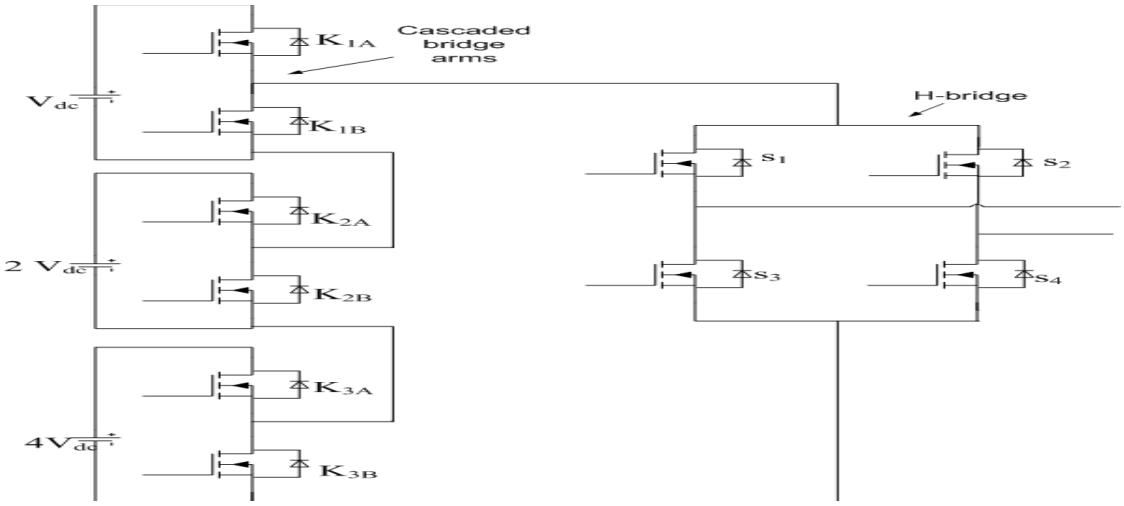

Fig 3: 15 level hybrid cascaded inverter with unequal voltage sources.

The modified topology requires only 10 switches and 3 sources required for a fifteen level inverter, whereas conventional cascaded inverter requires 28 switches and 7 sources , in case of hybrid cascaded inverter we require 18 switches and 7 sources. Thus from the above it is clear that by using this topology we can improve the power quality without sacrificing size of the hardware.

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K_{1A}	K_{1B}	K_{2A}	K_{2B}	K_{3A}	K_{3B}	S_1	S_2	S_3	S_4	Voltages
0	1	0	1	0	1	1	0	0	1	0
1	0	0	1	0	1	1	0	0	1	V_{dc}
0	1	1	0	0	1	1	0	0	1	$2 V_{dc}$
1	0	1	0	0	1	1	0	0	1	$3 V_{dc}$
0	1	0	1	1	0	1	0	0	1	$4 V_{dc}$
1	0	0	1	1	0	1	0	0	1	$5 V_{dc}$
0	1	1	0	1	0	1	0	0	1	$6 V_{dc}$
1	0	1	0	1	0	1	0	0	1	$7 V_{dc}$
1	0	0	1	0	1	0	1	1	0	$-V_{dc}$
0	1	1	0	0	1	0	1	1	0	$-2 V_{dc}$
1	0	1	0	0	1	0	1	1	0	$-3 V_{dc}$
0	1	0	1	1	0	0	1	1	0	$-4 V_{dc}$
1	0	0	1	1	0	0	1	1	0	$-5 V_{dc}$
0	1	1	0	1	0	0	1	1	0	$-6 V_{dc}$
1	0	1	0	1	0	0	1	1	0	$-7 V_{dc}$

Table 1: Switching scheme for 15 level inverter.

III. SIMULATION RESULTS

A 15 level asymmetrical hybrid cascaded multilevel inverter has been simulated using MATLAB. MATLAB SIMULINK model is shown in figure 4. Voltage source of 3V, 6V, 9V,12V is used for each cascaded bridge arm respectively. For generating gating signal for switches in cascaded bridge arms a sine wave of 50 Hz frequency is compared with constant values 1 to 7 and the generated signals are added up and the resultant signal is given as input to the program for producing switching signals. Voltage of cascaded bridge arms and output voltage is shown in the figure 5 & figure 6 . THD of 6.46 % is obtained and various harmonic components are shown in figure 7.

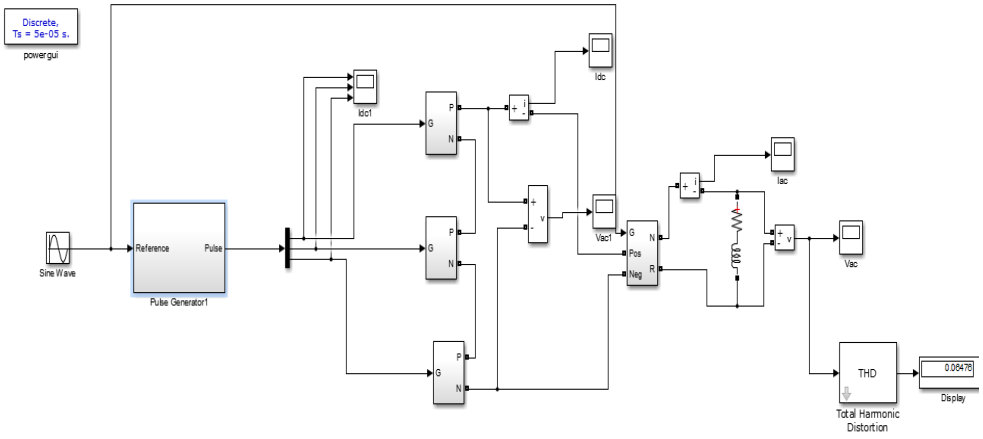

Fig 4: Simulink model of 15 level inverter

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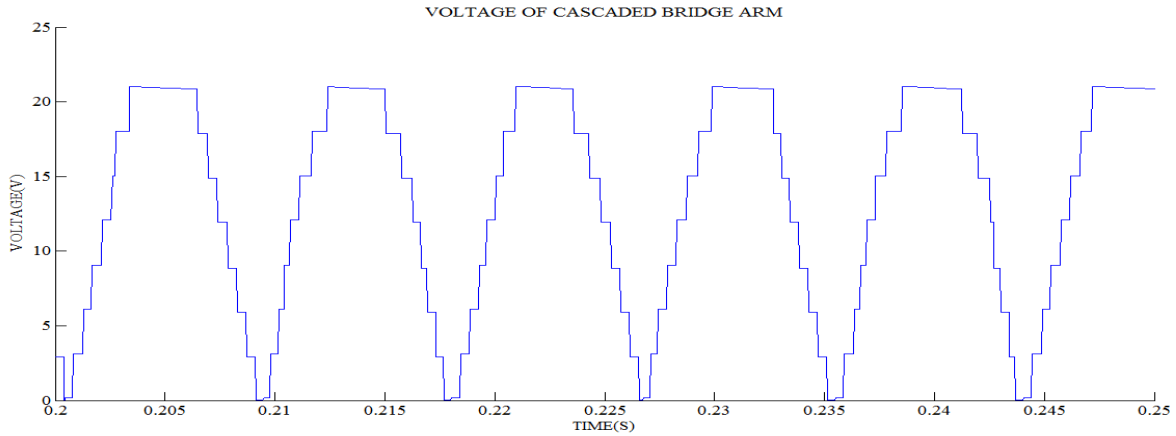

Fig 5: Voltage of cascaded bridge arm of 15 level inverter

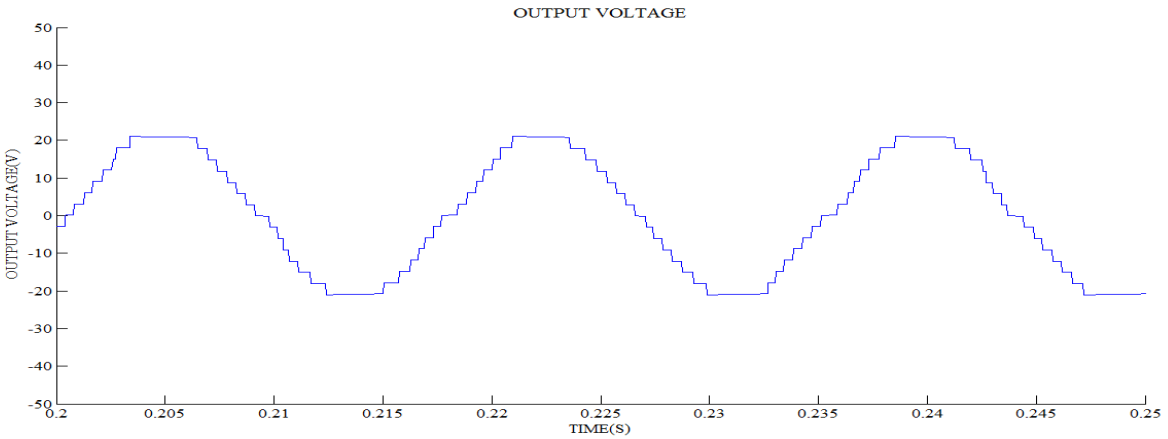

Fig 6: Output voltage of 15 level inverter

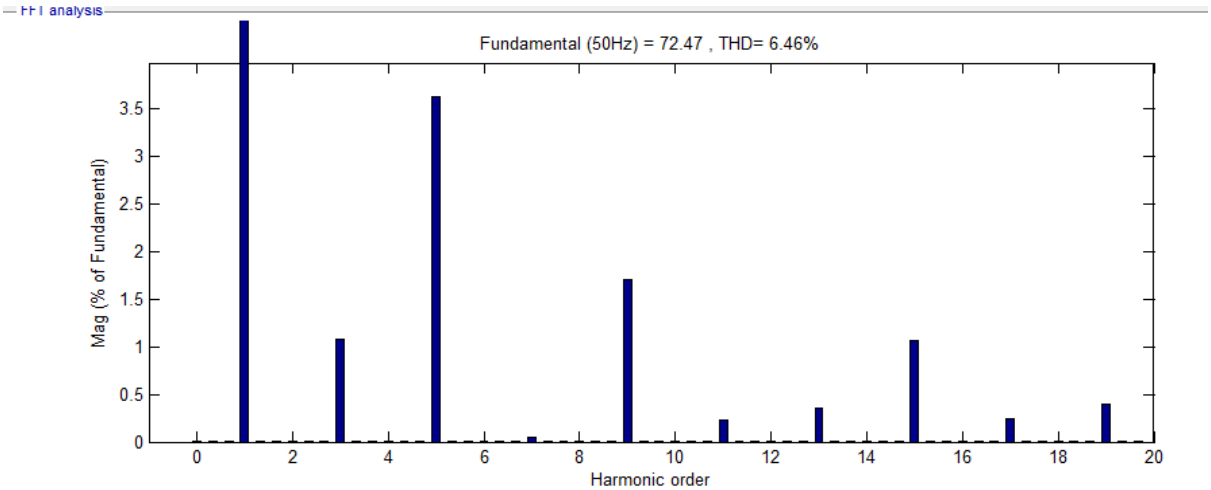

Fig 7: Plot of various harmonic components

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IV. EXPERIMENTAL RESULTS

Hardware prototype of fifteen level inverter has been developed in the laboratory with same specifications in the simulation environment which is shown in figure 8 . The circuit has three parts control circuit , drver circuit and power circuit. Control circuit is used for generating the gating signals and here PIC16F877A is used for generating the gating signals. Driver circuit is used for isolating the PIC circuit from higher voltage and boosting up the switching signals from PIC, here optocoupler 817 has been used for driver circuit. In power circuit IRFZ840 MOSFET has been used as the switch Here voltage sources of 3V, 6V, 12V has been used for each cascaded bridge arms. A fifteen level output has been obtained which is shown in the figure 9. A THD of 14.2% was obtained using harmonic analyzer(figure 9) which is higher than that obtained in simulation due to hardware limitations.

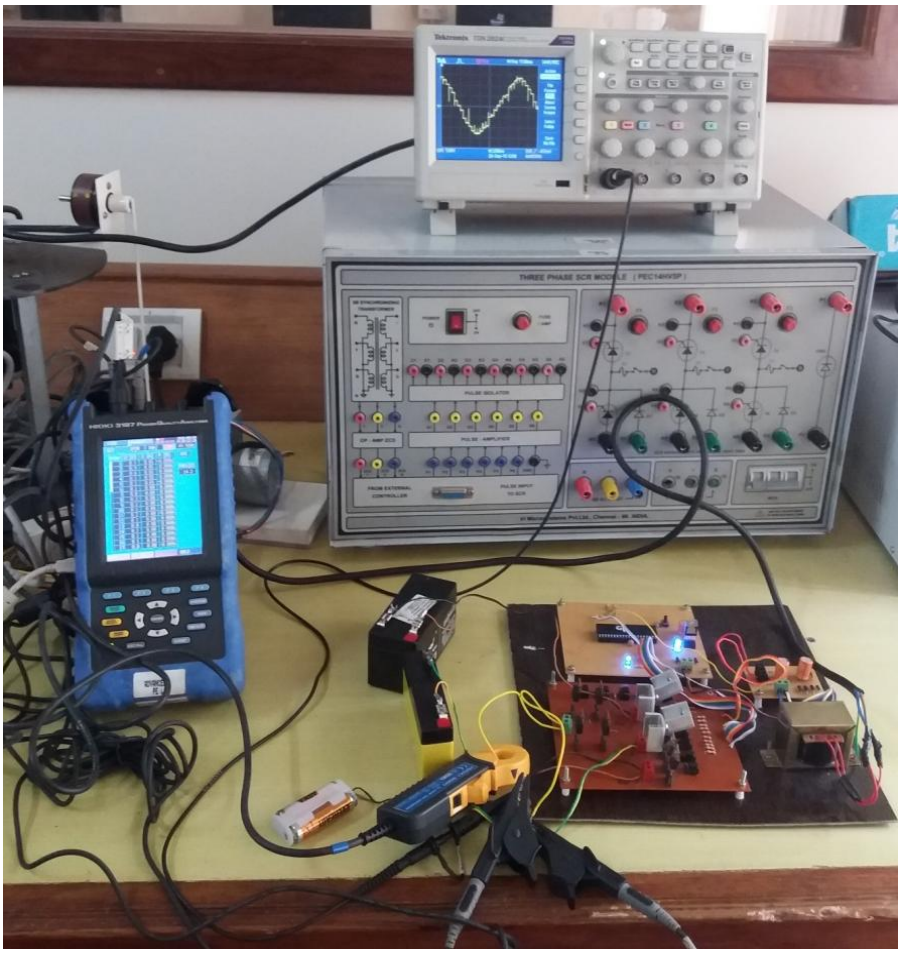

Fig 8: Prototype of fifteen level inverter

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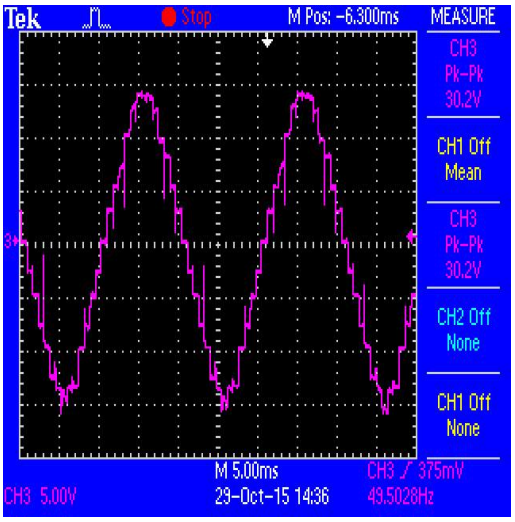

Fig 9 : Output waveform of fifteen level inverter

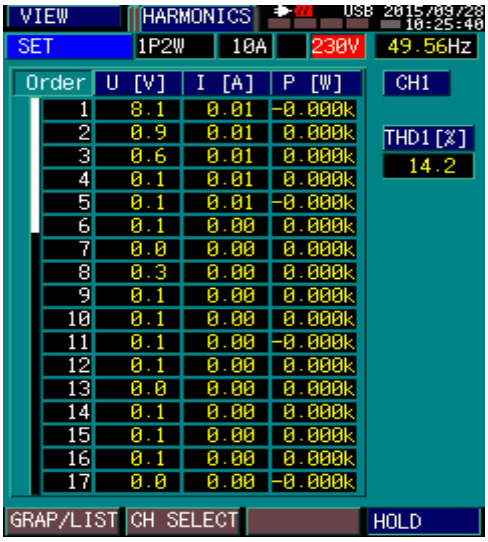

Fig 10 : Measurement of THD using harmonic analyzer

V.CONCLUSION

From the data and facts analysed above, we can see that the main disadvantage of multilevel inverter is the increase in number of switches with increase in number of levels. This paper presents asymmetrical multilevel inverter which requires only very less number of switches with the increase in number of levels. A fifteen level asymmetrical hybrid cascaded multilevel inverter has been simulated using MATLAB Simulink. The hardware prototype is implemented using PIC. A fifteen level inverter with unequal voltage sources is successfully fabricated and tested The proposed inverter requires just (m+8) switches, where m takes the values 0, 2, 4, 6, 8,.., for 7, 15, 31, 63,.., switching levels respectively. 15 level inverter of the proposed topology requires only 10 switches and 3 sources where as for conventional inverter we require 28 switches and 7 sources. Thus we can reduce the size of the hardware without sacrificing the power quality.

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