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Design of an Adiabatic FinFET Circuit Operating In Medium Strong Inversion Region

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ABSTRACT*:* Scaling of device technology, the leakage power has become the main part of power consumption, which seriously reduces the energy recovery efficiency of adiabatic logic.CMOS devices are shrinking to nanometer regime, increasing the consequences in short channel effects and variations in the process parameters which lead to cause the reliability of the circuit as well as performance. To solve these issues of CMOS, CMOS (Complementary metal oxide semiconductor) FinFET (Fin-type Field-Effect Transistors) is one of the promising and better technologies without sacrificing reliability and performance for its applications and the circuit design. To minimize short channel effects, FinFET is used. Lowering supply voltage of FinFET circuits is an effective way to achieve low power dissipations. The super-threshold adiabatic FinFET circuits based on PAL-2N operating on medium strong inversion regions are addressed in terms of energy consumption and operating frequency. In this paper, we use 32nm predictive Technology model. The super-threshold adiabatic FinFET logic circuits can attain low energy consumption with favorable performance, since FinFET devices can provide better drive strength than bulk CMOS ones.

KEYWORDS*:* Adiabatic computing, FinFET circuits, integrated circuits, super-threshold logic, low-power electronics

I.INTRODUCTION

In modern CMOS ICs, technology scaling increases the density and performance of a single chip, resulting in large energy consumptions [1, 2]. The total energy consumptions in a CMOS circuit mostly include two parts: static energy dissipation caused by leakage currents of MOS devices, dynamic energy dissipations caused by charging and discharging nodes of circuits. The major cause of leakage power is threshold voltage variations and device geometry. Supply voltage scaling has improved the energy per operation as dynamic power is approximately proportional to square of supply voltage. Higher operating frequencies and higher transistor densities trigger Dynamic power consumption. Whereas reduced gate length, oxide thickness and threshold voltage cause an exponential rise in leakage power consumption. In near future power consumption due to leakage will domain over dynamic power consumption. With the continuing scaling of CMOS processes, leakage energy dissipations are becoming the main source of energy consumptions. In order to cope with this problem, several novel devices have been developed. FinFET (Fin-type Field-Effect Transistors) devices show excellent performance.

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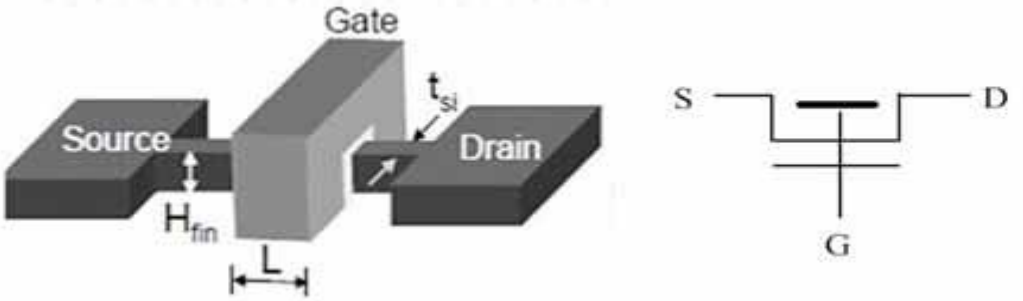

Fig. 1 shows Structure and symbol of FinFET.

FinFET has a three-dimensional structure. It consists of a thin silicon body, which is formed perpendicularly to the plane of the wafer. The current flows parallelly to the wafer plane. The channel is wrapped by the gate electrodes in three directions. FinFET can provide stronger control over the channel and suppress the SCEs, threshold current and gate-dielectric leakage current more effectively than MOSFET, resulting in higher on-state current, lower leakage and faster switching speed.

II. LEAKAGE CURRENT COMPONENTS AND THEIR IMPACT IN THE LOGIC CIRCUIT

In nanometer-scaled devices, the major leakage components are: 1) subthreshold leakage; 2) gate-oxide tunnelling leakage; and 3) reverse-bias drain-substrate and source-substrate junction BTBT leakage. There are other
Leakage components, like gate-induced-drain-leakage (GIDL), punch through current, etc., but those are not very serious at normal mode of operations. The aggressive scaling of oxide thickness results in a high direct tunnelling current through the gate insulator of the transistor. On the other hand, scaled devices require the use of the higher substrate doping density and the application of the "halo" profiles (implant of the high doping region near the source and drain junctions of the channel) to reduce the depletion region width of the source-substrate and drain-substrate junctions. A lower depletion-region width helps to control the SCE. The high-doping density near the source-substrate and drain-substrate junctions cause significantly large BTBT current through these junctions under high reversed bias. The basic physical mechanisms governing the different leakage-current components have different temperature dependence. Subthreshold current is governed by the carrier diffusion that increases with an increase of temperature. Since tunnelling probability of an electron through a potential barrier does not depend directly on temperature, the gate and the junction BTBT is expected to be less sensitive to temperature variations.

III. ADIABATIC FINFET LOGIC CIRCUITS BASED ON PAL-2N

The FinFET PAL-2N (Pass transistor adiabatic logic) buffer/inverter is shown in Fig. (2) [4]. It is composed of three main parts: the evaluation circuit consists of N-type FinFET transistors trees (N3 and N4) implementing logic function. The load driven circuit consists of a pair of P-type FinFET transistors (P1 and P2) for recovering energy into power clock. The clamp FinFET transistors (N1 and N2) providing a well-defined output logic '0'. The power-clock supply clk is a trapezoidal or sinusoidal waveform. It has the four phases: evaluation when the power clock clk is ramping up, hold when clk is keeping stable high, recovery when clk is ramping down, and wait when the power clock clk is keeping stable low for symmetry waveforms.

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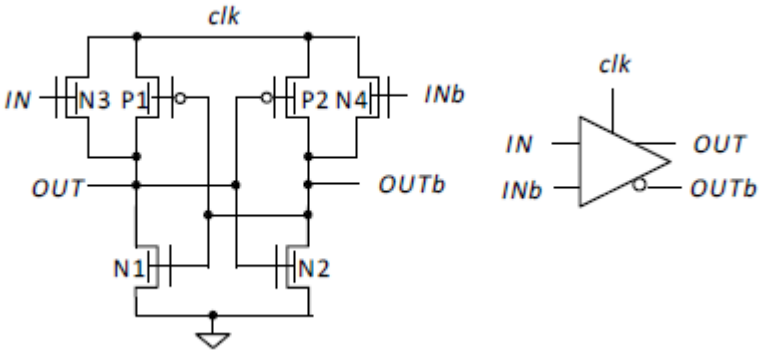

Fig. 2 shows FinFET buffer/inverter based on PAL-2N: schematic, symbol.

D flip-flop is considered to be the most essential memory cell in the vast majority of digital circuits, which brings it extensive utilization, especially under current circumstances where high-density pipeline technology is frequently employed in digital integrated circuits and massive flip-flop modules are indispensable components [5]. As a continuous research focus, numerous different types of 0 flip-flops have been invented and investigated [6] [7] [8], and the recent research trend has turned to high-speed low-power performance, which can be boiled down to low power-delay product. To implement high performance VLSI, choosing the most appropriate D flip-flop has obviously become an extremely significant part in the design flow. The reasons come from two aspects: one is that 0 flip-flop has direct effect on the clock frequency of digital circuit systems, especially for some micro-structures with shallow logical depth.

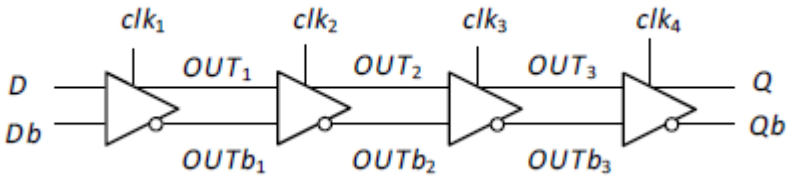

Fig. 3 shows FinFET PAL-2N logic *D* flip-flop.

IV.SIMULATIONS OF SUPER-THRESHOLD ADIABATIC FINFET PAL 2N LOGIC D FLIP FLOP

In order to investigate the performances of the PAN-2N circuits based on FinFET in sub-threshold, near-threshold, and super-threshold regions, the PAL-2N FinFET D flip flop are simulated with different peak-to-peak voltages of the power clocks ranging from 0.2V to 1.0V with 0.1V step using the 32nm FinFET PTM technology.

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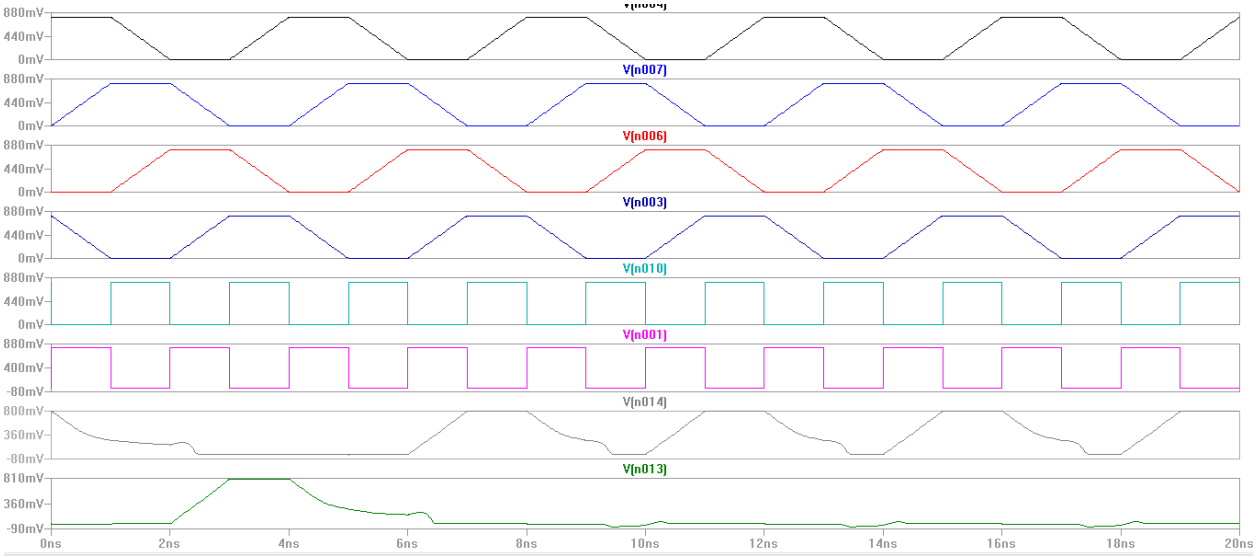

Fig. 4 shows CMOS PAL-2N logic *D* flip-flop.

The supply voltage of near-threshold CMOS circuits is slightly above the threshold voltage of the MOS transistors [9]. The near-threshold CMOS circuits can retain much of the energy savings of sub-threshold circuits[9, 10]. Compared with sub-threshold circuits, the near threshold CMOS circuits can obtain good performance due to large turn-on currents. However, the near-threshold CMOS circuits are only suitable for mid-speed applications, since their MOS devices operate on medium weak inversion.

The super-threshold adiabatic FinFET circuits based on PAL-2N operating on medium strong inversion regions are addressed in terms of energy consumption and operating frequency. The supply voltage of the super-threshold circuits is much larger than the threshold voltage of the transistors, but it is lower than the normal standard supply voltage For further verification and demonstration, in this section the performance on power dissipation and working speed of the modified D flip-flops has been investigated by comprehensive simulations.

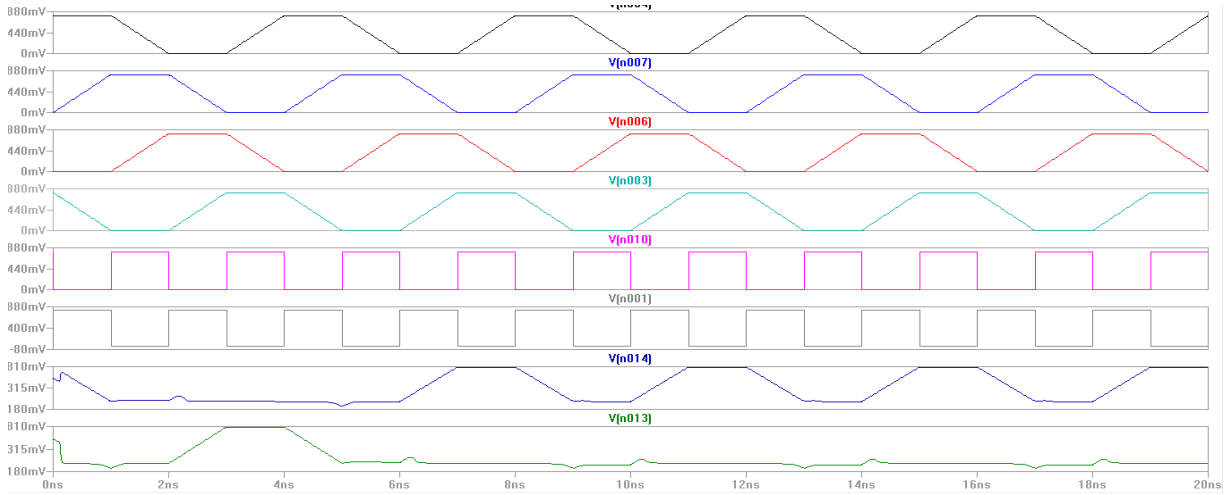

Fig. 5 shows FinFET PAL-2N logic *D* flip-flop.

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TABLE I: COMPARISON OF CMOS and FinFET based PAL-2N Flip-Flop

Device	PAL-2N Flip-Flop				Total power
	stage 1	stage2	stage3	stage4	
CMOS	9.63084µW	2.1112µW	34.7032µW	10.4414µW	56.8864 µW
FinFET	550.968nW	975.252nW	1.78329µW	75.6631nW	3.351731µW

From the study its found that the FinFET based PAL-2N circuit provides lesser power compared to conventional circuit. In future the work will be extended to implement a circuit based on FinFET PAL-2N logic.

V.CONCLUSION

Lowering supply voltage of FinFET circuits is an effective way to achieve low power dissipations. The super threshold adiabatic FinFET circuits based on PAL-2N operating on medium strong inversion regions have been addressed in terms of energy consumption and operating frequencies. The performance of FinFET PAL 2N D Flip flop has also been investigated with different source voltages ranging from 0.2V to 1.0V. From the study its found that the FinFET based PAL-2N circuit provides lesser power compared to conventional circuit.

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