ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

Design of a Low Power Adiabatic Logic Circuit Based on FinFET

P.Deepa, S.Priyanka, V.M.Senthil Kumar

PG Student [VLSI], Dept. of ECE, Vivekanandha College of Engg for Women, Tiruchengode, Tamilnadu, India

PG Student [VLSI], Dept. of ECE, Vivekanandha College of Engg for Women, Tiruchengode, Tamilnadu, India

Associate professor, Dept. of ECE, Vivekanandha College of Engg for Women, Tiruchengode, Tamilnadu, India

ABSTRACT*:* The rapid development of transistor technology has resulted in higher performance and integration density. Simultaneously, the continuous increasing power has become the primary barrier against further development of VLSI (Very large scale integration) circuit design. Over the past decade, research work concerning energy efficiency of computing systems has increased. From big data centers with many servers to small battery operated mobile devices power dissipation is becoming a major concern. For digital IC's design many low power design techniques have been proposed from time to time one of them which is suitable for ultralow power applications and is thus gaining attention is adiabatic logic. A number of different adiabatic logic styles have been proposed.Adiabatic logic style is an attractive solution for low power digital design. A novel low-power adiabatic logic based on FinFETs (Fin-type Field-Effect Transistors) devices has been proposed. Due to the lower leakage current, higher on-state current and design flexibility of FinFETs, The proposed adiabatic logic shows considerable power reduction, performance improvement and area saving compared with CMOS (Complementary metal oxide semiconductor) adiabatic logic. In this proposed work, we use 32nm predictive Technology model. And also analyzing the power dissipation of different adiabatic logic based on CMOS and FinFETs

KEYWORDS*:* leakage power, FinFET, adiabatic logic, power reduction.

I.INTRODUCTION

Scaling down size of MOS transistors has resulted in dramatic increase of leakage currents. To decrease leakage power dissipations is becoming more and more important in low-power nanometer circuits. Power consumption is composed of two parts: dynamic power and static power. The dynamic power is due to the switching activities during charging and discharging process, while static power is caused by the inherent device leakage when the circuit is in the off state [1]. Therefore, both dynamic power and static power need to be investigated in the low-power VLSI circuit design. The leakage dissipation catches up with the dynamic power consumption gradually, and it is becoming an important factor in low-power design for deep sub-micron. In early period, the power consumption was once dominated by the dynamic power. A lot of novel circuit technologies like adiabatic circuit [2], sub-threshold circuit [3] and multi-threshold technology [4] have been introduced to reduce dynamic power. Among these, adiabatic logic, a novel low-power circuit structure, utilizes AC voltage supply rather than DC voltage supply to recycle the energy of circuits.

Adiabatic circuits are low power circuitry which use "reversible logic" to conserve energy. The word adiabatic comes from a Greek word that describes thermodynamic processes which exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. Adiabatic circuits employ AC power source (clock) rather than the DC supply, and therefore can recover the energy stored in capacitance back to the power source, and completely avoid the dynamic power dissipation theoretically. In adiabatic logic, the node voltage changes synchronously with the supply voltage (sine wave); thus the energy released from the power supply is just 0.5 CV^2DD, which could be stored in the load capacitance. Moreover, when the supply voltage falls down to the ground level, the energy stored in the capacitance could flow back to the power supply. Therefore in the field of low power design, adiabatic logic is a good selection in the circuit

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level. We extract charge from the supply at the lowest feasible voltage, and return it at the highest feasible voltage. Therefore in the field of low powerdesign, adiabatic logic is a good selection in the circuit level.

II. CMOS ADIABATIC LOGIC

A.CMOS 2N2N2P INVERTER

The adiabatic circuit operation consists of four phases, namely Wait, Evaluate, Hold and Recover. The phase difference between adjacent phases is a quarter of period. The simplest adiabatic buffer with 2N2P structure, which contains two cross-coupled P-MOSFETs and two differentials input N-MOSFETs, is taken as an example to explain the four-phase operation mode [5]. The N-MOSFETs block is the evaluation logic and the P-MOSFETs are the charging and discharging current access of the adiabatic logic. The four-phase operations are shown as follows: They are

1) Wait: The power supply stays zero, the inputs become valid and the evaluation logic generates pre-evaluated result and the outputs keep low voltage.

2) Evaluate: The power supply rises from zero to *V*DD gradually, and inputs remain stable. According to the result of pre-evaluation, output follows the power supply to become valid.

3) Hold: The power supply stays high to keep the output valid, providing the constant input signal for the next stage in the adiabatic pipeline Besides the inputs return to zero.

4) Recover: The power supply climbs down to zero. The remaining zero voltage inputs shut down the current access to the ground; thus the charge stored in the node capacitance can flow back to the power supply through the cross-coupled P-MOSFETs.

B.CMOS IPAL INVERTER

In the 2N2N2P logic, the two more N-MOSFETs with P-MOSFETs make up two inverters to cross-couple, which increases the stability of the outputs. The IPAL (improved pass-transistor adiabatic logic) [6] logic folds the evaluation logic upward to the pull-up blocks to form two charging paths with a pair of cross-coupled P-MOSFTEs, which reduces the time taken to evaluate the outputs.

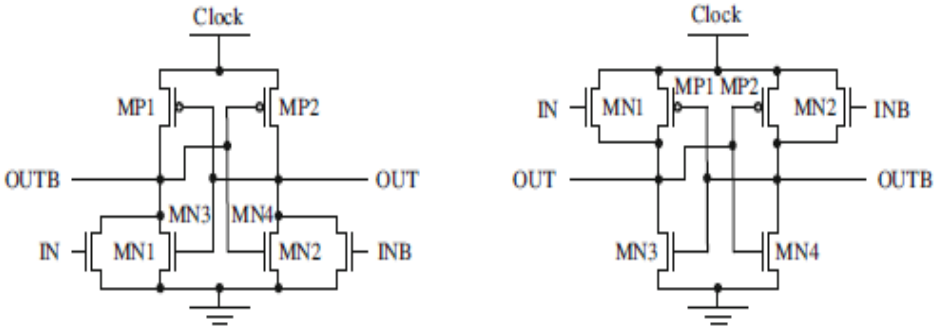

Fig. 1. CMOS Adiabatic logic (a) 2N2N2P (b) IPAL

III. FINFET ADIABATIC LOGIC

A.FINFET 2N2N2P INVERTER

FinFET has a three-dimensional structure. It consists of a thin silicon body, which is formed perpendicularly to the plane of the wafer. The current flows parallelly to the wafer plane. The channel is wrapped by the gate electrodes in three directions. FinFET can provide stronger control over the channel and suppress the SCEs, (Short-Channel Effects) threshold current and gate-dielectric leakage current more effectively than MOSFET, resulting in higher on-state current, lower

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leakage and faster switching speed. The PTM [7] is chosen as the model for the simulation due to the following reasons: PTM covers sufficient physical effects, and excellent scalability of PTM across process and design conditions have been shown in the published results.

B.FINFET IPAL INVERTER

Besides, the multi-gate structure provides more design flexibilities. It is worth noting that the frontgate and the back-gate of FinFET could be tied together or be controlled independently by different voltages, which provides three basic working modes for FinFET, namely Short-Gate mode, Independent-Gate mode and Low-Power mode.

1) Short-Gate (SG) mode, where the double gates are tied together, acting as a three-terminal device. The SG FinFET is a promising replacement for MOSFET. Higher on-state current and faster switch speed make it a high performance mode. And strong gate control offers better suppression for the SCEs and gate-dielectric leakage.

2) Independent-Gate (IG) mode, where the top part of the gate is removed to form two independent gates, acting as a four-terminal device. The front-gate and the back-gate can be connected to different inputs, and thus the IG FinFET can work as two parallel transistors, thus greatly reducing the number of transistors and improving the design flexibility.

3) Low-Power (LP) mode, where the back-gate is connected to a reverse-bias to reduce the threshold leakage. Actually it is a special case of IG mode. In this mode, the threshold leakage can be reduced by adjusting the back-gate voltage

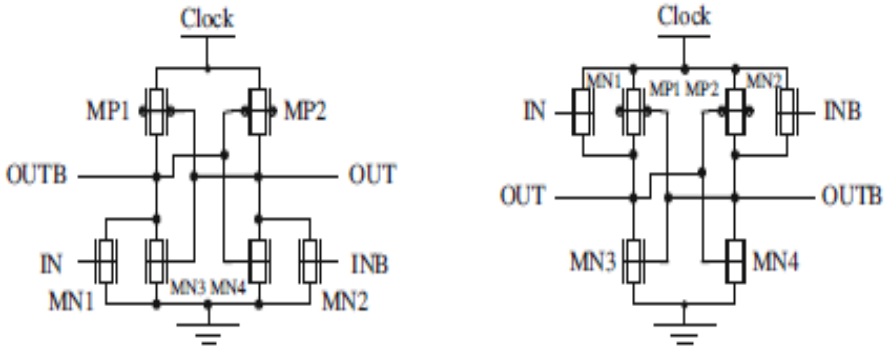

Fig. 1. FINFET Adiabatic logic based on SG mode (a) 2N2N2P (b) IPAL

IV. RESULT AND DISCUSSION

In the fig 3(a), it shows the graph of voltage v_s time for CMOS Adiabatic logic using improved pass transistor logic in the VLSI development technology

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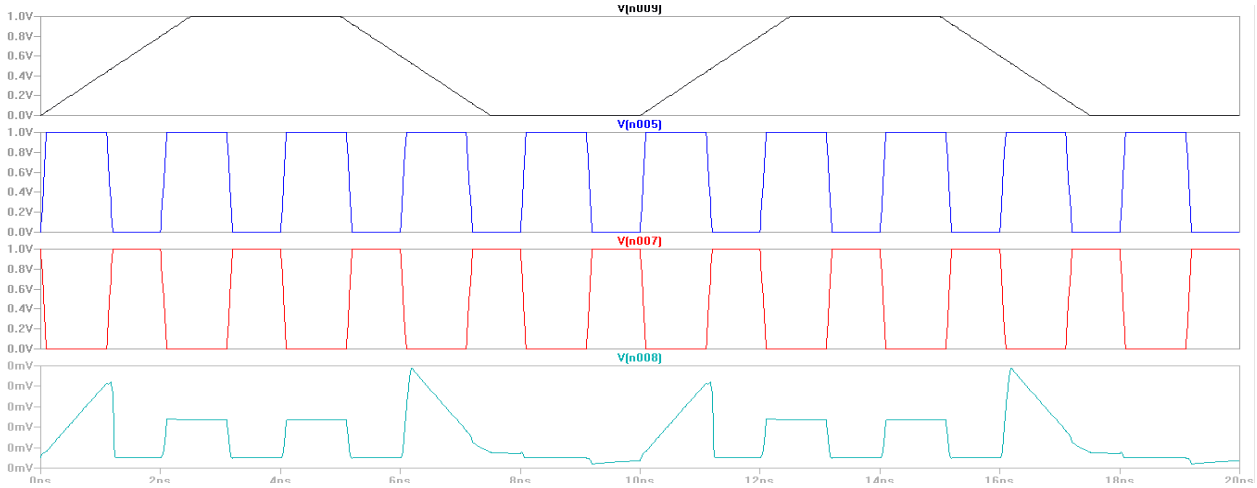

Fig. 3(a). CMOS IPAL LOGIC

In the fig 3(b), it shows the graph of voltage v_s time for FINFET Adiabatic logic based on SG mode using improved pass transistor logic in the VLSI development technology

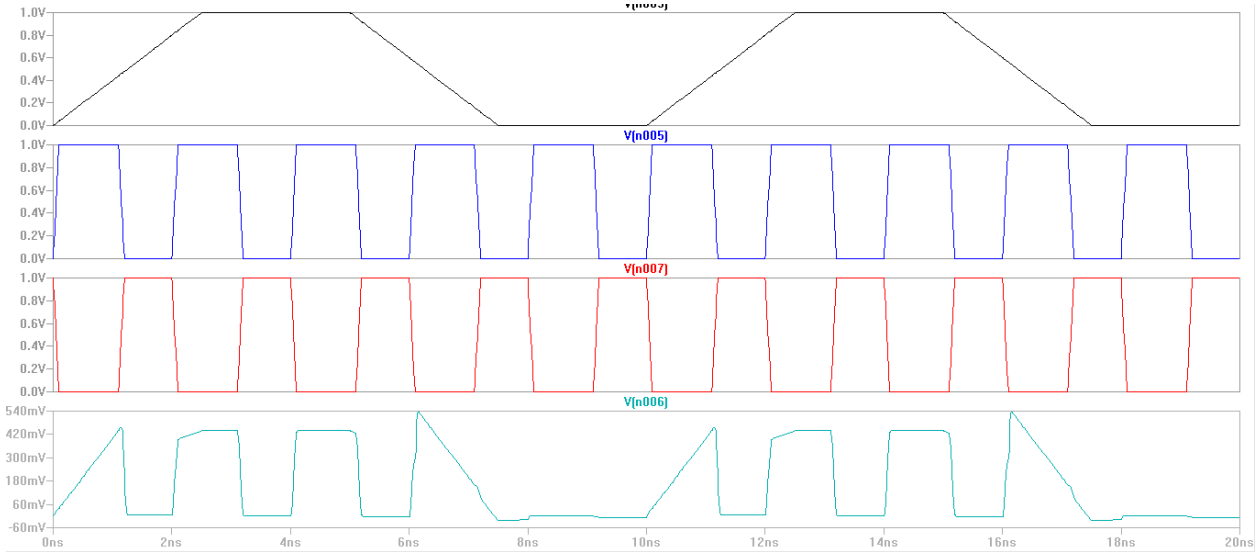

Fig. 3(b). FINFET IPAL LOGIC Based on SG mode

From the results obtained its clear that the FinFET based adiabatic logic is better than the conventional circuit.In future on application circuit will be implemented using the logic.

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TABLE I: Power comparison for CMOS and FinFET based inverter using Adiabatic logic

Vdd-1V

Device	Power calculation							
	PI 1Mhz		PI 100Mhz		PI 500Mhz		PI 1Ghz	
	2n2n2p	ipal	2n2n2p	ipal	2n2n2p	ipal	2n2n2p	ipal
CMOS	879.458nW	417.3nW	879.042nW	874.688nW	2.13493µW	2.0998µW	2.32308µW	1.38114µW
FinFET SG mode	10.4733nW	8.15694nW	10.4498nW	9.79779nW	11.3222nW	1.99452nW	59.6083nW	18.8738nW

V.CONCLUSION

In this paper presents the novel adiabatic logic based on FinFETs. Two types of adiabatic logic, namely 2N2N2P, IPAL are rebuilt by SG mode FinFET. Compared with the CMOS adiabatic logic, the proposed logic effectively reduces the power consumption and improves the performance. And the improvement of power reduction becomes more significant as the frequency increases. Moreover, due to the higher on-state current and faster switching speed, the implementing of FinFET further improves the limiting frequency of adiabatic circuit. Therefore, the low-power and high-performance FinFET adiabatic logic will be a competing structure in the future IC design.

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