



# **High Performance ADDLL using DDFF Based Frequency Divider and Counter**

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**ABSTRACT:** In many areas, the Delay-Locked Loop (DLL) can be an alternative to the traditional frequency generation technique - the Phase-Locked Loop (PLL). The DLL is preferred because of its better stability, smaller jitter accumulation, and shorter locking time, as compared to the PLL. Since using the high performance DDFF in the design of counter, frequency divider, and phase detector, can achieve high performance DLL with minimum power consumption. The performance will be analysed with the ADDLL based on conventional flip-flop and XCFF. This project presents the design and implementation of high performance ADDLL using DDFF based frequency divider and counter with minimum power delay product . In this project, design of frequency multiplier using DDFF based ADDLL which multiplies the frequency of output wave by factors of 8 is done .The circuit is implemented in 180nm technology using cadence virtuoso software.

**KEYWORDS:** Flip\_Flop, DDFF, ADDLL.

## **I.INTRODUCTION**

In many areas, the Delay-Locked Loop (DLL) can be an alternative to the traditional frequency generation technique - the Phase-Locked Loop (PLL). In ADDLL it is possible to stop any toggling, thus no dynamic power is consumed. The area of ADDLL is typically much lower than that of analog DLLs. The main reason is the large filtering capacitors used in analog DLLs/PLLs. Typical ADDLLs require few thousands gates, and their area is scaled at each technology generation .

Technology and speed are always moving forward, from low scale integration to large and VLSI and from megahertz (MHz) to gigahertz (GHz). The system requirements are also rising up with this continuous advancing process of technology and speed of operation.The proposed DDFF eliminates the redundant power dissipation present in the XCFF. Hybrid latch flip-flop (HLFF) and semi dynamic flip-flop (SDFF) are considered as the classic high-performance flip-flops. They possess a hybrid architecture that combines the merits of dynamic and static structures. In addition, SDFF has a distinctive capability of incorporating logic very efficiently, because unlike the true single phase latch (TSPC) ,only one transistor is driven by the data input. This greatly helps in reducing the pipeline overhead since the delay and area associated with one or more logic stages preceding the flip-flop can be eliminated. Several hybrid flip-flop designs have been proposed in the past decade, all aiming at reduction of power, delay.

A recent paper introduced a flip-flop architecture named cross charge control flip-flop (XCFF), which has considerable advantages over SDFF and HLFF in both power and speed. It uses a split-dynamic node to reduce the precharge capacitance, which is one of the most important reasons for the large power consumption in most of the conventional designs. But this structure still has some drawbacks, due to redundant power dissipation that results when the data does not switch for more than one clock (CLK) cycles. Also, the large hold-time requirement makes the design of timing-critical systems with XCFF an involved process. Finally, despite having a single data-driven transistor, embedding logic to XCFF is not very efficient due to the susceptibility to charge sharing at the internal dynamic nodes.

DDFF consists of 1 pseudo-dynamic and 1 dynamic split nodes which separately drives the output pull up and pull down transistors. A comparison of the DDFF flip-flop with the conventional flip-flops showed that it exhibits lower power dissipation along with comparable speed performances, and it is capable of efficiently incorporating complex logic in to the flip-flop. A comparison of the DDFF flip-flop based ADDLL with the conventional flip-flop based

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ADDLL showed that it exhibits lower power dissipation along with comparable speed performances. So when using the low power and delay flip flop the entire power consumption of the circuit can be reduced. Since the delay locked loop have a delay adjustment cell, but using the low delayed flip-flop based modules we can reduce the total delay of circuit without affecting the ADDL working.

This paper proposes a High performance ADDLL architecture has the phase detector subsystem and the up/down counter subsystem using the high performance DDFF. The implementations of the DLL can be categorized by its delay elements which can be continuously variable or analog, discretely ordered/continuous or analog-digital, or all-digital. Due to all digital components it consumes very low power. To incorporate the digital configuration the charge pump was replaced by a counter. The total system consists of a phase detector, an up/down counter, the delay line, clock divider, and the frequency multiplier. The frequency multiplying technique is performed by using an edge combiner based clock synthesis system. The ADDLL architecture has the phase detector subsystem generates an up/down signal based on the phase difference between reference clock and the delayed version of the clock from the Bit controlled Delay line block. The up/down counter subsystem counts either up or down based on the signal from the phase detector. The low frequency clock to the counter subsystem is generated by the clock divider subsystem. The clock divider subsystem generates a clock frequency of the output of the counter controls the load of the delay elements in the delay line.

## ILDFF ARCHITECTURE

Fig 1 shows the DDFF architecture. Node X1 is pseudo-dynamic, with a weak inverter acting as a keeper, whereas, compared to the XCFF, in the new architecture node X2 is purely dynamic. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF. The operation of the flip-flop can be divided into two phases: 1) the evaluation phase, when CLK is high, and 2) the precharge phase, when CLK is low. The actual latching occurs during the 1–1 overlap of CLK and CLKB during the evaluation phase. If D is high prior to this overlap period, node X1 is discharged through NM0-2. This switches the state of the cross coupled inverter pair INV1-2 causing node X1B to go high and output QB to discharge through. NM4. The low level at the node X1 is retained by the inverter pair INV1-2 for the rest of the evaluation phase where no latching occurs. Thus, node X2 is held high throughout the evaluation period by the pMOS transistor PM1. As the CLK falls low, the circuit enters the precharge phase and node X1 is pulled high through PM0, switching the state of INV1-2. During this period node X2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node QB and maintain their voltage levels through INV3-4. If D is zero prior to the overlap period, node X1 remains high and node X2 is pulled low through NM3 as the CLK goes high. Thus, node QB is charged high through PM2 and NM4 is held off. At the end of the evaluation phase, as the CLK falls low, node X1 remains high and X2 stores the charge dynamically. The architecture exhibits negative setup time since the short transparency period defined by the 1–1 overlap CLK of and CLKB allows the data to be sampled even after the rising edge of the CLK before CLKB falls low.

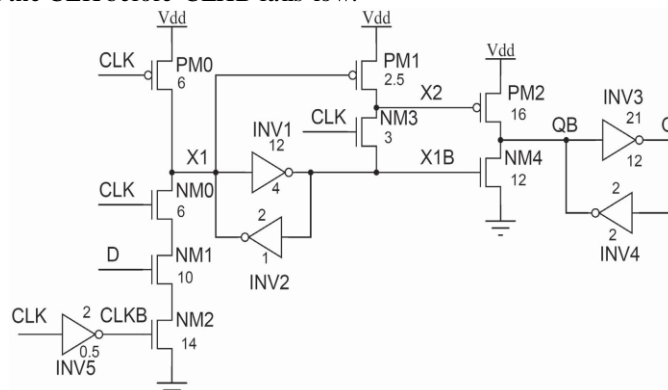


Fig. 1 DDFF used in the Up-down Counter.

Node X1 undergoes charge sharing when the CLK makes a low to high transition while D is held low. This result in a momentary fall in voltage at node X1, but the inverter pair INV1-2 is skewed properly such that it has a switching

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threshold well below the worst case voltage drop at node X1 due to charge sharing. The DDFF have low power, less charge sharing at internal node, low power delay product .so DDFF is used in the design of ADDLL.

### III.ADDLL ARCHITECTURE

Control part of the ADDLL consists of the phase discriminator, delay controlled delay line and counter .Outputs of the delay line and the reference signal are fed into the phase discriminator. When the phases of these two signals are mismatched, phase discriminator produces either an up signal or down signal, depending on the phase lag of the reference or delayed signal. Digital types of phase discriminators operate on the binary signals exclusively, and are usually combined with a m-bit binary UP/DOWN/HOLD counter that replaces the analog charge pump and the loop filter of the analog DLL. When the delay of the DE has to be increased/decreased (phase mismatch), the PD generates the UP/DOWN signal, which increments/decrements m bit counter. A frequency divider is a circuit that takes an input signal of a frequency  $f_{in}$  and generates an output signal of a frequency  $f_{out}$ , where  $f_{out} = f_{in}/n$  and ‘n’ is an integer. Digital dividers can work up to tens of GHz. They can be used for improving the performance of electronic counter measures equipment.

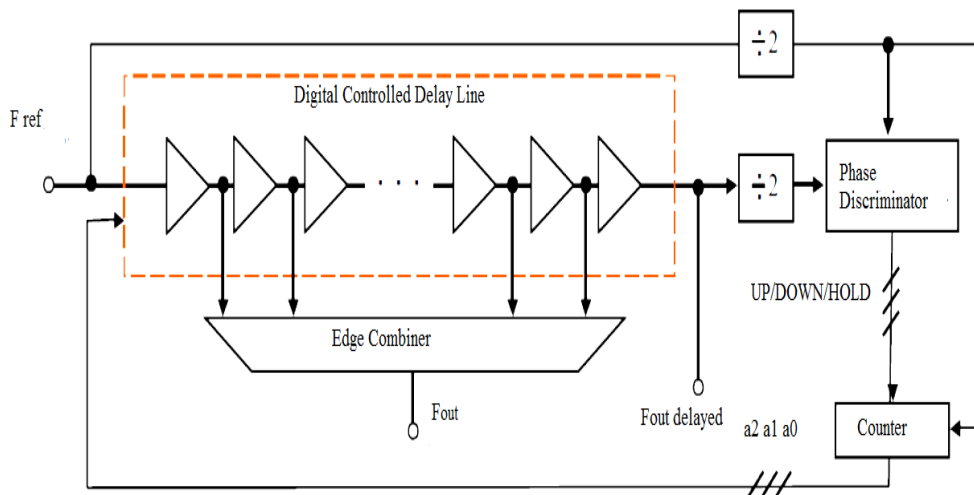


Fig. 2 All-digital DLL

Phase discriminators, shown in Fig.3 are digital circuits and they require square waves for both reference and output signals. The UP and DOWN signals are defined here as active-low signals. In the case of zero phase error, both UP and DOWN signals are permanently HIGH. If the signal  $f_{OUT}$  delayed lags the reference signal  $f_{REF}$ , the UP output generates pulses with a duty-cycle ratio proportional to the phase error. In the opposite case, DOWN output is pulsed.

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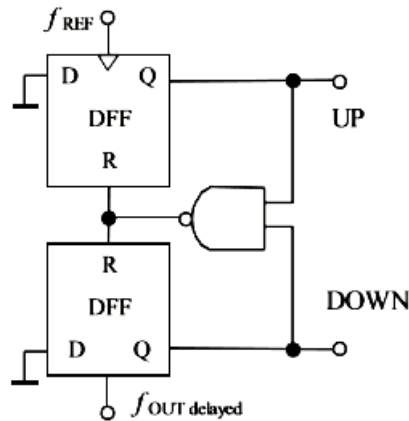


Fig. 3 Phase discriminator(PD)

The Digital-Controlled Delay Element (DCDE) is based on the MUX structure (Fig. 4 illustrates the case of  $m = 3$ ). According to the combination of them control bits  $[a_{m-1} \dots a_1, a_0]$  generated in the counter of the phase discriminator, multiplexers serially combine binary-weighted LCELL delays, resulting with the following delay increments .

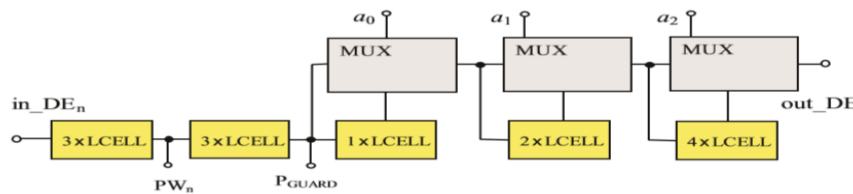


Fig. 4 Digital-Controlled Delay Element (DCDE) for  $m = 3$

The Digital Controlled Delay Line (DCDL) consists of  $n$  serially connected DCDE (Fig. 5 illustrates the case of  $n = 8$ ). So, the maximal multiplication factor can be equal to  $f_{OUTMAX} = n f_{REF}$ . The DCDL is the most important part of an ADDLL design, as it decides the operating frequency range, delay resolution and delay linearity of the ADDLL.

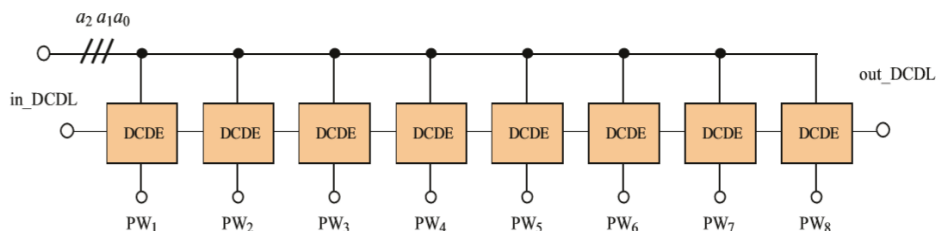


Fig. 5 Digital-Controlled Delay Line (DCDL) for  $n = 8$

The logical AND-OR operation of these signals  $(AB + BC + CA)$  results in a frequency multiplied output waveform .

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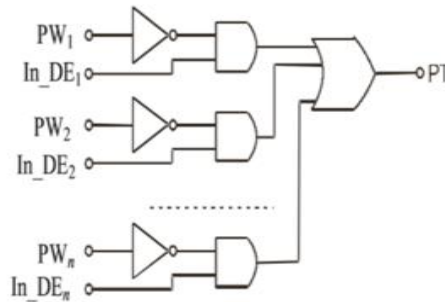


Fig. 6 Edge combiner (EC)

The ADDL using DDFF based frequency divider and counter performance is analyzed using cadence virtuoso software in 180 nm technology . the ADDL using DDFF is compared with the performance of ADDL using XCFE and conventional flip-flop ie NAND based D flip flop.

## V. RESULT AND DISCUSSION

Table 1 illustrates the speed and power delay product (PDP) of various flip-flops at 50% data activity. The results show that the Dual Dynamic flip-flop has the lowest PDP among the group and uses least number of devices .

Table 1 Performance Comparison of various flip-flops

Flip-flop	Number of transistors	Total power (mw)	Minimum D-Q(ps)	PDP(pj)
SDFE	23	25.138	80.98	2.03
HLEF	20	13.806	99.07	1.367
Power PC 603	22	22	104.1	2.29
XCFE	21	7.98	101.8	0.812
DDFF	18	7.7	94.25	0.725

The chart Fig. 7 shown below is the PDP analysis of flip-flop under study. The Dual Dynamic flip-flop has the lowest PDP among the group.

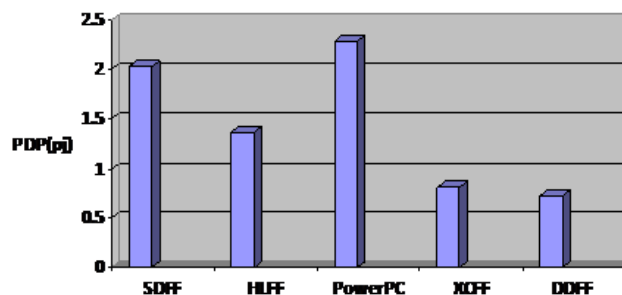


Fig.7 PDP of flip- flops under study



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Table. 2 illustrates the speed and power delay product (PDP) of ADDLL using different flip -flops at 50% data activity. The results show that the ADDLL using Dual Dynamic flip-flop has the lowest PDP among the group.

Table .2 Performance Comparison of various ADDLL

ADDLL	Total Power (mw)	Delay (ns)	PDP(pj)
ADDLL(Conventional)	25.35	0.9	22.8
ADDLL(XCFF)	15.8	1.35	21.33
ADDLL(DDFE)	13.1	1.104	14.46

The chart Fig. 8 shown below is the PDP analysis of ADDLL under study. The ADDL using Dual Dynamic flip-flop has the lowest PDP among the group.

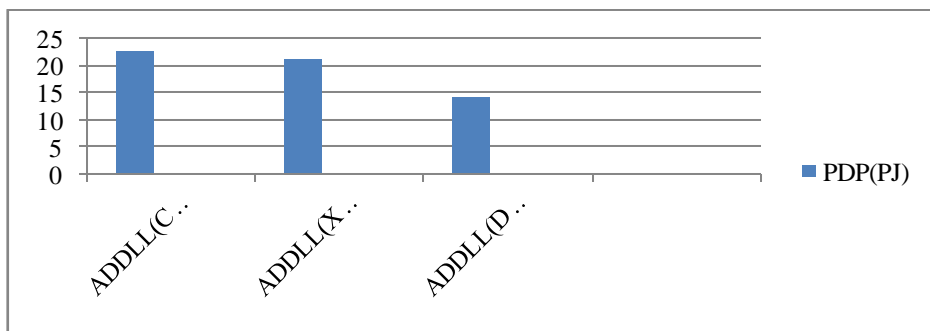


Fig. 8 PDP analysis of ADDLL under study.

The matching between the parallel paths of the EC is degraded by the random local variations. To demonstrate the device mismatch effects on EC performance, simulations are carried out on the layout extracted view of the EC with symmetric logic gates. The matching between the transistors can be improved by increasing their size. Simulations for ECs with different transistor widths are performed to study the improvement.

## VI CONCLUSION

The ADDLL is preferred because of its better stability, smaller jitter accumulation, and shorter locking time, as compared to the PLL. Since using the high performance DDFE in the design of counter, frequency divider, and phase detector, can achieve high performance DLL with minimum power consumption. If more advanced technologies were used, the performance of the DLL such as operating frequency range and jitters could be improved with a little design effort. The power consumption and the total die area would be reduced as well. The circuit is implemented in 180nm technology. And the performance is analyzed with the DLL based on conventional flip-flop and XCFF flip-flop. ADDLL using DDFE flip-flop has the lowest PDP.

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