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Time Efficient Square and Cube Architecture using Vedic Sutras

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ABSTRACT: Vedic Mathematics is an ancient system of mathematics. Square and cube are frequently performed functions in most of the DSP systems. The existing system of the thesis was based on low power square and cube architecture of 8 bit using Vedic sutras due to its frequent usage. Squaring utilised Duplex property properties of Urdhva Tiryagbhyam and cubing used Anurupyena sutra. The proposed system aimed at performing both these square and cube architectures using a single algorithm which is time efficient and have simple architecture based on Vedic mathematics. The modified system enabled performing 4-bit multiplication and addition besides 8-bit squaring and cubing. Thus the thesis comprises of a single architecture that can perfom addition, multiplication and also special case of multiplication that is square and cube of 8-bit numbers. It basically consists of a control unit and an arithmetic and logic unit. The control unit selects which operation is to be performed and accordingly the ALU unit functions and gives the result after the required number of clock cycles. The architecture is simple and time efficient.

KEYWORDS: Vedic Mathematics, Urdhva Tiryagbhyam, Anurupyena sutra, Duplex property.

I.INTRODUCTION

Vedic mathematics is the name given to ancient mathematical system which was rediscovered from the Vedas by Sri Bharati Krishna Tirthaji between 1911 and 1918. The most important feature of the Vedic mathematics system is its coherence. Instead of lengthy unrelated techniques the entire system is beautifully interrelated and unified. The general multiplication method can be easily reversed to allow one-line division also the simple squaring method can be reversed to get one-line square root. All these methods can be easily understood. The unifying quality of this system is its highlight, this makes mathematics easy and it will encourage innovation. In the past, conventional methods have been used for multiplication. Conventional methods have been highly time consuming. Heart of many of the DSP operations like Decoding, Image Compression , Demodulation are cube and square architectures. It has numerous applications in cryptography also. Since many of the DSP sytems use square and cube operations it caused greater delay in the entire system.

The objective of this paper is to design a single architecture for performing square and cube operations due to the wide usage of these mathematical operations in many digital signal processing systems as mentioned above. In the existing systems two architectures were used for square and cube operations.The main objectives of this thesis are Designing a single architecture for various mathematical operations such as 4-bit multiplication and addition and 8-bit square and cube architecture. Other objectives include: architecture should be simple as well as time efficient . When opting for the hardware implementation it should be cost effective.The architecture should be consuming less area with respect to the existing designs.

II. RELATED WORKS

Various methods of operation are used to perform square and cube architecture using Vedic mathematics in previous studies included in this field. They include:

1. To calculate the square of a number Duplex property of Urdhva Tiryagbhyam is used. In the Duplex, calculate twice the product of the outermost pair, then add twice the product of the next outermost pair, and continue till no pairs are left. If the number of bits is odd one bit will be left in the middle add its square[13].

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2. Square can also be calculated using Duplex property of binary numbers which is similar to the Duplex property of decimal numbers present in Vedic mathematics In this Duplex, take twice the product of the outermost pair, then add twice the product of the next outermost pair, and till no pairs are left. If the number of bits is odd, one bit is left in the middle, enter it as such.
3. Calculation of cube is based on the Anurupya Sutra. It states that begin with the cube of first digit then take next three numbers in Geometrical Proportion then the 4th figure present at the right end will be the cube of the second digit. If a and b are two digits, according to the Anurupya Sutra the result will be equal to $(a+b)^3$[13].
4. Yavadunam Sutra can also be applied for performing squaring as well as cubing operations of a system.
5. Conventional 8-bit multipliers, 4-bit multipliers etc are replaced by Vedic multipliers as well.

III.MODIFIED SYSTEM

The work is mainly aimed at 8-bit square and cube architecture. Suitable modifications are done to the existing system which was based on dwandwa yoga property of urdhvatiryagbhyam sutra for squaring and Yavadunam Sutra for cubing inorder to confine both the operations in one architecture whereas separate architectures were required for square and cube in the every existing systems. Also the designing of the architecture was done carefully inorder to improve the timing efficiency of the system from the previous architectures for the square and cube operations. It uses basic operations like selection, shifting, addition only. So the architecture is simple with mux, adders, shifters etc. Along with 8-bit squaring and cubing this design will also perform 4-bit addition and multiplication. This forms the modified system.

IV.OVERVIEW OF THE MODIFIED SYSTEM

The modified system is composed of two important blocks. One is the control unit and the other one is the Arithmetic and Logic Unit. As the name suggests the ALU performs the arithmetic operations and it is the control unit that determines which operation is to be performed. The overview of the system is shown in the figure 1.

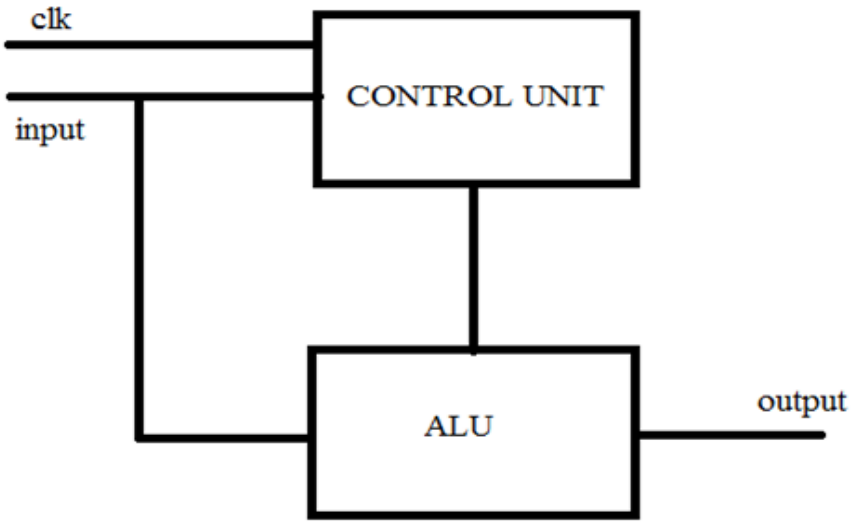

Figure 1. Block diagram of the proposed system

This proposed design can perform 8-bit square and cube operations. Also 4-bit addition ,4-bitmultiplication, 4-bit square and cube operation is possible in this design. Suppose an 8-bit input is given to the system and it is divided into 4-bit MSB,a and 4-bit LSB,b. This two 4-bit numbers can undergo multiplication of the patterns ab, 2ab, $3a^2b$, $3ab^2$, a^2b, ab^2, a^2,b^2,a^3 and b^3. Also addition of the 4-bit numbers a and b is also possible. This much variety of operations can be performed in this design and it is this control unit that determines which operation is to be performed. The control

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unit is provided with many commands. The command given to the control unit determines the operation to be performed by the arithmetic and logic unit of the proposed design.

TABLE 1 COMMANDS AND OPERATION IN CU

COMMAND	OPERATION
8'h00	$(MSB^2)(LSB)$
8'h10	(MSB)(LSB)
8'h20	(MSB^3)
8'h1A	(MSB^2)
8'h2A	(LSB^3)
8'h3A	(LSB^2)
8'h4A	$(MSB)(LSB^2)$
8'h5A	(MSB)+(LSB)
8'hAA	$INPUT^2$
8'hFF	$INPUT^3$

ALU as the name suggests is the section which performs all the arithmetic operations of the design. It can perform 8-bit square and 8-bit cube operations from the single architecture which was the main objective of our proposed design. Besides this it can perform various 4-bit operations shown in the above table apart from the 8-bit operations. It can perform 4-bit addition, multiplication, squaring and cubing operations. The selection of the operation is based on the commands given in the table 1.

V. ARCHITECTURE OF THE PROPOSED SYSTEM

The figure 2 shown below is the algorithm showing the operation upto obtaining the partial products (MSB)(LSB),$(MSB)^2(LSB)$, $(MSB)(LSB)^2$, $(MSB)^2$, $(LSB)^2$,$(MSB)^3$, $(LSB)^3$. The algorithm starts with initially storing the 8-bit input into a D-flipflop. The 8-bit input is then split into two 4-bit parts ie., 4-bit LSB and 4-bit MSB. This MSB and LSB are connected to two multiplexers. This multiplexers according to the select lines S1 and S2 selects MSB or LSB. If S1 of MUX1 selects MSB then the output of the squaring section will be $(MSB)^2$ and is S1 of MUX1 selects LSB then its otput will be $(LSB)^2$. Similarly according to the select line S2 of MUX2 the output of the multiplexer will be (MSB) or (LSB). Then the output of the multiplexer with select line S3 of MUX3 will be $(MSB)^2$ or $(LSB)^2$ or otherwise (MSB) or (LSB). The output of MUX2 and MUX3 are given to the vedic multiplier. Also the output of the MUX3 is also given to MUX6.

The output of the multiplier is stored in a D flip flop so that output doesnot change with the change in the output. The output of the DFF is given to a leftshifter and an adder. The input given to the left shifter is also given to the MUX6. The input to the MUX4 is the combination of the output of the left shifter and adder. The output of the MUX4 is selected by the select line S4. It is given to the MUX 5 which is controlled by the select line S5. Output of the MUX5 is stored in a 16 bit DFF which forms the partial product of the system. The value stored in the 16 bit DFF may be

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$(MSB)^2(LSB)$, $(MSB)(LSB)^2$, $(MSB)^2$, $(LSB)^2$,$(MSB)^3$, $(LSB)^3$ or (MSB)(LSB). This value depends on the select line S1,S2,S3,S4,S5, S6.

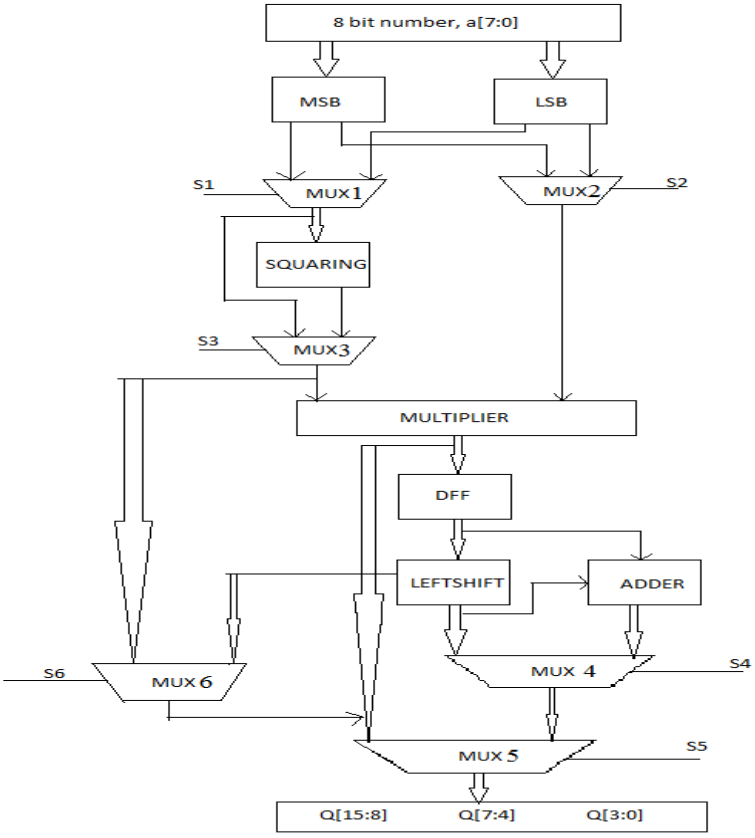

Figure 2 Algorithm showing partial product of the proposed system

The 16-bit partial product stored in the D flipflop as shown in Figure 2 is then coined with 6 zero bits in the MSB to form a 22 bit value and it is stored in a 22 bit DFF as shown in Figure 3. Consider the 22 bit number is Q[21:0], from this Q[11:0] is stored in DFF1. The output of DFF1 is stored in DFF2 inorder match with the time delay. Q[17:0] is stored in DFF4 along with [3:0] bits from the output of DFF2. The output of DFF4 is given to a ripple carry adder RCA2, the inputs to RCA2 are [7:0] bits of the output DFF4 and [21:8] bits of the output DFF4. The output of RCA2 is given as input to DFF3 along with Q[21:18] as LSB. The output of DFF3 is given to RCA 1 by dividing the input into [9:0]bits and [21:10] bits.

The output of RCA1 is given to DFF6 and the output of RCA2 is given to DFF7. The input of DFF6 and DFF7 are given as inputs to the MUX7. The output of MUX7 depends on the select line S. Its output is given to DFF5 which is given as input to RCA 3 with the bits split into two similar as RCA1. The output of RCA 3, DFF6, and DFF7 are stored in a D flipflop which is named as CUBEOUT in the figure . The output of RCA3, DFF2 and DFF7 are stored in a D flipflop named SQUAREOUT. The value stored in the CUBEOUT is the cube output of the given 8-bit input and the value stored in the SQUAREOUT is the square output of the given 8-bit input. CUBEOUT and SQUAREOUT are given as input to MUX8 whose select line is s. This select line determines whether to output square or cube depending on the commands given to the control unit. Also it can perform 4-bit multiplication and 4-bit addition operations depending on the commands of control unit as discussed in the control unit section.

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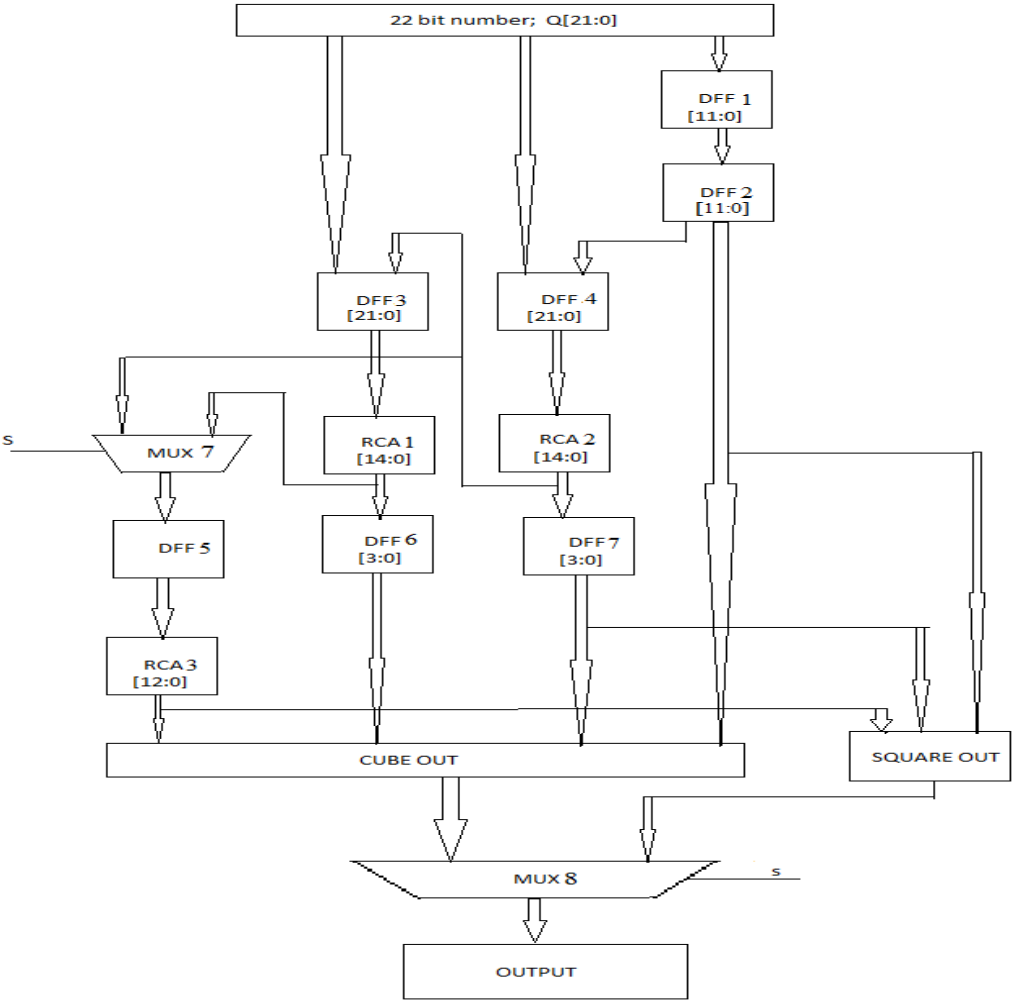

Figure 3 Algorithm showing the operation of the proposed system

Thus, the 8-bit number is given as input as shown in figure 2 and a partial product is obtained as the output of the algorithm. Then it is given as input of the algorithm shown in figure 3 and we can obtain the final output at the end of operations as shown in the algorithm.

VI. RESULTS

The simulation results of the proposed system includes the simulation of the single architecture showing both the square and cube output along with multiplication and addition operations. The simulation result shown in figure 4 includes the square and cube output and also the 4-bit multiplication output. . In the figure the result named A is the input given to the architecture, 'in' represents the commands in the control unit, clk is the clock cycle and Y is the output of the existing square and cube architecture.

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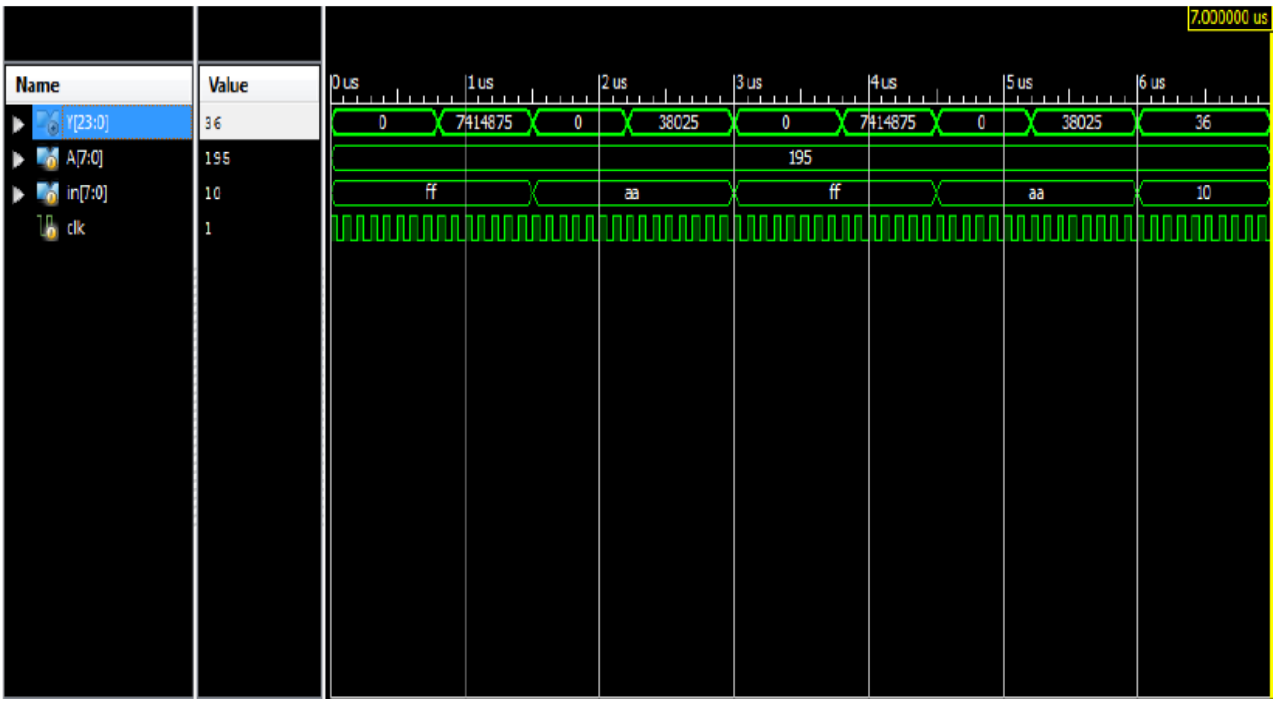

Figure 4 Proposed architecture along with 4-bit multiplier

The final simulation results of the proposed system shown in figure 5 includes the 8-bit square and cube output and also the 4-bit multiplication and 4-bit addition output of the system. . In the figure the result named A is the input given to the architecture, 'in' represents the commands in the control unit, clk is the clock cycle and Y is the output of the existing square and cube architecture.

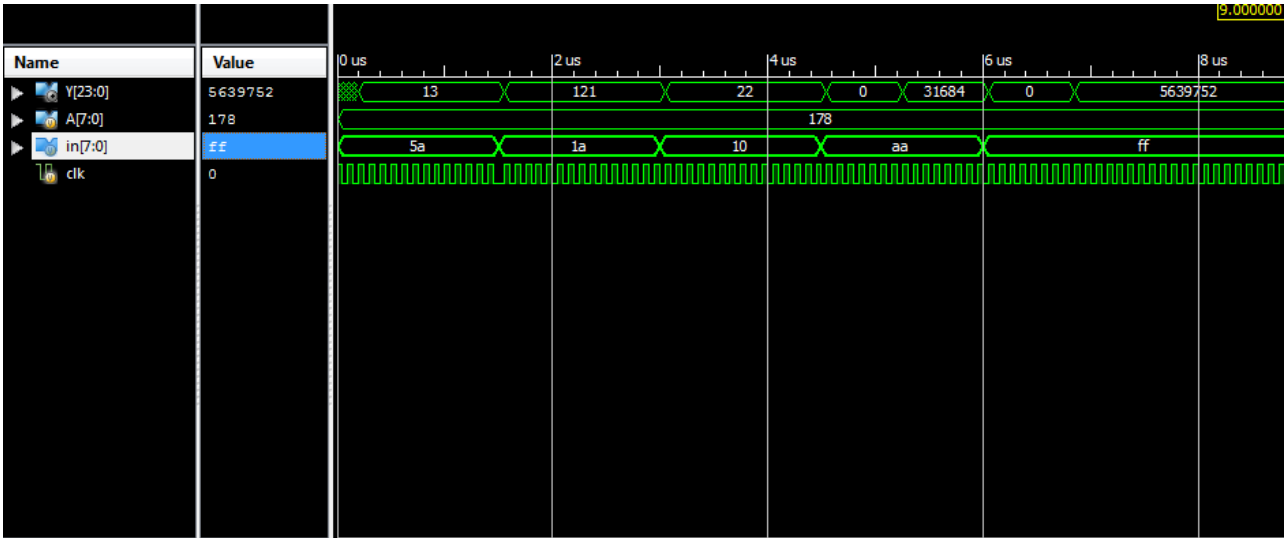

Figure 4 Proposed architecture along with 4-bit multiplier and adder

From the synthesis reports it can also be inferred that delay occurring in the existing square system is 5.7ns which is lesser than the conventional methods whose delay is 27ns. Delay occurring in the existing cube system is 7ns which is lesser than the conventional methods whose delay is 41ns. Delay occurring in the proposed system for the calculation

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of square and cube is 3ns only which has a higher margin than the conventional methods whose delays were 27ns and 41ns respectively.

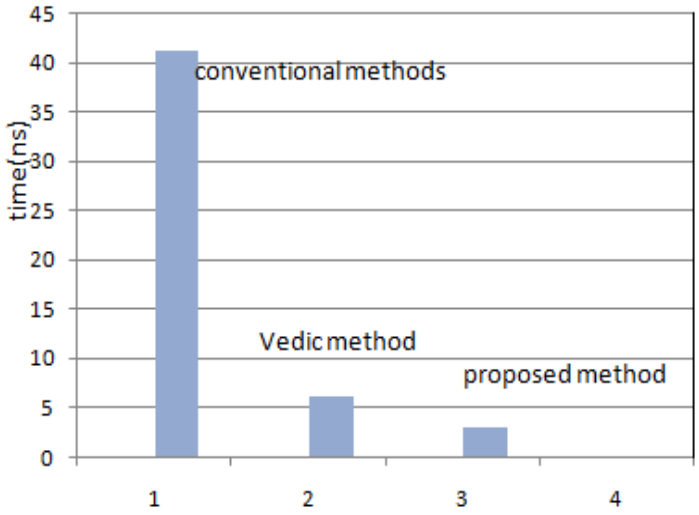

Figure 5 Time delay comparison graph of three systems

Synthesis reports shows that for calculating the cube of an 8-bit input the architecture utilizes 349 number of LUTs. This LUTs are used for the calculation of cube operation alone. For calculating the square of an 8-bit input the architecture utilizes 58 number of LUTs. This LUTs are used for the calculation of square operation only. Thus for calculating square and cube simultaneously a total of 407 LUTs are required. For the proposed system,the architecture utilizes 349 number of LUTs. This LUTs are used for the calculation of square,cube, multiplication and addition operations simultaneously. So the proposed system utilises less number of LUTs as compared to that of the existing system. Hence it uses less area than the previous architectures.

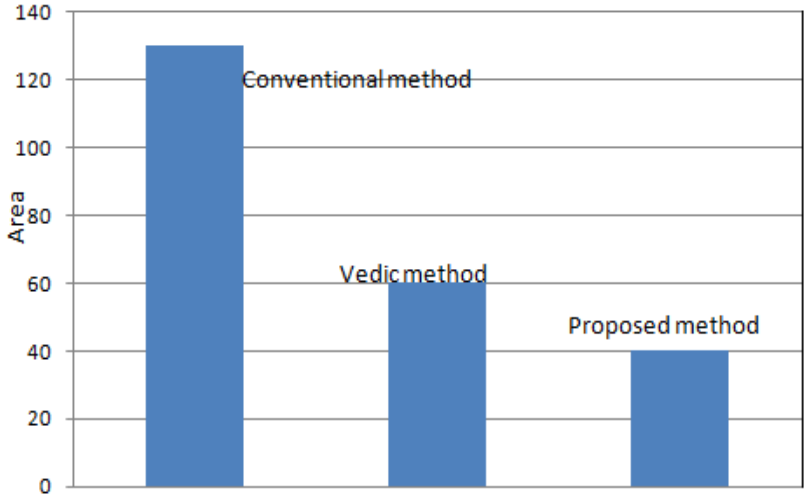

Figure 6 Area comparison graph of three systems

From the graphs it can be inferred that the whole system consumes less area and is time efficient.

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VII. CONCLUSION

In this work designing and the simulation of a single architecture for performing 8-bit square and 8-bit cube operations is mainly done. The system is designed in such a way to include multiplication and addition operation of 4-bit numbers also. The main purpose of the thesis is the time efficient operation of the design inorder to increase the overall performance of the system utilising this design. Digital signal processing systems are the systems mainly utilising square and cube operations. It is the bottleneck of many of the DSP operations hence by increasing the speed of square and cube operations we can improve the overall performance. The aim of this project was to achieve two objectives. Firstly,to propose a new architecture to improve the timing efficiency of the square and cube operation. Secondly, to ensure that the both the operations is performed using a single architecture . Also the architecture designed should be simple and utilises less area. In contradiction to the previous systems square and cube operations were done using a single architecture which is time efficient, simple and consumes less area.

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