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An Integrated Step-Down Converter Using Single-Stage Single-Switch Double Buck Converter

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ABSTRACT: This paper discusses the design of a new transformerless single-stage single-switch double buck converter (ISSSSDB) which integrates a buck-type power factor correction (PFC) cell with a buck-type dc–dc output cell in a special way. High input power factor can be obtained automatically by operating the PFC cell inductor in discontinuous conduction mode (DCM), where the well and tight output voltage is regulated by the DC-DC cell. The advantages of this converter are low voltage stress across the dc-link capacitor, low current stress on the switch, and high step down input to output voltage, low cost and reduced size. These characteristics makes the converter cost-efficient, easy-to-design, and suitable for the low-power and non-isolated applications. The results are validated by simulating ISSSSDB using MATLAB/Simulink.

KEYWORDS: Double buck AC-DC Converter, Power Factor Correction, single-stage single-switch converter, Discontinuous conduction mode, Buck type DC-DC converter.

I.INTRODUCTION

Many industrial applications require not only a tight dc voltage to feed their loads, but also a high-input power factor(PF) to reduce harmonic distortion in the current drawn from the electric power utility. The active PFC techniques have rapidly become a vigorous research topic in the power electronics field and considerable efforts have been made on the development of the PFC converters. Active PFC techniques are usually divided into two categories: single-stage and two-stage approaches. The single-stage approach improves the power factor and high step down feature using single converter [1-3]. The output voltage of single-stage approach has high ripples at twice of line frequency. These ripples get even higher when the output voltage becomes lower and the load becomes heavier. The other solution is using a PFC converter in cascade with a dc–dc converter, with which the instantaneous input power and the stable output power can be decoupled by an intermediate dc-link capacitor [4-8].The two- stage approach can achieve good performance such as high power factor, low voltage stress and tight output voltage regulation. The major drawbacks of the two-stage approach are its high cost, larger size, and complex control, particularly in low-power applications. To compromise the size, cost, and performance, many single-stage single-switch (S4) converters have been proposed. The S4 converters can be treated as an integration version of the two-stage structure, in which the switches in the PFC and dc–dc converter are combined as one. Several advantages can be obtained using this integration approach: 1) the PFC and dc–dc cells share one switch, the size and cost can be reduced; 2) the high input PF can be obtained automatically by the PFC cell with the discontinuous conduction mode (DCM), only the output voltage needs to be regulated, the controller can be simple; and 3) the input and output power can still be decoupled since the intermediate dc-link capacitor is remained. Therefore the voltage ripples in the output are alleviated. Due to these features, S4 converters are especially suitable for the low- power applications with critical size and cost limitations.

The single-stage single-switch (S4) converters with galvanic isolation have been well studied in the past decades [9]–[11]. However, in some lighting applications, galvanic isolation is not mandatory by the safety requirements. Recently, several transformerless S4 converters have been presented. The boost/buck-boost S4 converter is presented

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in [12]. The boost PFC cell provides a good input PF, but it also requires a high dc- link voltage, which degrades the converter's step-down feature. The S4 converters with buck-boost PFC cells [13] reduce the dc-link voltage, and the voltage step-down can be realized by a buck [14], quadratic buck [15], or buck-boost [16] cell. However, the single switch in the aforementioned converters needs to handle the currents of both cells, which leads to the thermal problem of the switch. In [17] a Double buck S4 converter is proposed to further reduce the dc-link voltage and enhance the step-down feature, and the single-switch does not need to handle the currents of both cells.

II.PROPOSED ISSSSDB CONVERTER AND ITS OPERATION PRINCIPLE

The proposed ISSDB converter is obtained by merging of a buck PFC cell (L, D_1, Da, C_O, and C_b), in which V_{in} is treated as input, C_b in series with C_o is treated as output and a buck dc/dc cell (L_2, S_1, D_a, C_O, and C_B) as illustrated in Fig.1. When both cells are operating in discontinuous conduction mode (DCM) there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle t_0.

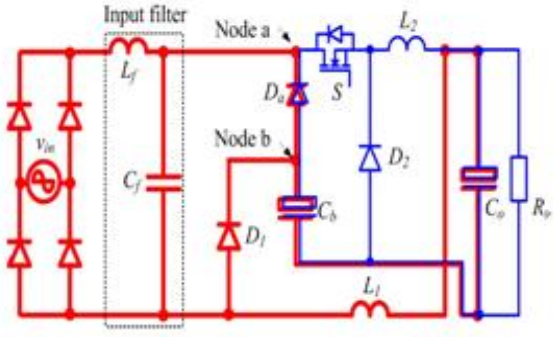

Fig.1Integrated single-stage single-switch double buck converter

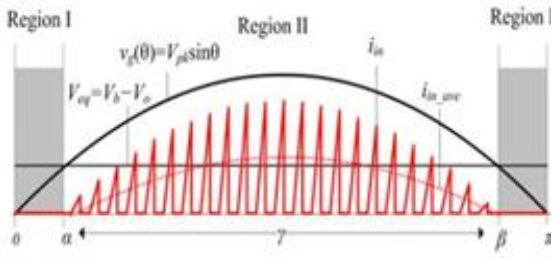

Fig.2 Input voltage and current waveforms

The proposed S4 converter includes a buck-type PFC cell, therefore, two working regions can be found within half of line-cycle period, as shown in Fig. 2. With the proposed integration, the equivalent voltage Veq = Vb−Vo acts as the sink of the PFC cell, the rectifier does not conduct when vg (θ) <Veq, this interval is defined as Region I. oppositely, if Vg (θ) > Veq, the rectifier conducts and an input current i_{in} appears. This interval is defined as Region II. The start point α and end point β of Region II shown in Fig. 2.The circuit operation over a switching period can be divided into three stages and the corresponding sequence is shown in Fig.3 (a), 3(b), and 3(c). The current waveforms are shown fig.4.

A. OPERATIONAL MODES IN REGION I

M1 (t_0− t_1) (period M1 in Fig.4) [see Fig. 3(a)]
When Switch S_1 is turned ON, the voltage applied on L_2 is $V_{eq} = V_b−V_o$, i_{L_2} increases linearly from zero with the slope V_{eq} /L_2 on the other hand, the voltage applied on the rectifier diodes is vg (θ)−V_{eq} . Noticing $V_{g(\theta)} < V_{eq}$ in this region, the rectifier is blocked, there is no current flowing through L_1, $i_{L1} = i_{in} = 0$. This mode will persist until S is turned OFF at t_1.

M2 (t_1− t_2) (period M2 in Fig. 4) [see Fig.3 (b)]
When Switch S_1 is turned OFF, i_{L2} is freewheeling through S_2 (since S_2 is turned on), i_{L2} decreases linearly with the slope Vo /L_2. The current flowing through C_b and S is now zero; in the PFC cell, i_{L1} and i_{in} are also zero, which is the same as M1. This mode will persist until i_{L2} decreases to zero at t_2.

M3 (t_2 − t_3) (period M3 in Fig.4) [see Fig.3(c)]
Once i_{L2} decreases to zero, it keeps zero until S is turned ON again. In this mode, only the energy in Co is released to Ro, the currents flowing through L_1, L_2, C_b and S are all zero. Obviously, the dc–dc cell is actually a buck converter working in the DCM, while the PFC cell is deactivated during this region.

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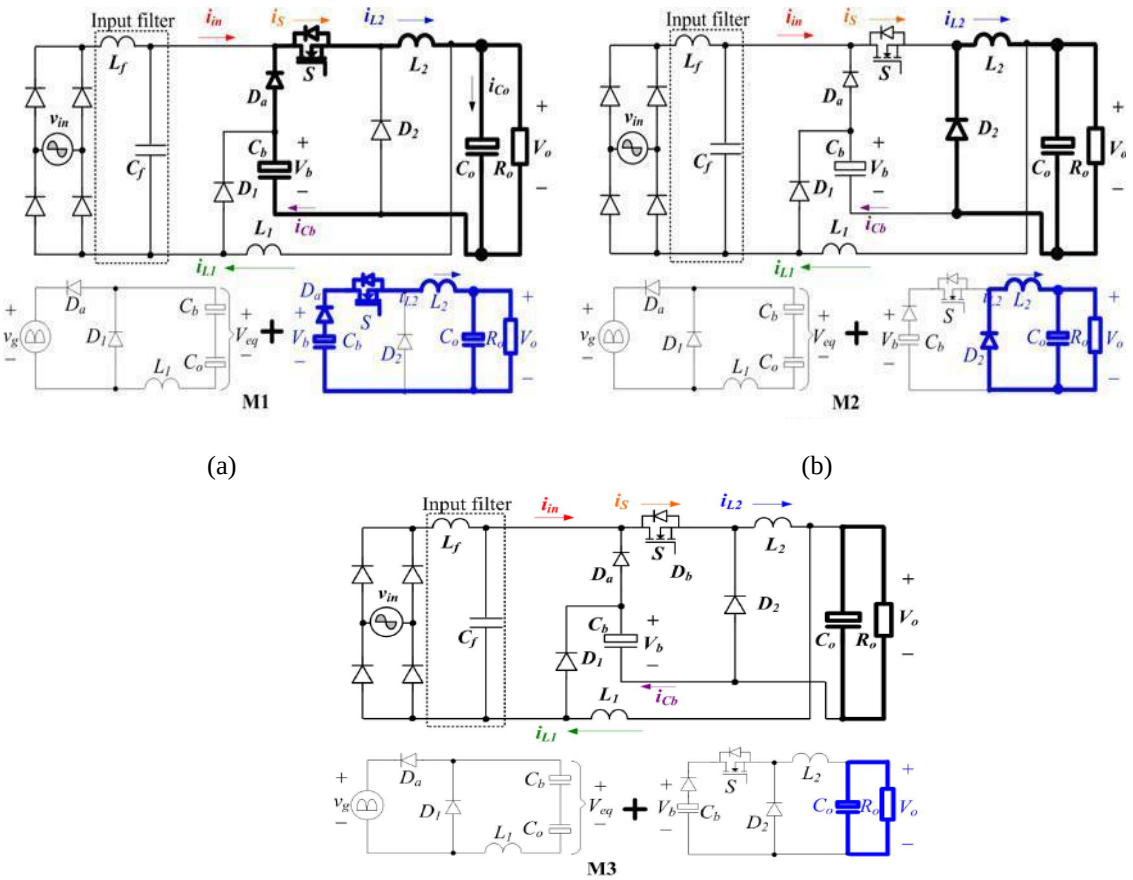

(a) (b)

(c)

Fig.3 Circuit operation stages of region I of proposed converter

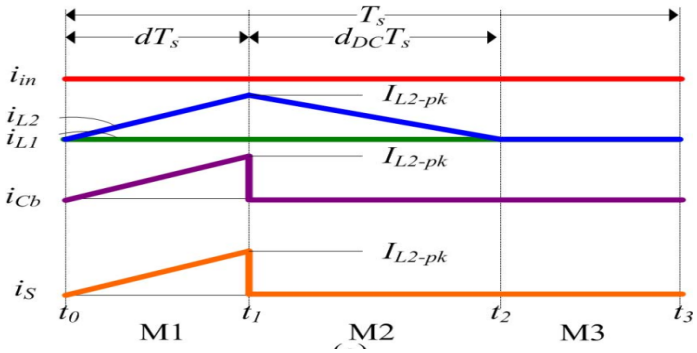

Fig.4 Current waveform of the proposed circuit in region I

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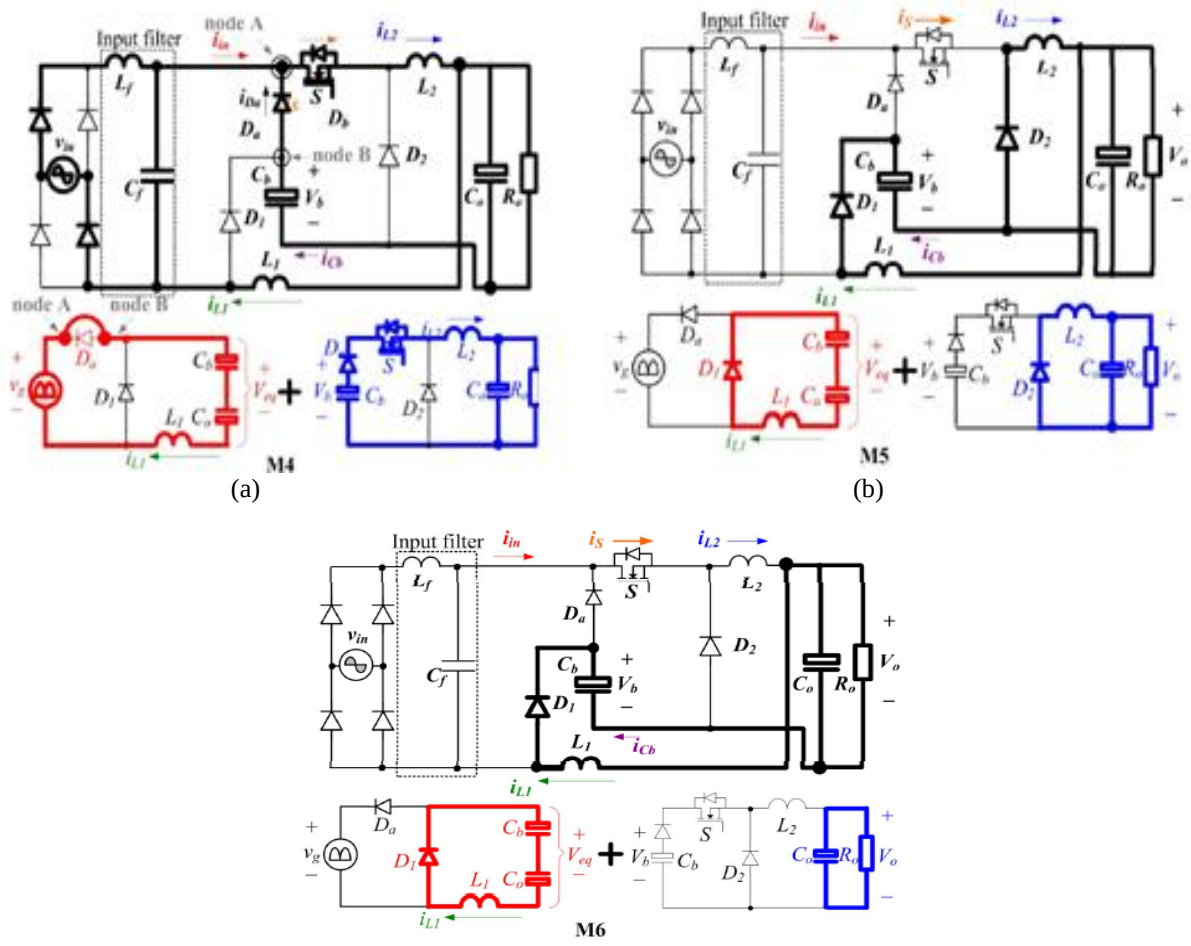
B.*OPERATIONAL MODES IN REGION II*

M4 (t_0–t_1) (period M1 in Fig.6) [see Fig.5 (a)]
When S1 is turned ON in this case, the voltage across L_2 is $V_{eq} = V_b - Vo$, which is the same as that in M1. And since D_a also conducts, nodes a and b have the same voltage levels, it means the voltage applied on L_1 is $V_{g(\theta)} - V_{eq}$. Noticing $V_{g(\theta)} > V_{eq}$, the rectifier is conducted and i_{L1} begins to increase linearly from zero with the slope $[vg\ (\theta) - Veq\ ]/L_1$. It means $i_S > i_{in}$ or equivalently $i_{L2} > i_{L1}$ must be satisfied, this mode will persist until t1
when S is turned OFF.

M5 (t_1–t_2) (period M2 in Fig.6) [see Fig.5 (b)]
When S1 is turned OFF. In the dc–dc cell, i_{L2} is freewheeling through S2, the voltage applied on L_2 is −Vo, and therefore i_{L2} decreases linearly with the slope $-Vo/L_2$, and finally reaches zero at t_2. In the PFC cell, i_{L1} is freewheeling through D1 the voltage applied on L1 is $-V_{eq}$, iL1 decreases with the slope $-V_{eq}/L_1$. In this mode, i_{in} keeps zero and i_{Cb} always equals to $-i_{L1}$.

M6 (t_2–t_3) (period M3 in Fig. 6 [see Fig.5(c)]
When i_{L2} has decreased to zero, i_{L1} keeps decreasing because the voltage applied on L_1 is still V_{eq}. I_{L1} will finally reach zero at t_3.



(a) (b)

(c)

Fig.5 Circuit operation stages of region II of proposed converter

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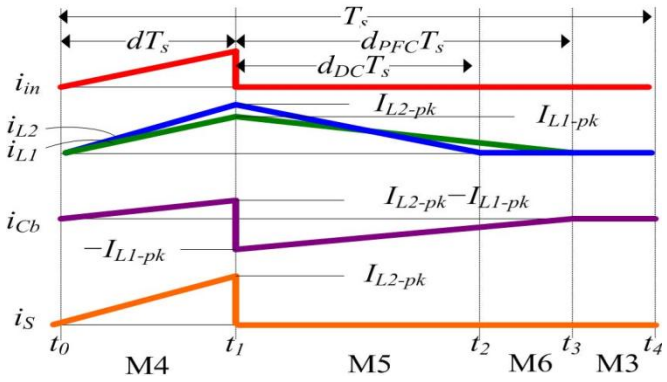

Fig.6 The key waveforms of the proposed S4 converter in region II

III. DESIGN OF ISSSSDB CONVERTER

The ISSSSSDB converter is designed as follows for simulation in Matlab. The input voltage of the converter can be varied between (90-270Vrms.

Let the input voltage be, Vin = (260Vrms)
Switching frequency = 20 kHz
Output power = 100W
Output voltage = 19 Vdc
Power factor = > 98%
Intermediate bus voltage = < 160V

Switch control = Closed loop PI control

In order to design the circuit components, first find the Peak-input to equivalent sink ratio Mpe.

$M_{pe} = \frac{Veq}{Vpk}$, where Veq= Vb-Vo (1)

$Vg(\theta) = |V_{in}| = V_{pk}\sin\theta \quad \in [0, \pi]$ (2)

dead angles,

$\alpha = \arcsin(V_{equ} \div V_{pk})$ (3)

$\beta = \pi - \alpha = \pi - \arcsin(V_{equ} \div V_{pk})$ (4)

To find the value of inductor, use the following equations

$$L = \frac{2\pi M_{pe}^2}{\pi - 2\arcsin M_{pe} - 2 \cdot M_{pe}\sqrt{1-M_{pe}^2}} \quad (5)$$

Current flows through the inductor L_1 and L_2 is calculated by

$$I_{L1-pk} = I_{in-pk} = \frac{v_g(\theta) - V_{eq}}{L_1} dT_s$$

$$I_{L2-pk} = \frac{V_{eq}}{L_2} dT_s \quad (6)$$

IV. SIMULATION RESULTS

The performance of the proposed circuit is verified by Using MATLAB/ Simulink. To ensure the converter working properly with constant output voltage, a simple voltage mode control is employed. To achieve high performance of the converter for universal line operation in terms of low bus voltage (< 160V) and high power factor, the inductance ratio has to be optimized. The lower the bus voltage of the converter, the lower voltage rating capacitor (160 V) can be used. The simulation model of proposed ISSSSDB converter is shown in Fig.7.

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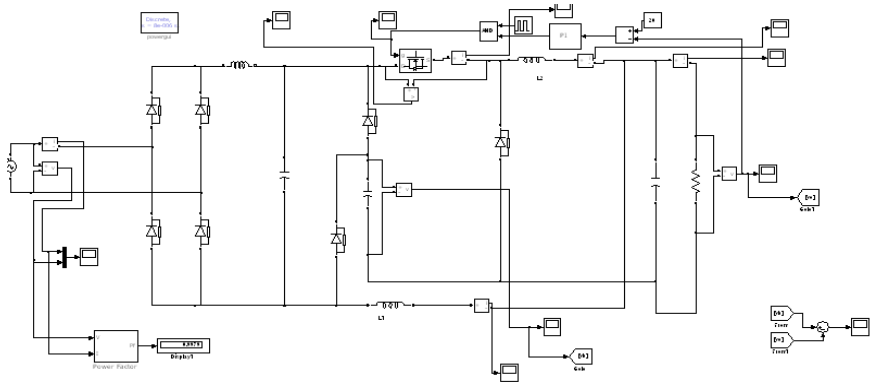

Fig.7 Simulation of proposed ISSSDB converter

The input voltage, input current, bus capacitar voltage, output voltage are shown in Fig.8

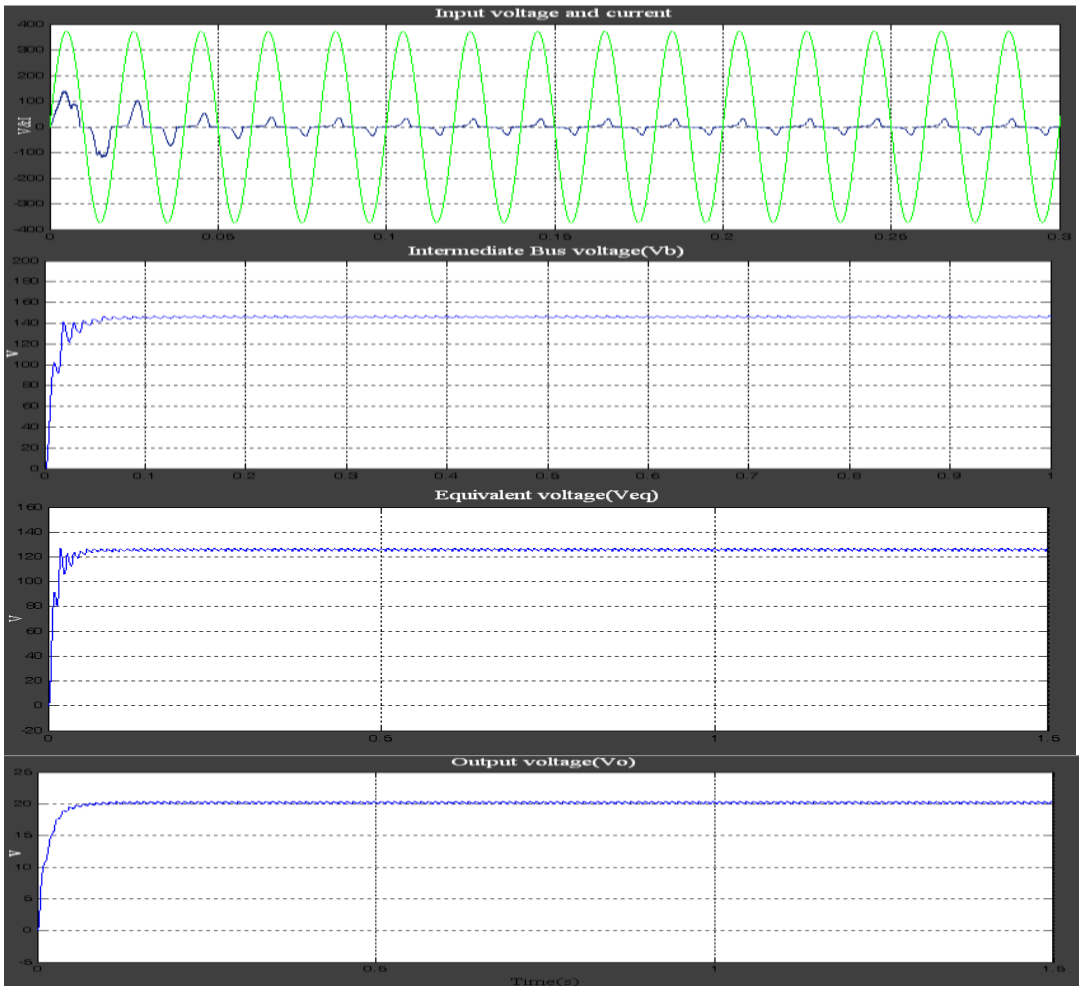

Fig.8 The ISSSSDB waveformes of (a) Input voltage and current (c) Intermediate bus voltage (d) Output voltage for input voltage 260 Vrms

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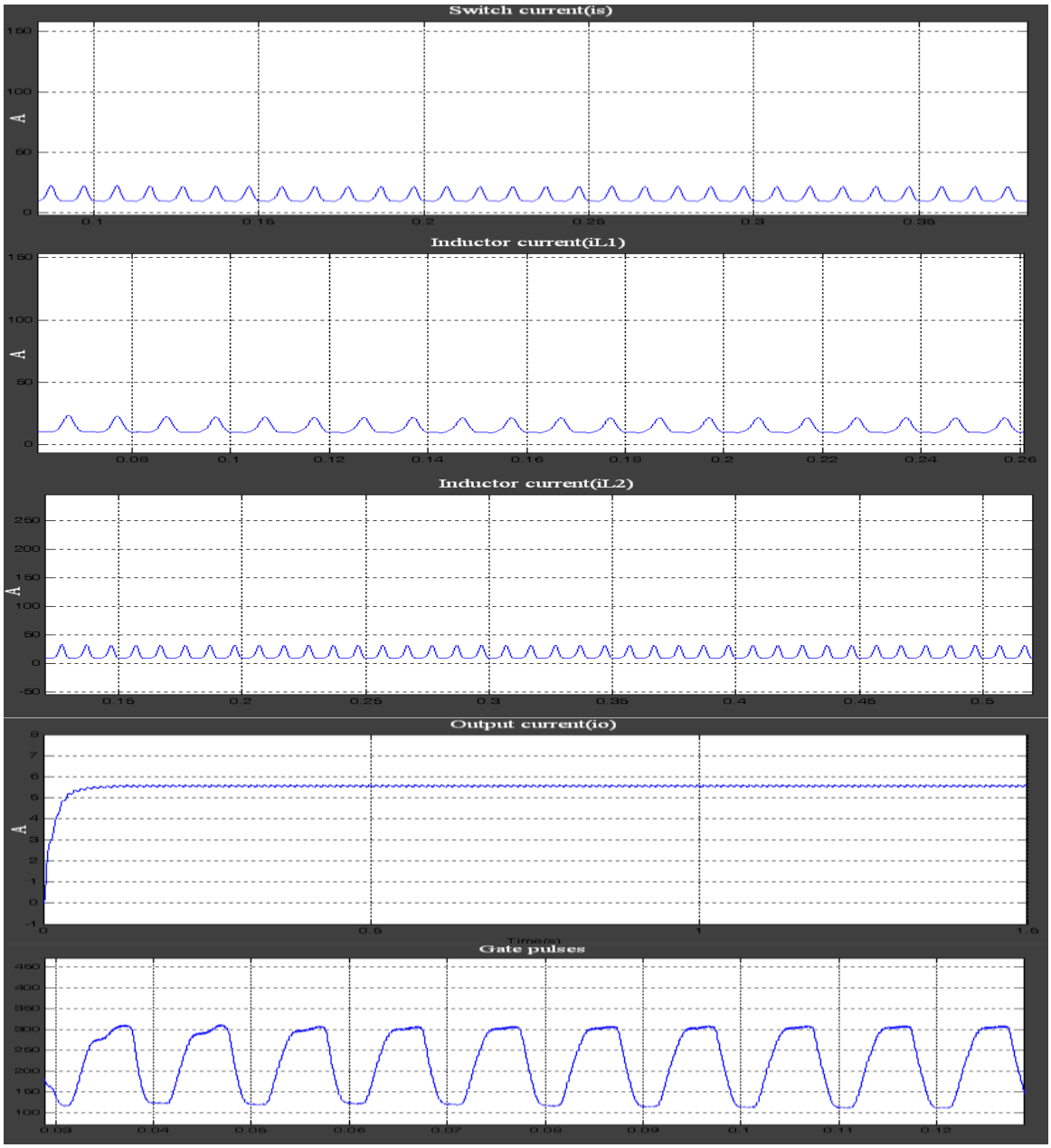

Fig.9 The ISSSSDB waveformes of (a) switch current (b) Inductor1 current(i_{L1}) (c) Inductor2 current(i_{L2}) (d) Output current(e) Gate pulses for input voltage 260 Vrms

The currents in inductor (i_{L1}), inductor (i_{L2}), switch current (Is), gate pulses and output current (Io) are shown in Fig.9.From fig.9 it is clearly seen that high AC input(260 Vrms) is stepped down to low DC output voltage(19v) without using high step down transformer and have low intermediate bus voltage, usually(135V) for a given 260 AC.

The power factor of the proposed ISSSDB converter as shown in fig.10.The power factor of the proposed converter is 0.99.i.e. high power factor is automatically achieved by operating the PFC cell in discontinuous conduction mode.

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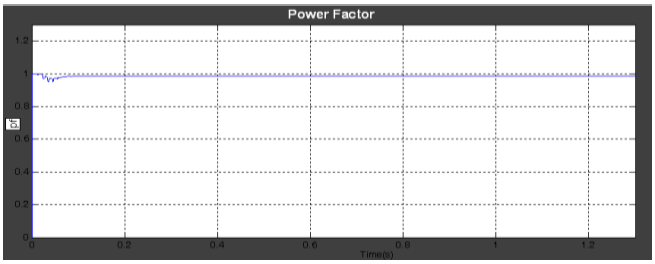

Fig.10 Power factor of the converter

V. CONCLUSION

The ISSSSDB converter is designed and results are verified. The proposed ISSSSDB converter has the following advantages: Due to the integration of two buck cell, a high step-down feature is obtained, the buck PFC cell leads to a low dc link capacitor voltage not greater than 160V, voltage stress is low, the switch in the converter needs to handle the current of the DC-DC cell, current stress is low, high power factor and low total harmonic distortion, low cost and small size. Due to these benefits, the proposed S4 converter can be treated as a cost-efficient candidate for the low power, nonisolated, applications where a high input PF and a stable output are required

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