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Hybrid Fuzzy-PI Controller Based MC-UPQC for Power Quality Enhancement

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ABSTRACT: Power quality problems like voltage sag/swell, flickers, interruptions, voltage distortions and imbalance can have drastic effects on home appliances, industries, processing plants and other applications. In this paper, a novel multi-converter unified power quality conditioner (MC-UPQC) is proposed for simultaneous compensation of voltage and current in multibus/multifeeder distribution systems. A MC-UPQC is a combination of one shunt active power filter (APF) and two or more series APFs. MC-UPQC can be applied to adjacent feeders to compensate for supply-voltage and load current imperfections on the main feeder and full compensation of supply voltage imperfections on the other feeders. In this paper, a two feeder MC-UPQC is used, which has one shunt APF and two series APFs. All APFs are connected back to back on the DC side and share a common DC link capacitor. As control of this DC link capacitor is very critical for the better performance of MC-UPQC, a novel hybrid fuzzy-PI controller is designed, which is more robust to parameter changes, is non-linear and has a fast dynamic response along with superior steady state response. Through simulation results, it is shown that the hybrid fuzzy-PI controller has performed very well and MC-UPQC is able to compensate supply voltage and load current imperfections on feeder1 and fully protect the sensitive/critical load on feeder2 against distortion, sag/swell, and interruption.

KEYWORDS: multiconverter unified power quality conditioner, multifeeder distributed system, power quality enhancement, hybrid fuzzy-PI control, SRF based control, hysteresis current control, dc voltage control.

I. INTRODUCTION

With increasing applications of nonlinear and power electronic converters in distribution systems and industries, consumers are concerned not only about continuity of supply but also the quality of power being supplied. Although the power electronic converter based power processing offers higher efficiency, compact size and better controllability, due to switching actions, these systems behave as non- linear loads.Therefore, whenever, these systems are connected to utility, they draw non-sinusoidal and /or lagging current from source. As a result these systems behave as loads having poor displacement as well as distortion factors, drawing considerably high reactive volt-amperes from the utility and inject harmonics in the power supply networks. Various problems such as voltage sags/swells, voltage interruptions, voltage imbalances, harmonics, voltage flickers, undervoltages and over voltages result in poor power quality. This lack of standard quality power can cause loss of production, damage of equipment and appliances.On the other hand, an increase of sensitive loads involving digital electronics and complex process controllers requires a pure sinusoidal supply voltage for proper load operation [1].

Extensive work has been done in order to resolve these power quality problems [2-7].Several new techniques were developed among which shunt Active Power Filter (APF) is one of the most promising methods to tackle the current related problems, whereas series APF is most suitable for voltage related problems [8-9]. In recent years, solutions based on flexible AC transmission systems (FACTS) have appeared. The application of FACTS concepts in distribution systems has resulted in a new generation of compensating devices. A unified power-quality conditioner (UPQC) [10] is the extension of the unified power-flow controller (UPFC) [11] concept at the distribution level. It consists of combined series and shunt converters for simultaneous compensation of voltage and current imperfections in a supply feeder [12–14].

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Recently, multi-converter FACTS devices, such as an interline power-flow controller (IPFC) [15] and the generalized unified power-flow controller (GUPFC) [16] are introduced. The aim of these devices is to control the power flow of multilines or a subnetwork rather than control the power flow of a single line by, for instance, a UPFC.When the power flows of two lines starting in one substation need to be controlled, an interline power flow controller (IPFC) can be used. An IPFC consists of two series active power filters (APF) whose DC capacitors are coupled. This allows active power to circulate between the APFs. With this configuration, two lines can be controlled simultaneously to optimize the network utilization.

This concept can be extended to design multiconverter configurations for PQ improvement in adjacent feeders. For example, an interline unified power quality conditioner (IUPQC), which is the extension of the IPFC concept at the distribution level, has been proposed in [17]. The IUPQC consists of one series and one shunt converter. It is connected between two feeders to regulate the bus voltage of one of the feeders, while regulating the voltage across a sensitive load in the other feeder. However, since the source impedance is very low, a high amount of current would be needed to boost the bus voltage in case of a voltage sag/swell which is not feasible. It also has low dynamic performance because the DC link capacitor voltage is not regulated.

Here, a new configuration of a UPQC called the multiconverter unified power-quality conditioner (MC-UPQC) is presented. The system is extended by adding a series-APF in an adjacent feeder. MC-UPQC can be used for simultaneous compensation of voltage and current imperfections in both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected.

II. MC–UPQC CONFIGURATION

The single-line diagram of a distribution system with an MC-UPQC is shown in
Figure 1 [18]. As shown in this figure, two feeders connected to two different substations supply the loads L1 and L2. The MC-UPQC is connected to two buses BUS1 and BUS2 with voltages of U_{t1} and U_{t2}, respectively. The shunt part of the MC-UPQC is also connected to load L1 with a current of I_{L1}. Supply voltages are denoted by U_{s1} and U_{s2} and load voltages by U_{L1} and U_{L2}. Finally, feeder currents are denoted by I_{s1} and I_{s2} and load currents are I_{L1} and I_{L2}.

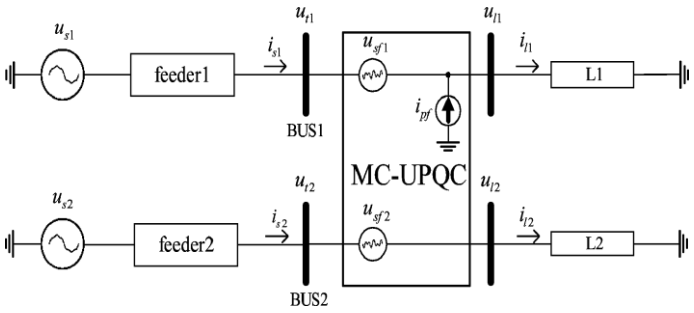

Figure 1: Single-line diagram of a distribution system with an MC-UPQC [18]

Bus voltages U_{L1} and U_{L2} are distorted and may be subjected to sag/swell. The load L1 is a nonlinear/sensitive load which needs a pure sinusoidal voltage for proper operation while its current is non-sinusoidal and contains harmonics. The load L2 is a sensitive/critical load which needs a purely sinusoidal voltage and must be fully protected against distortion, sag/swell, and interruption. These types of loads primarily include production industries and critical service providers, such as medical centers, airports, or broadcasting centers where voltage interruption can result in severe economic losses or human damages.

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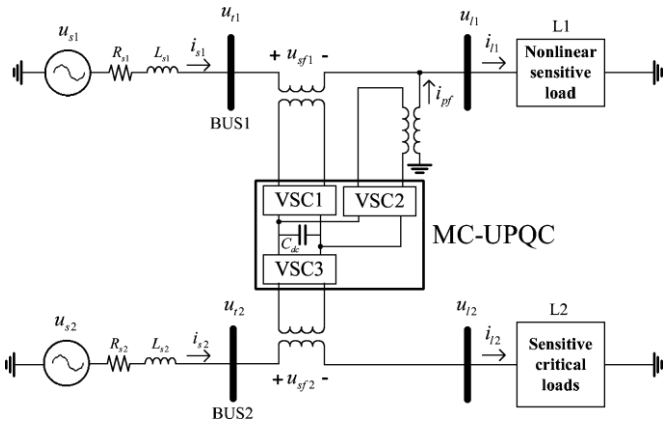

Figure 2: Typical MC-UPQC used in a distribution system [18]

The internal structure of the typical MC–UPQC used in a distribution system is shown in Figure 2. It consists of three APFs (APF1, APF2, and APF3) which are connected back to back through a common DC-link capacitor. In this configuration, APF1 is connected in series with BUS1 and APF2 is connected in parallel with load L1 at the end of Feeder1. APF3 is connected in series with BUS2 at the end of feeder2. Each of the three APFs in Figure 2 is realized by a three-phase converter with a commutation reactor and high-pass output filter which prevents the flow of switching harmonics into the power supply.

As shown in Figure 2, all converters are supplied from a common DC-link capacitor and connected to the distribution system through a transformer. Secondary (distribution) sides of the series-connected transformers are directly connected in series with BUS1 and BUS2, and the secondary (distribution) side of the shunt-connected transformer is connected in parallel with load L1. The aims of the MC-UPQC are:

1) To regulate the load voltage U_{L1} against sag/swell and disturbances in the system to protect the nonlinear/sensitive load L1;
2) To regulate the load voltage U_{L2} against sag/swell, interruption, and disturbances in the system to protect the sensitive/critical load L2;
3) To compensate for the reactive and harmonic components of nonlinear load current I_{L1}.

In order to achieve these goals, series APFs (i.e., APF1 and APF3) operate as voltage controllers while the shunt APF (i.e., APF2) operates as a current controller.

III. CONTROL STRATEGIES

The performance of an APF depends on the design characteristics of the currentcontroller. The control scheme of a shunt active power filter must calculate the current reference waveform for each phase of the inverter, maintain the DC link voltage constant and generate the inverter gating signals. Also, the compensation effectiveness of an APF depends on its abilityto follow the reference signal calculated to compensate the distorted load current with aminimum error and time delay.The current reference circuit generates the reference currents required to compensate the load current harmonics, load reactive power and also to maintain the DC link voltage constant. Synchronous Reference Frame (SRF) based control is used to achieve this objective.

Synchronous Reference Frame (SRF) based control:

In this control, the three phase load currents I_a, I_b and I_c are transformed into α-β frame using the following transformation relations [19]:

$$\begin{pmatrix} p \\ q \end{pmatrix} = \begin{pmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{pmatrix} \begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} \qquad \text{Equation 1}$$

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Where p and q are active and reactive powers respectively. From equation 1, we get:

$$\begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} = 1/(v_\alpha^2 + v_\beta^2)\begin{pmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{pmatrix}\begin{pmatrix} p \\ q \end{pmatrix} \qquad \text{Equation 2}$$

These load currents presented in the α-β frame are transformed into synchronous reference frame as shown below:

$$\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{pmatrix}\begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} \qquad \text{Equation 3}$$

The reference frame is synchronised with the supply voltages and rotates with the same frequency. A Phase Locked Loop (PLL) is needed for implementing this method. I_d and I_q are composed of DC and AC components as

$$I_d = \overline{Id} + \widetilde{Id} \qquad \text{Equation 4}$$

$$I_q = \overline{Iq} + \widetilde{Iq} \qquad \text{Equation 5}$$

The DC components $\overline{Id}$ and $\overline{Iq}$ correspond to the fundamental load currents and the AC components $\widetilde{Id}$ and $\widetilde{Iq}$ correspond to the load currents harmonics. Component $\widetilde{Iq}$ corresponds to the reactive power drawn by the load. The isolation of the AC component can be achieved by filtering out the DC offset. The compensation reference signals are obtained from the following expressions:

$$I_{d,ref} = -\widetilde{Id} \qquad \text{Equation 6}$$

$$I_{q,ref} = -\overline{Iq} - \widetilde{Iq} \qquad \text{Equation 7}$$

This means that there will be no harmonics and reactive components in the system currents after the compensation. However, in real time, capacitor voltage may vary due to switching loss or other disturbances such as imbalance and sudden load variations. Thus an extra term to account for capacitor voltage balancing needs to be added in, which is shown below in the Figure 3 [20].

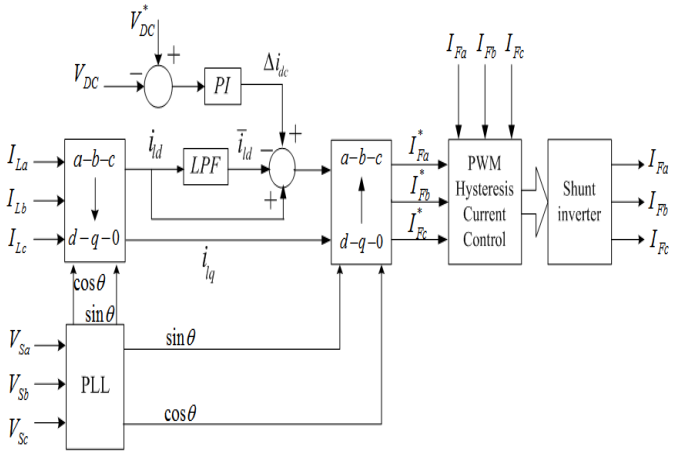

Figure 3: SRF control block diagram for shunt active filter [19]

It is observed that the unbalanced load currents generate a different harmonic spectrum in the DC reference frame, and low order harmonic components appear in the reference signal. In order to separate these unwanted low frequency current components, the cut-off frequency of the low pass filter must be reduced.One of the important characteristics of this algorithm is that the reference signals are directly derived from the load current without the need of source voltages. This shows that the SRF control is not affected by the voltage unbalance or distortion, which is the case with other conventional techniques like instantaneous p-q theory. Thus SRF control has greater compensation robustness and superior performance than p-q control.

Hysteresis current control is used in the simulation for the shunt part of UPQC. In hysteresis control, as shown in Figure 4 error signal, e(t) is used to control theswitches in an inverter. This error is the difference between the desired current,

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$I_F^*(t)$andthe current being injected by the inverter, $I_F(t)$. When the error reaches an upper limit, thecurrent is forced to decrease and when the error reaches a lower limit the current is forced toincrease. The minimum and maximum values of the error signal are e_{min} and e_{max}respectively. The range of the error signal, $e_{max} - e_{min}$called hysteresis band, directly controls the amount of ripplein the output current from the inverter. The hysteresis limits, e_{min} and e_{max} relate directly to an offset from the reference signal and are referred to as the lower hysteresis limit and the upper hysteresis limit. The current is forced to stay within these limits even as the reference current changes.

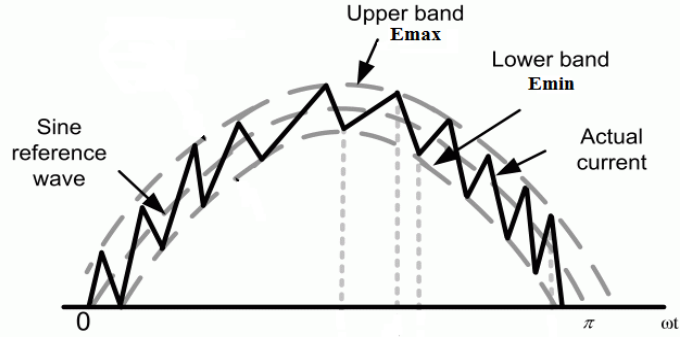

Figure 4: Hysteresis band control

Control of series APFs of both feeders:

The series APFs of MC-UPQC are controlled to inject the appropriate voltage betweenthe point of common coupling (PCC) and loads, such that the load voltages become balanced,distortion free and have the desired magnitude. Theoretically the injected voltages can be ofarbitrary magnitude and angle. However the power flow and device rating are important issues that must be considered while determining the magnitude and angle ofinjected voltage. There are two models for a UPQC—quadrature compensation (UPQC-Q) and in-phase compensation (UPQC-P).

In the quadrature compensation scheme, the injected voltage by the series-APF maintains a quadrature advance relationship with the supply current so that no real power is consumed by the series APF at steady state. This is a significant advantage when UPQC mitigates sag conditions. The series APF also shares the volt-ampere reactive (VAR) of the load along with the shunt APF, reducing the power rating of the shunt APF.Figure 5 shows the phasor diagram of this scheme under a typical load power factor condition with and without voltage sag. When the bus voltage is at the desired value (U_L=U_t=U_o), the series-injected voltage (U_{sf}) is zero (see Figure 5(a)). The shunt APF injects the reactive component of load current, resulting in unity input power factor. Furthermore, the shunt APF compensates not only for the reactive component, but also for the harmonic components of the load current. For sag compensation in this model, the quadrature series voltage injection is needed as shown in Figure 5 (b). The shunt APF injects I_c in such a way that the active power requirement of the load is only drawn from the utility which again results in a unity input power factor.

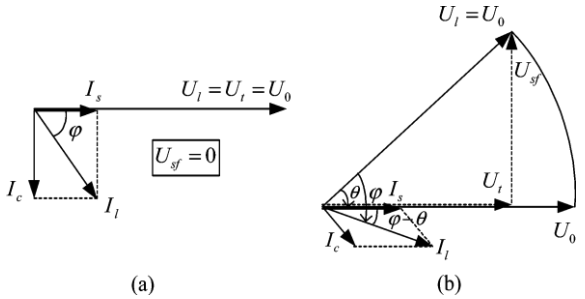

Figure 5: Phasor diagram of quadrature compensation. (a) Without voltage sag and (b) With voltage sag [18]

In an in-phase compensation scheme, in general the injected voltage is in phase with the supply voltagewhen the supply is balanced. Therefore, the series inverter would consume most of the activepower. By virtue of in phase injection, UPQC-P will mitigate voltage sag conditions byminimum injected voltage.The phasor diagram in Figure 6 [19] explains the operation of UPQC-P at thefundamental frequency. When the system voltage and current are in phase due to the action ofthe shunt compensator, the series converter handles purely active power. As seen from Figure 6, the shunt

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inverters current increases when there is supply voltage sag, as the seriesinverter consumes active power through the shunt inverter. When the supply sag is created,the series inverter of the UPQC-P should compensate for the fall in voltage to maintain theload voltage to its specified value. The injected voltage being in phase with the supplyvoltage, the supply current and injected voltages are also in phase with each other. Hence, theseries inverter handles only active power. The series inverter delivers this additional activepower by drawing the same from the DC link of the UPQC-P. Therefore, it acts as an activeload to the shunt inverter. As seen from the phasor diagram, I_{C2} has the same reactive component as $I_{C1}$and an additional active component.

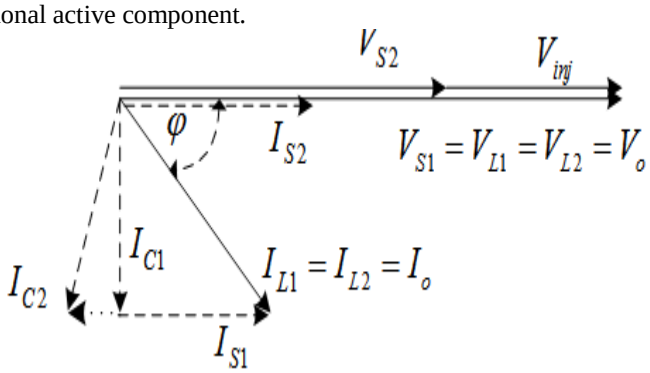

Figure 6: Phasor diagram for UPQC-P

A comparison between in-phase (UPQC-P) and quadrature (UPQC-Q) models is made for different sag conditions and load power factors in [20]. It is shown that the power rating of the shunt APF in the UPQC-Q model is lower than that of the UPQC-P, and the power rating of the series APF in the UPQC-P model is lower than that of the UPQC-Q for a power factor of less than or equal to 0.9. It is also shown that the total power rating of UPQC-Q is lower than that of UPQC-P where the VAR demand of the load is high. UPQC-P has a lower power rating of series inverter and can also be used for voltage swell condition. Therefore a UPQC-P is more advantageous than UPQC- Q and hence UPQC-P is used for both the series inverters in the simulation of MC-UPQC.

Figure 7shows the block diagram of UPQC-P control scheme. The desired value ofload voltage in d-axis and q-axis is compared with the load voltage and the result isconsidered as the reference signal. This control further contains a feed-forward voltage loopfollowed by a PWM voltage control.

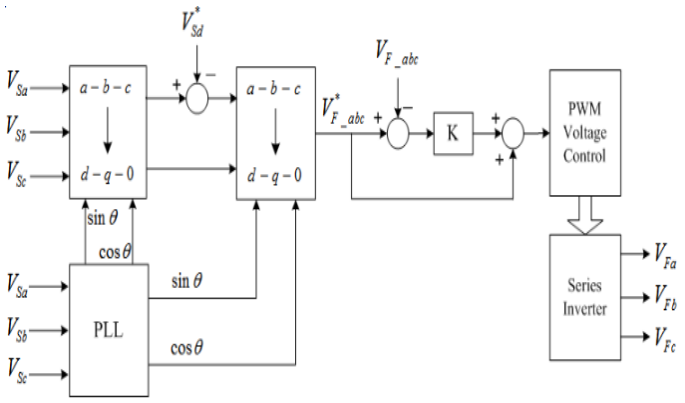

Figure 7: Control block diagram of UPQC-P for series inverter of UPQC [19]

Voltage Control of DC Bus:

For a voltage source inverter, the DC voltage needs to be maintained at a certain levelto ensure the DC-AC power transfer. Because of the switching and other power losses insideUPQC, the voltage level of the dc capacitor will be reduced even in the steady state, if it isnot compensated. Thus, the DC link voltage control unit is meant to keep the average DC busvoltage constant and equal to a given reference value. The DC link voltage control isachieved by adjusting the small amount of real power absorbed by the shunt inverter. Thisreal power is adjusted by changing the

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amplitude of the fundamental component of thereference current. The AC source provides some active current to recharge the DC capacitor.Thus, in addition to reactive and harmonic components, the reference current of the shuntactive filter has to contain some amount of active current as compensating current. This active compensating current flowing through the shunt active filter regulates the DC capacitorvoltage. Control of shunt active filter along with the modification for regulating the voltage ofDC link capacitor is shown inFigure 3.

Usually a PI controller is used for determining the magnitude of this compensating current from the error between the average voltage across the DC capacitor and the reference voltage. But due to its fixed proportional gain (K_p) and integral gain (K_i), the performance of the PI controllers are affected by parameter variations, load disturbances etc.

However, instead of the PI controller, a fuzzy logic controller is proposed for processing the DC capacitor average voltage error [21]. The fuzzy controller claims to have the following advantages over the PI controller:

- it does not require an accurate mathematical model,
- can work with imprecise inputs and handle non-linearity,
- it is more robust,
- has fast dynamic response.

But under steady state conditions, PI controller has superior performance as comparedto the fuzzy controller. Hence, a hybrid fuzzy-PI controller has been proposed. The objectiveof the hybrid controller is to utilize best attributes of the PI controller and fuzzy controller toprovide a controller which will produce better response than either PI or fuzzy controller [22]. Fuzzy controller offers a better speed response for large reference input changes (largevoltage error) whereas the PI controller supports steady state accuracy. The superiority ofboth fuzzy and PI controller are integrated together by using a switching function.

Modelling of Hybrid fuzzy-PI Controller:

A hybrid fuzzy-PI controller will have one PI controller and two fuzzy controllers. One of the two fuzzy controllers is used to generate a switching function in order to combine the output of both PI and fuzzy controllers.

PI controller:

In case of PI controller, proportional gain (K_p) and integral gain (K_i) values plays animportant role in voltage regulation. Values of K_p and K_i are chosen by repeated simulationby keeping in mind the following points:

1. Too much increase in proportional gain leads to instability in control system and toomuch reduction decreases the responding speed of control system.
2. Integral gain of controller corrects the steady state error of the voltage control system.Also, too much increase in its value may also leads to instability.

Thus, values of K_p and K_i used in simulation are 0.8 and 25 respectively.

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Fuzzy Controller:

Fuzzy logic (FL) basically deals with reasoning that is approximate rather than fixed and exact. In contrast with traditional logic theory, where binary sets have two-valued logic: true or false, fuzzy logic variables may have a truth value that ranges in degree between 0 and 1. Fuzzy logic has been extended to handle the concept of partial truth, where the truth value may range between completely true and completely false. Furthermore, when linguistic variables are used, these degrees may be managed by specific functions.

Fuzzy logic system provides a convenient way of nonlinear mapping from the input to the output space. By elaborating on the notion of fuzzy sets and fuzzy relations fuzzy logic systems (FLS) can be defined. These are rule-based systems in which an input is first fuzzified (i.e., converted from a crisp number to a fuzzy set) and subsequently processed by an inference engine that retrieves knowledge in the form of fuzzy rules contained in a rule-base. The fuzzy sets computed by the fuzzy inference as the output of each rule are then composed and defuzzified (i.e., converted from a fuzzy set to a crisp number). Implementation of Fuzzy logic controller block is shown below:

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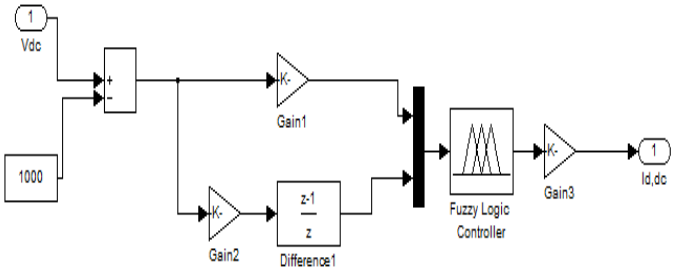

Figure 8: DC link Voltage regulation using Fuzzy logic control in Matlab.

E / CE	PL	PM	PS	ZE	NS	NM	NL
NL	ZE	NS	NM	NL	NL	NL	NL
NM	PS	ZE	NS	NM	NL	NL	NL
NS	PM	PS	ZE	NS	NM	NL	NL
Z	PL	PM	PS	ZE	NS	NM	NL
PS	PL	PL	PM	PS	ZE	NS	NM
PM	PL	PL	PL	PM	PS	ZE	NS
PL	PL	PL	PL	PL	PM	PS	ZE

Table 1: Rule table for Fuzzy DC link Controller.

The general considerations in the design of the controller are:

- If both E and CE are zero, then maintain the present control setting $I_{d,\,DC} = 0$
- If E is not zero but is approaching to the reference value at a satisfactory rate then maintain the present control setting
- If E is increasing, then change the control signal $I_{d,\,DC}$ depending on the magnitude and sign of E and CE to force E towards zero.

Membership functions for the error signal ($V_{DC} - V_{DC,\,ref}$ = E), change in error (de/dt) and output $I_{d,DC}$ is shown inFigure 9, 10 and 11. Symmetrical triangular membership functions are taken, as unsymmetrical membership functions give same steady state response but poor dynamic response as compared to symmetrical membership function.

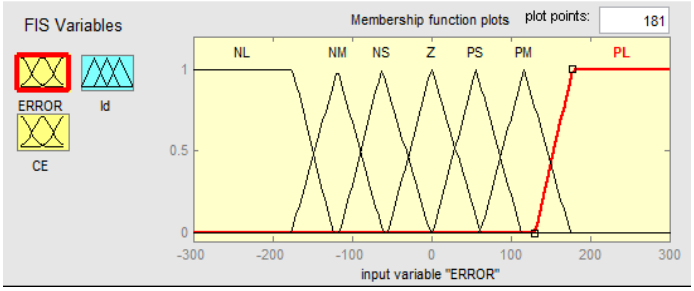

Figure 9: Membership functions for the error signal ($V_{DC} - V_{DC,\,ref}$)

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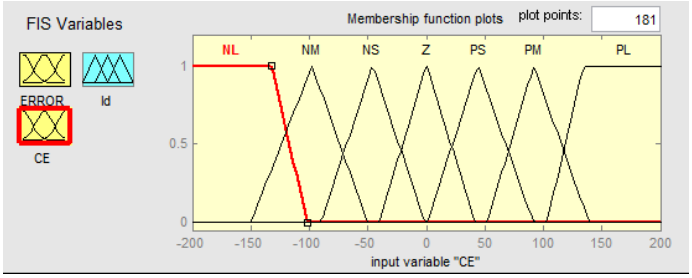

Figure 10: Membership functions for the change in error signal

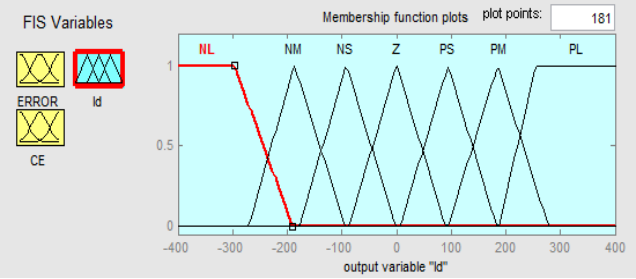

Figure 11: Membership functions for the output signal ($I_{d,\,DC}$).

Fuzzy controller for generating switching functions:

Various types of switching functions can be implemented to combine these two controller outputs to make a hybrid controller and based on the switching functions, the performance of the UPQC will vary. The main focus of the controller design is not only to improve the performance of the controller, but also to reduce the computational burden and thereby to reduce the algorithm execution time.

The switching function has its own rules for assigning the weights for both the fuzzy and PI controller outputs. The switching function is based on a rule, that during the transient conditions, the output of the fuzzy logic controller has the prominent effect on the output of the hybrid controller and during the steady state conditions, the PI controller has the more prominent effect. The advantages of this switching function are absence of chattering, less computational burden resulting in reduced ripples, and simple yet robust switching algorithm.

The selection between fuzzy and PI controllers is based on set of simple rulesshown in Table 2. Under the dynamic conditions, the weightage given for the fuzzy controller output is more than that of the PI controller output, and under the steady state conditions, the weightage given for the PI controller output is more than that of the fuzzy controller output. The combined weightage is decided by another fuzzy controller. The rule table and membership functions of the fuzzy controller which generates switching function are given below in Table 2 andFigure 122, respectively. Singleton output membership functions are used to generate weights for both the controllers.

ERROR	FUZZY	PI
NL	PS	NM
NM	Z	NS
NS	NS	Z
Z	NM	PS
PS	NS	Z
PM	Z	NS
PL	PS	NM

Table 2: Rule table for switching function of hybrid controller.

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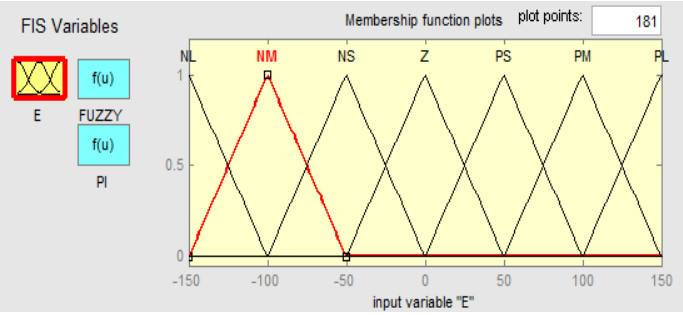

Figure 12: Membership functions for generating switching function of hybrid controller.

The control block diagram of DC link voltage regulation using hybrid fuzzy-PI controller in Matlab is shown in Figure 133.

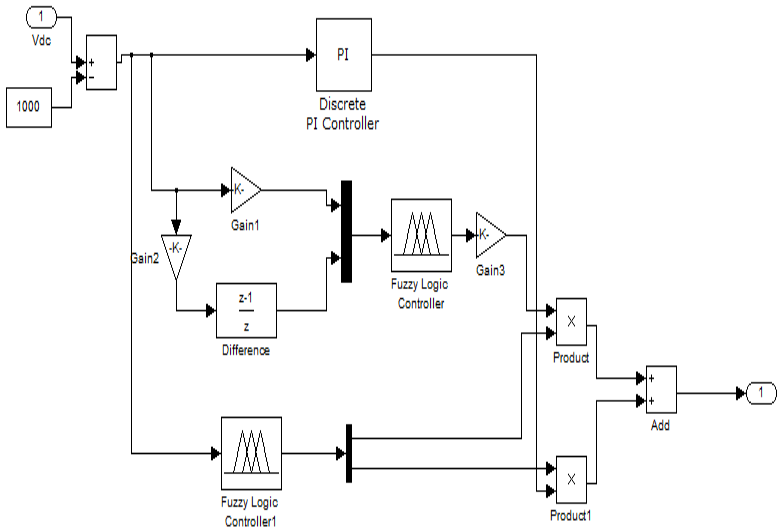

Figure 13: DC link Voltage regulation using Hybrid Fuzzy-PI controller in Matlab.

IV. SIMULATION RESULTS

Two 440V, 50Hz three-phase four-wire 400KVA distribution system with nominal distributed line parameters are modelled in Matlab/Simulink. The supply voltage of both the feeders contains a fifth order harmonic with THD of 20%. A linear RL load of 180KW and 1KVAR and a non-linear load (RL load connected to three-phase diode bridge rectifier, where, R =1Ω, L = 100mH) is connected at load end of feeder 1 and a sensitive critical load of R = 10 Ω and L = 50mH is connected at load end of feeder 2. Table. 5.1 show all the parameters of the system used in the simulation study. Performance of MC-UPQC is evaluated in terms of voltage and current harmonics mitigation, mitigation of voltage sags and swell. Power flow analysis during the operation of UPQC is also presented.

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Parameter/Component	Symbol	Value
Supply Voltage of both feeders	V_s	440V (RMS) L-L
DC link capacitor	C_{DC}	10000 µF
DC link voltage	V_{DC}	1000 V
Shunt filter inductance	L_{sh}	0.5 mH
Series filter inductance	L_{se}	0.61 mH
Series filter capacitance	C_{se}	1µF
Switching frequency of series inverters of both feeders	f_{se}	10KHz
Hysteresis band for shunt inverter	h	+- 0.1A
Linear RL load of feeder 1	$(RL)_{linear1}$	180KW, 1KVAR
Non-linear load (RL load connected to three-phase diode bridge rectifier) of feeder 1	$(RL)_{non\text{-}linear1}$	R =1Ω, L = 100mH
Sensitive critical load of feeder 2	$(RL)_{linear2}$	R =10Ω, L = 50mH

Table 3: Parameters of system used for simulation study.

Case Study 1: In this case study the load as mentioned above inTable 3 of is considered for analysing steady state and dynamic performance of MC-UPQC under voltage sag conditions. MC-UPQC is connected to the distribution system at 0.1 sec of operation. Balanced voltage sag of 0.8pu is considered at 0.2 to 0.3 sec of operation in both feeders. Figure 14and Figure 145 shows the waveforms of both feeders with hybrid fuzzy-PI controller.

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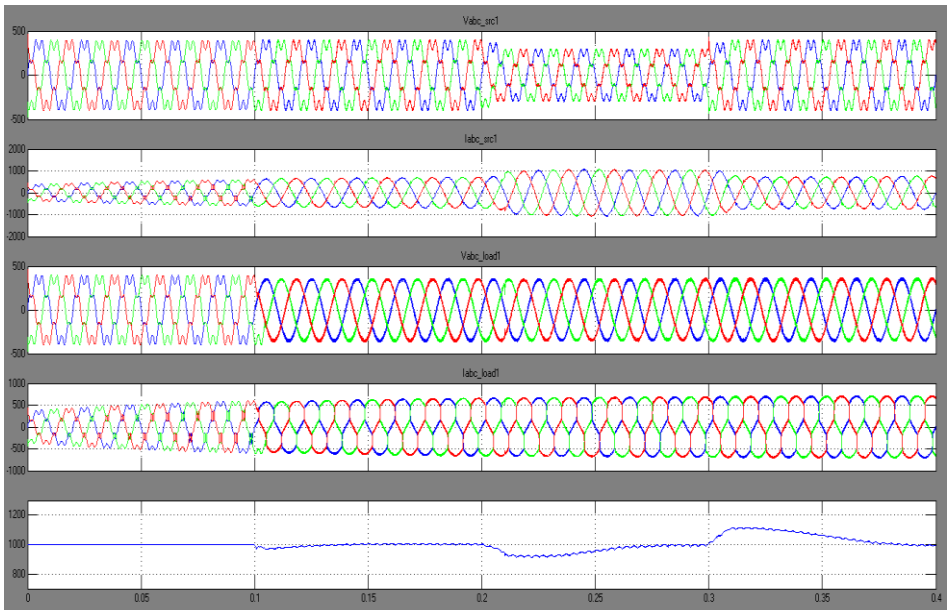

Figure 14: a) source voltage b) source current c) load voltage d) load current and e) dc link capacitor voltage of feeder 1.

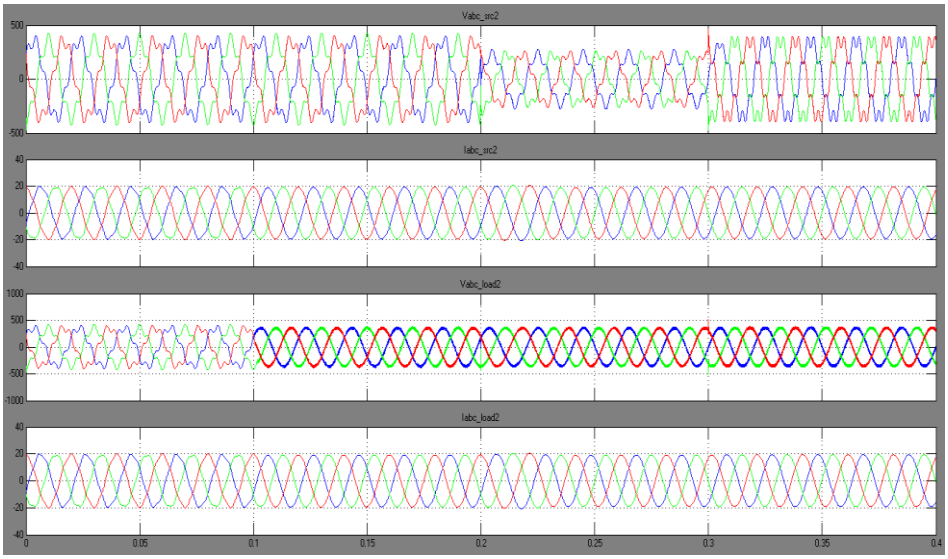

Figure 15: a) source voltage b) source current c) load voltage d) load current of feeder 2.

As shown in above waveforms, the distorted voltages of feeder 1 and feeder 2 are satisfactorily compensated for across the loads L1 and L2 with very good dynamic response. The distorted nonlinear load current is compensated very well, and the THD of the feeder1 current is reduced from 22% to less than 3.32%, while THD of feeder1 load voltage is 3.68%. THD of load voltage of feeder2 reduced from 20% to 4.01%. Also, the DC link capacitor voltage got settled in 0.06secs which shows that DC voltage regulation loop has functioned properly under the voltage sag condition in both feeders.

Case Study 2:

In this case study the load as mentioned in Table 3 is considered for analysing steady state and dynamic performance of MC-UPQC under voltage swell conditions. MC-UPQC is connected to the distribution system at 0.1 sec of operation.

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A balanced voltage swell of 0.35 pu is considered at 0.3 to 0.4 sec in both feeders. Figure 16shows the simulation with hybrid fuzzy-PI controller of feeder 1.

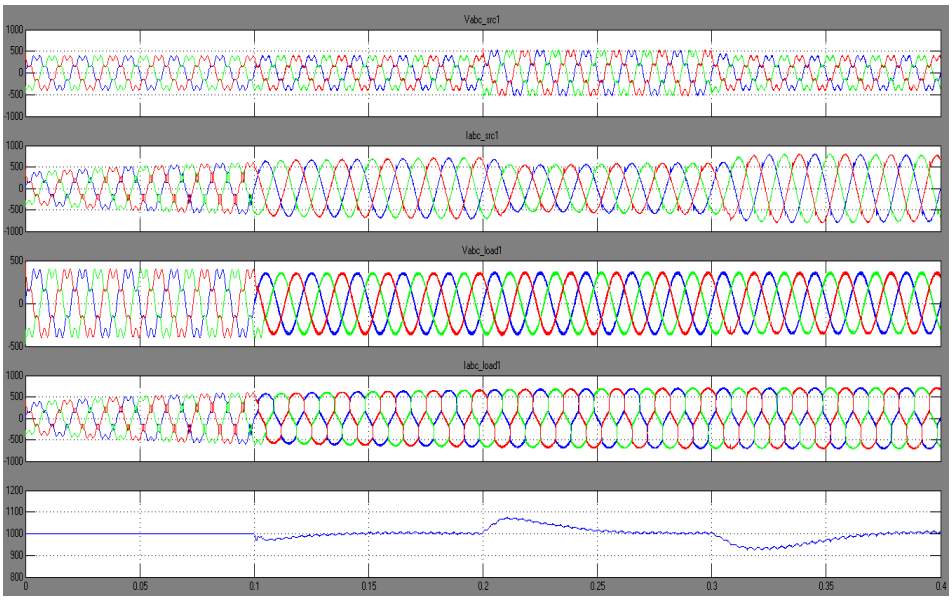

Figure 16: a) source voltage b) source current c) load voltage d) load current and e) dc link capacitor voltage of feeder 1.

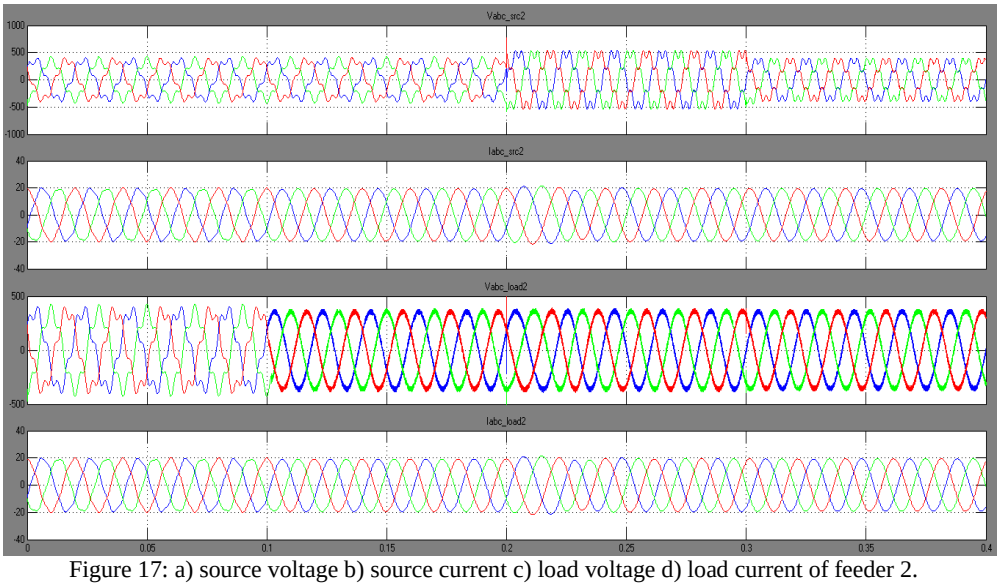

Figure 17: a) source voltage b) source current c) load voltage d) load current of feeder 2.

Figure 16 (b) shows that after connecting MC-UPQC at 0.1 sec of operation, the source current became sinusoidal and in phase with supply voltage of feeder1 having THD of 3.73%. Also, the THD of feeder1 load voltage reduced from 20% to 3.86% and became sinusoidal. The DC link capacitor voltage got settled in 0.05secs which shows that DC voltage regulation loop has functioned properly under the voltage swell condition.Figure 167 shows the simulation with hybrid fuzzy-PI controller of feeder 2. The THD of feeder 2 load voltage got reduced from 20% to 3.99% which shows that MC-UPQC is successful in protecting feeder 2 from voltage swell condition.

Case Study 3:

In this case study the load as mentioned in Table 3 is considered for analysing steady state and dynamic performance of MC-UPQC under fault condition. MC-UPQC is connected to the distribution system at 0.1 sec of operation. In feeder

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1, balanced voltage sag of 0.8pu is considered at 0.2 to 0.3 sec of operation. In feeder 2, a LLLG fault (an interruption) is considered at 0.2 to 0.3 sec of operation.Figure 18shows the simulation with hybrid fuzzy-PI controller of feeder 1

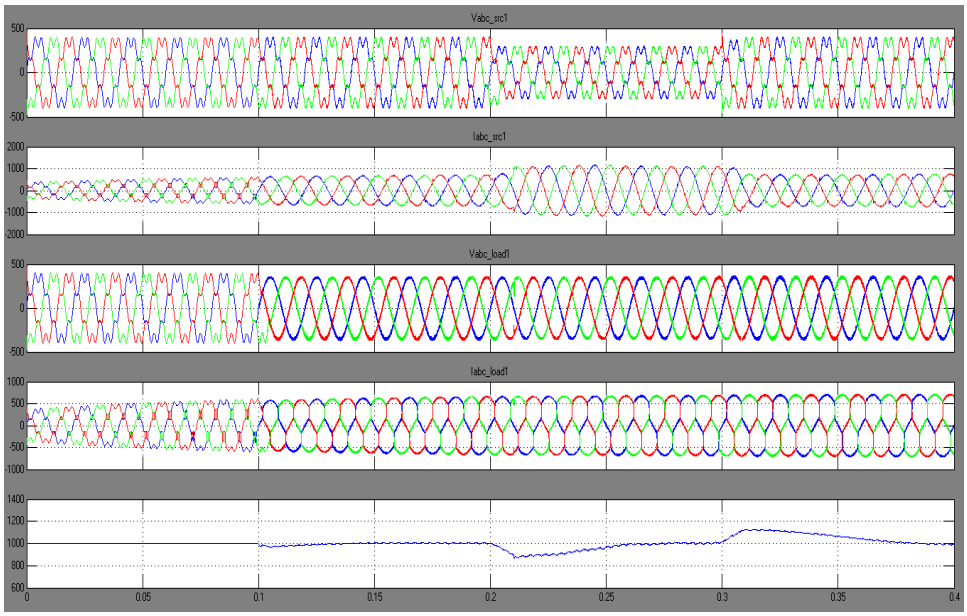

Figure 18: a) source voltage b) source current c) load voltage d) load current e) dc link capacitor voltage of feeder 1.

Figure 18 (b) shows that after connecting MC-UPQC at 0.1 sec of operation, the source current became sinusoidal and in phase with supply voltage of feeder1 having THD of 3.98%. Also, the THD of feeder1 load voltage reduced from 20% to 4.1% and became sinusoidal. The DC link capacitor voltage got settled in 0.06secs which shows that DC voltage regulation loop has functioned properly under the voltage sag condition.

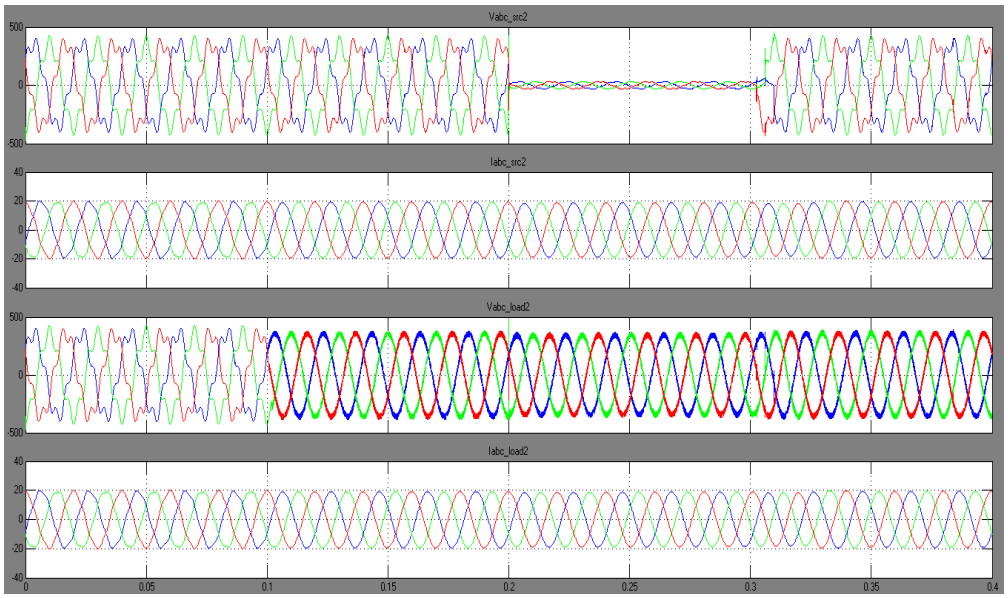

Figure 19: a) source voltage b) source current c) load voltage d) load current

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Figure 189 shows the simulation with hybrid fuzzy-PI controller of feeder 2. The THD of feeder 2 load voltage got reduced from 20% to 4.01% which shows that MC-UPQC is successful in protecting feeder 2 from interruption (supply side LLLG fault) condition.

When a fault occurs in Feeder2 (in any form of L-G, L-L-G, and L-L-L-G faults) as shown above, the voltage across the sensitive/critical load L2 is involved in sag/swell or interruption. This voltage imperfection is compensated for by shunt APF. In this case, the power required by load L2 is supplied through shunt APF and series APF connected to feeder 2. This implies that the power semiconductor switches of APF2 and APF3 must be rated such that total power transfer is possible. This may increase the cost of the device, but the benefit that may be obtained can offset the expense. Thus the sensitive/critical load on Feeder2 is fully protected against distortion, sag/swell, and interruption. Furthermore, the regulated voltage across the sensitive load on Feeder1 can supply several customers who are also protected against distortion, sag/swell, and momentary interruption.

Case Study 4:

In this case study the load as mentioned in in Table 3 is considered for analysing steady state and dynamic performance of MC-UPQC under sudden load changes. MC-UPQC is connected to the distribution system at 0.1 sec of operation. In feeder 1, a non-linear load (RL load connected to three-phase diode bridge rectifier, where, R =2Ω, L = 10mH) is added at 0.2 sec and removed at 0.3 sec of operation. Figure 20 shows the simulation with hybrid fuzzy-PI controller of feeder 1.

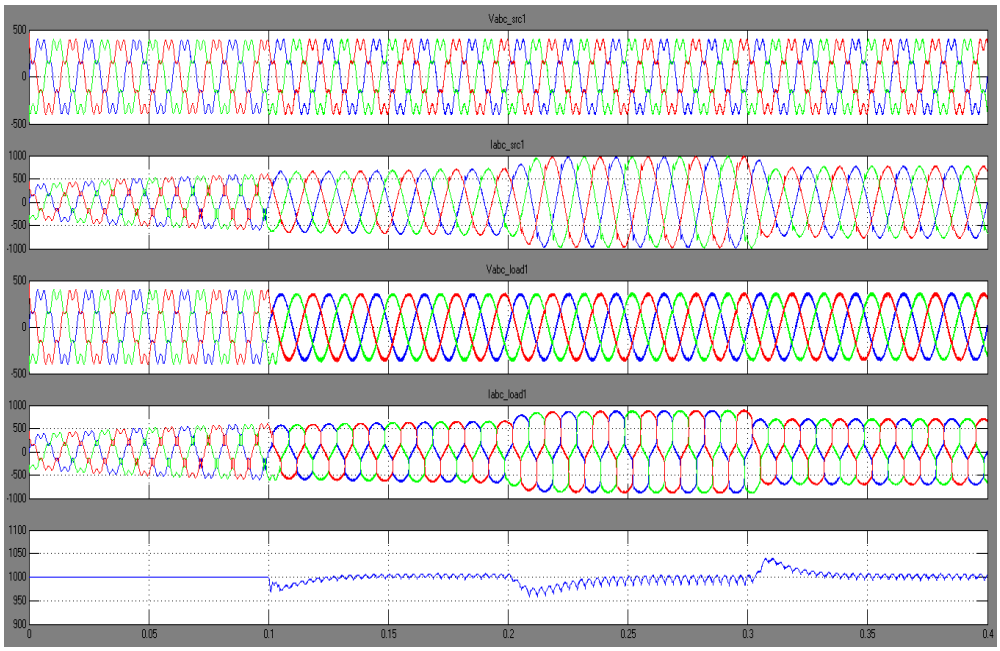

Figure 20: a) source voltage b) source current c) load voltage d) load current e) dc link capacitor voltage of feeder 1

Figure 18 (b) shows that after connecting MC-UPQC at 0.1 sec of operation, the source current became sinusoidal and in phase with supply voltage of feeder1 having THD of 3.78%.Also, the THD of feeder1 load voltage reduced from 20% to 3.9% and became sinusoidal. At 0.2 sec, when there was a sudden increase of load for about 0.1 seconds the feeder1 load voltage remained stable having a THD of 4.01%. The DC link capacitor voltage got settled in 0.05secs which shows that DC voltage regulation loop has functioned properly under the in this condition.

Fig. 5.9 shows the simulation with hybrid fuzzy-PI controller of feeder 2.

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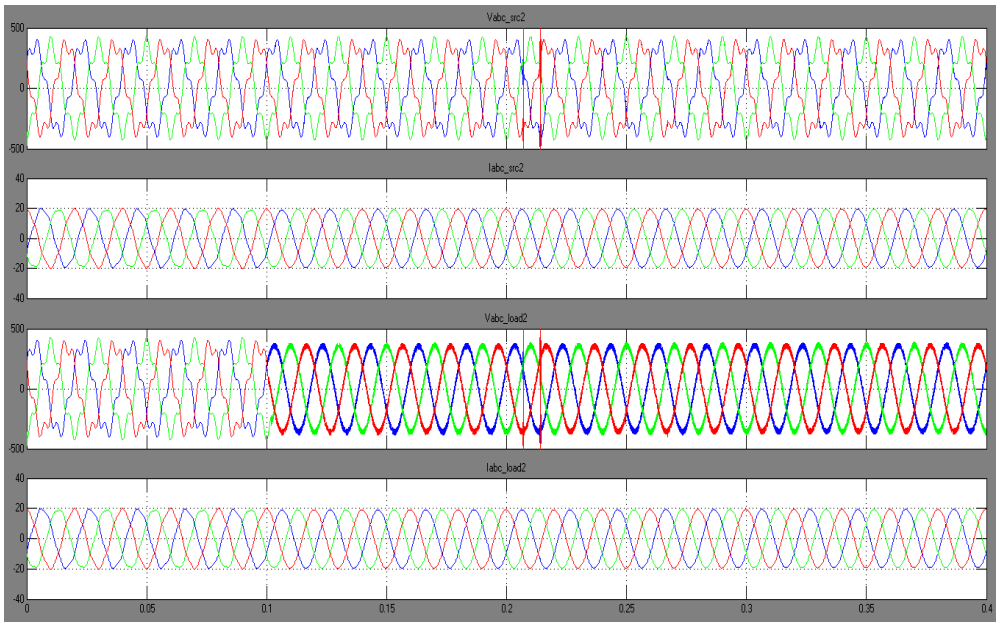

Figure 21: a) source voltage b) source current c) load voltage d) load current

To evaluate the system behaviour during a load change, the nonlinear load L1 is suddenly increased as mentioned above at 0.2 sec. The other load, however, is kept unchanged. It can be seen that as load L1 changes, the load voltages U_{L1} and U_{L2} remain undisturbed. The dc bus voltage is regulated, and the nonlinear load current is compensated.

V. CONCLUSIONS

Conventional UPQC is capable of protecting only one feeder distribution system. In this paper, a novel UPQC configuration for simultaneous compensation of voltage and current in adjacent feeders named multiconverter unified power-quality conditioner (MC-UPQC) has been proposed.Compared to conventional UPQC, MC-UPQC is capable of fully protecting critical and sensitive loads against distortions, sags/swell, and interruption in two-feeder systems. This idea of multiconverter UPQC can be extended to multibus/multifeeder distribution systems simply by adding more series APFs. A two feeder MC-UPQC simulation model in Matlab/Simulink was developed as solution to various power quality problems in distribution systemslike voltage sags, swells, distortion, and sudden load change.The system was applied to adjacent feeders to compensate for supply-voltage and load current imperfections on the main feeder and full compensation of supply voltage imperfections on the other feeder.Simulation results shows that the MC-UPQC was successful for current harmonics such that the supply currents are in phase with line voltages even in dynamic conditions and its THD is within the acceptable limits. Also simulation results show that the compensation performance of MC-UPQC remains unaffected even with unbalanced and highly distorted supply voltage with SRF control.A novel hybrid fuzzy-PI controller was designed which combines the advantages of both PI and fuzzy logic controllers to give better steady state and dynamic responses. The hybrid controller was more robust to parameter changes, non-linear and have fast dynamic response along with superior steady state performance.From the simulation study, it was concluded that the hybrid fuzzy-PI controller has performedvery well and was able to compensate supply voltage and load current imperfections on feeder1 and fully protect the sensitive/critical load on feeder2 against distortion, sag/swell, and interruption.

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BIOGRAPHY

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