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Optimal Approach for Bus Voltage Control with zero distortion

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ABSTRACT: In this paper we Described review method for bus voltage control with zero distortion. It provides detail analysis of how system works for less power consumption. The bus voltage controller must filter this ripple, while regulating the bus voltage efficiently during transients, and must therefore balance a tradeoff between two conflicting constraints, low-harmonic distortion and high bandwidth. This paper analyzes this tradeoff, and proposes a new control method for solving it without using addition hardware. Instead of reducing the distortion by lowering the loop gain, the new controller employs digital FIR filter that samples the bus voltage at an integer multiple of the second harmonic frequency. The filter presents a notch that moves the second harmonic ripple, enabling a design that operates with zero distortion and high bandwidth simultaneously, ands suitable for inverters with small bus capacitors. The proposed controller is tested on a micro inverter prototype with a 300-W photovoltaic panel and a 20-μF bus capacitor

KEYWORDS: Bus capacitor, dc bus, three phase voltage-source inverter (VSI), harmonic distortion, micro inverter, photovoltaic, solar.

I. INTRODUCTION

In comparison to other photovoltaic (PV) architectures, a main advantage of the microinverter architecture is flexibility and modularity. For this reason, these devices have been gaining popularity, especially at small urban installations, where modularity and individual maximum power point (MPP) tracking are an advantage. Each microinverter is connected to a single PV source and directly to the ac line so they are easy to install, and can track the MPP of their adjacent PV sources. In addition, the microinverter architecture is tolerant to failures, because any single failure does not disproportionately reduce the output power of the system [4]. A common topology for microinverter is the two-stage topology shown in Fig. 1. Typically, the first stage tracks the MPP of the source, and boosts the low input voltage, providing suitable high voltage for the second stage. The second stage generates the ac that is injected to the ac line, a current that is typically synchronized to the line voltage. The capacitor between these stages, the bus capacitor, is an internal energy storage device [7].

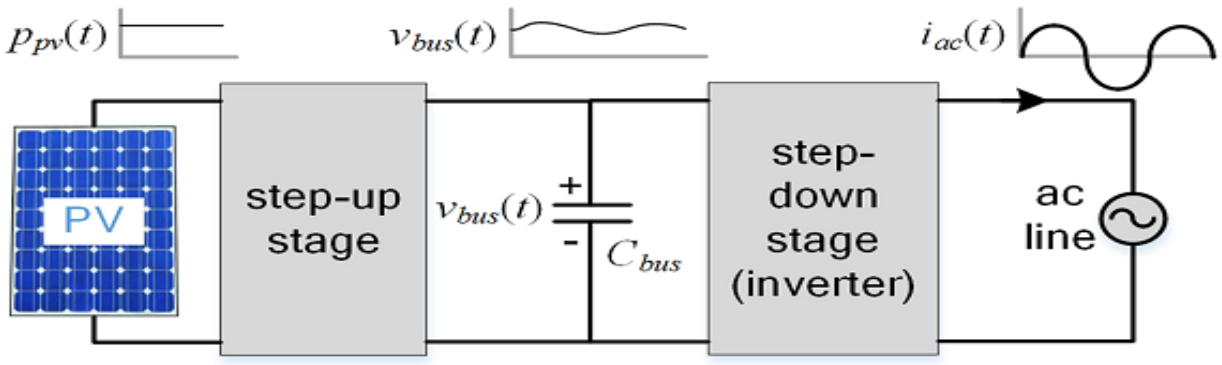

Figure 1:. Two-stage single-phase microinverter with an intermediate high voltage bus capacitor.

The energy and, consequently, the voltage on this capacitor are determined by the difference in power, the constant input power that charges the capacitor, and the pulsating output power that discharges it. Due to this difference, the bus

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voltage includes a harmonic component at twice the ac line frequency, which is a direct outcome of the balance of powers and cannot be mitigated by control. This harmonic component, the second harmonic ripple, may degrade the efficiency and stability of the inverter if not handled appropriately by the inverter control circuitry . raditionally, the bus capacitor has been a high-capacitance low-voltage electrolytic capacitor. However, electrolytic capacitors are known to have limited lifetime and are not compatible with the 20 year or longer lifetime that is desired for modern solar power systems To increase the system lifetime, a high-voltage film or similar capacitor for energy storage is preferred. Because of their increased cost, the size of these capacitors must be minimized The bus capacitor voltage must be regulated within a bounded range that is typically higher than the peak ac voltage but lower than the rated voltage of the bus capacitor and switching devices. This regulation is done by the bus voltage controller, a negative feedback loop that stabilizes the bus voltage against variation in input power, output voltage, and other variations. The loop senses the bus voltage and controls the output current in order to balance the voltage on the bus. It should be quick enough to maintain the bus voltage within acceptable range during transients and, therefore, it is imperative that the loop be designed with sufficient bandwidth. In addition to bandwidth, a second design constraint is harmonic distortion in the output current This distortion must be low to comply with international standards, such as the IEEE 1547 standard which requires that the total harmonic distortion (THD) be lower than 5% at rated power. As a result, the bus voltage loop must comply with two constraints: sufficient bandwidth and low-harmonic distortion, constraints that are often contradicting, particularly when the bus capacitance is low To be cost competitive, new inverters are designed with small bus capacitors , and consequently their bus voltage includes a high second harmonic ripple. With high ripple, however, it is challenging to design a loop that achieves both sufficient bandwidth and low harmonic distortion If the loop has high bandwidth, it responds to changes quickly and can tightly regulate the bus voltage. However, this also introduces variations in the output current that can lead to high and unacceptable distortion on the ac line. To settle the contradicting constraints of distortion and bandwidth, there is need for innovative designs and control methods that can operate with small bus capacitors that cause high second harmonic ripple. A straightforward approach is to use a passive filter to attenuate this ripple. Balog and Krein for example, propose a coupled inductor that presents a notch at the ripple frequency. Another solution is a loop compensator that filters the second harmonic ripple, while maintaining high gain at low frequencies . This type of solution enables low distortion and high bandwidth, but requires a high-order filters with poles and zeroes at low frequencies. In recent years, the majority of research works have attempted to solve this problem by means of active filters While these works differ in details, the main idea is to connect the energy storage elements to the bus through an additional converter that regulates the bus voltage, a topology that can be viewed as a three-port converter This approach solves the problem by essentially eliminating the ripple at the bus voltage, while using a minimal bus capacitor. However, it requires additional hardware, which affects both cost and efficiency. This paper explains the tradeoff between bandwidth and harmonic distortion in the bus voltage loop, and provides a new control method for regulating the bus voltage, a method that is simple, low cost, and does not require additional hardware. The proposed controller uses a digital finite impulse response (FIR) filter that samples the bus voltage at a slow sampling rate that is an integer multiple of the ac line second harmonic frequency. This digital filter achieves what a simple analog feedback cannot; it extracts the low-frequency components of the bus voltage signal, measuring the average bus voltage, while effectively filtering the noise of the second harmonic ripple. The digital filter thus combines three properties that are desired in this application: it operates at a very low sampling frequency and, thus, it is potentially low cost, it attenuates the second harmonic ripple well, and eliminates the distortion due to a notch in its transfer function, and it is quick enough to obtain highly stable dynamic response that maintains the bus voltage well regulated during transients. The paper continues as follows. Section II explains the reasons for distortion in the bus voltage loop, and explains the tradeoff between distortion and bandwidth. Section III introduces the digital controller and FIR filter, and shows how this controller eliminates this tradeoff. Section IV develops a dynamic model of the bus voltage loop and introduces methods for designing an optimized loop compensator. Section V describes tests with an experimental inverter prototype. Section VI summarizes key conclusions.

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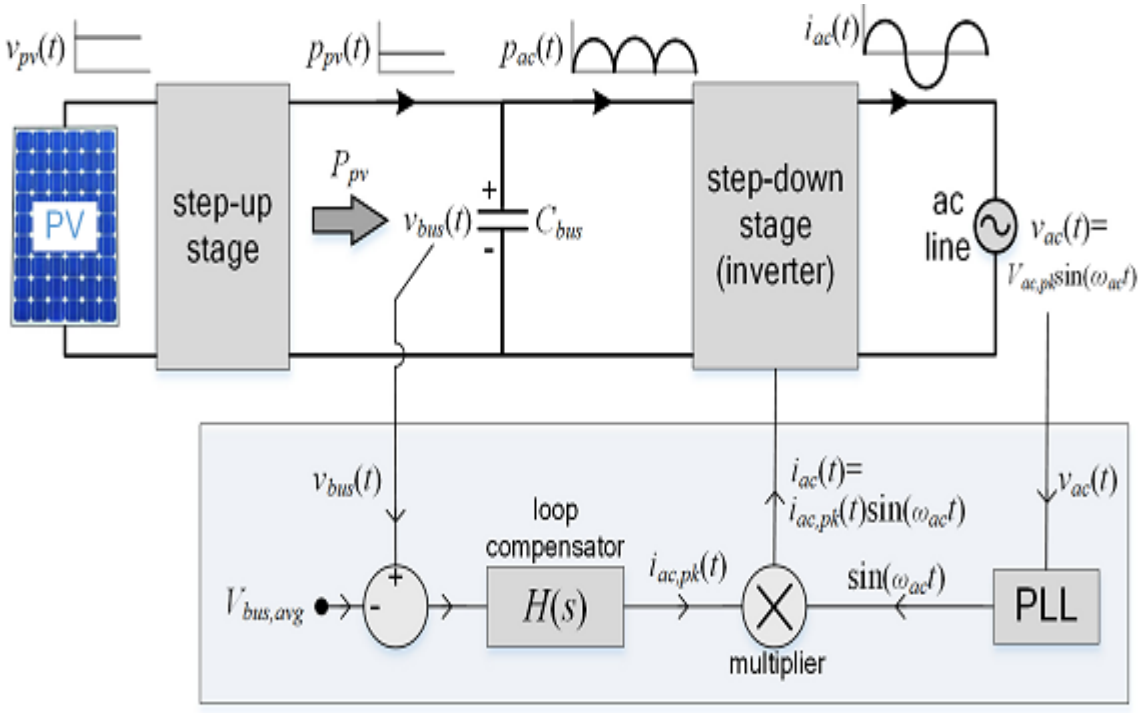

Figure 2: Basic bus voltage feedback loop.

II. METHOD OF POWER LINE DISTORTION

Most adjustable frequency drives operate by using a bridge rectifier to convert the incoming AC voltage to DC voltage (see figure 3). An inverter in the drive then converts the DC voltage into a precise output voltage and frequency to control the speed of the motor.

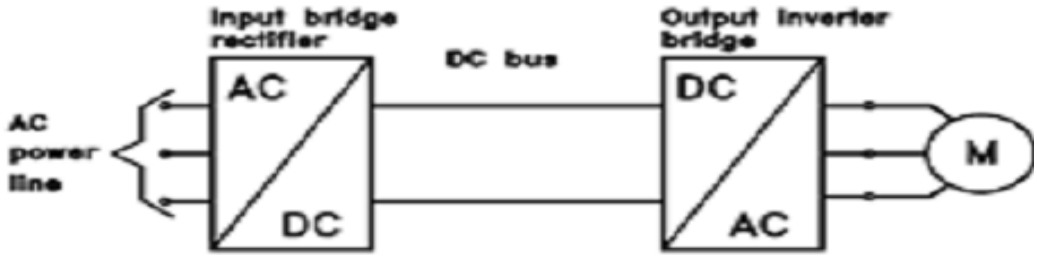

Figure 3: General block diagram of an adjustable frequency drive.

Drives today use a diode bridge rectifier to convert the AC line power into a fixed‑voltage DC bus (see figure 4). A DC

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bus capacitor bank is then used to filter out the AC ripple.

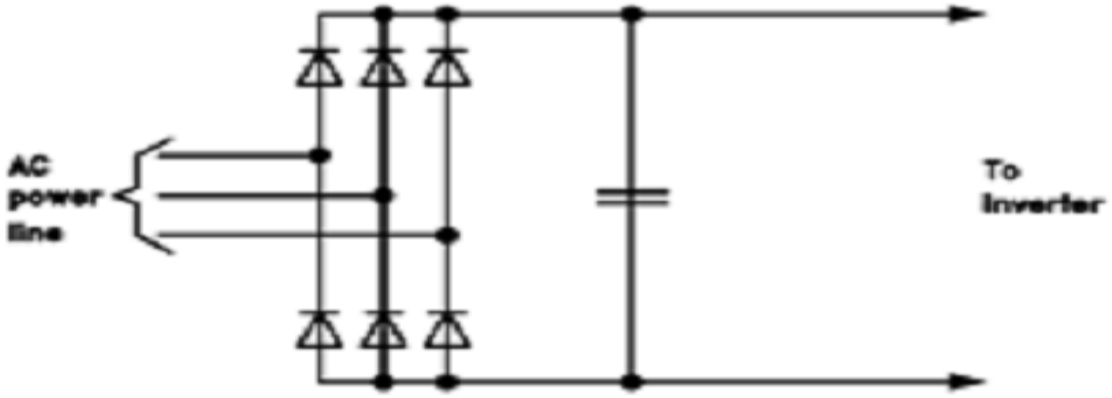

Figure 4: Diode bridge rectifier on a PWM drive.

While this results in a very efficient drive, it can cause disturbances on the AC power line due to the way the drive draws AC current. Current cannot flow from the rectifier into the DC bus until the input voltage is greater than the DC bus voltage.

III. EFFCTS OF POWER LINE DISTORTION

On three phase systems, the actual current to an adjustable frequency drive flows in two pulses that are 60o apart. For line 1, one pulse occurs when the voltage difference between L1 and L2 is at maximum. A second pulse occurs when the voltage difference between L1 and L3 is at maximum. The actual input current to a typical drive, or other similar electronic equipment, is shown in figure 6. These short duration, high peak current pulses can cause a number of problems to the rest of the building's electrical systems.

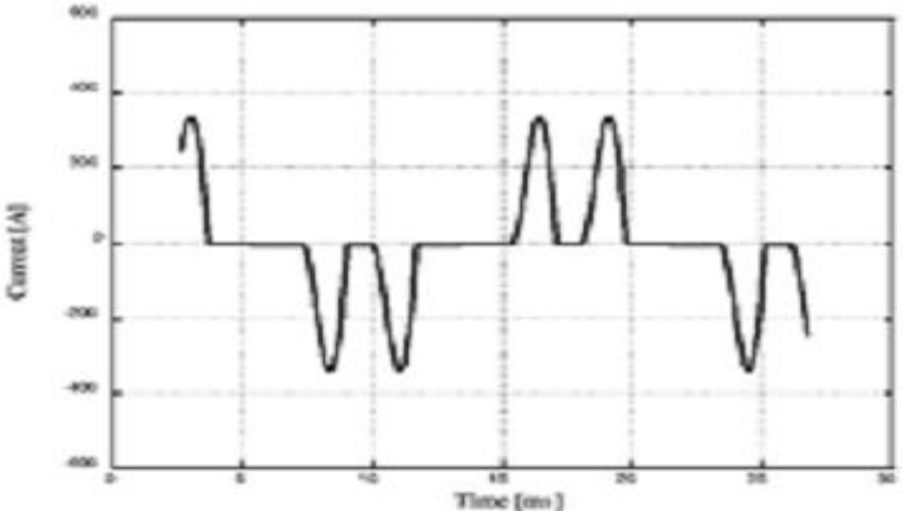

Figure 5. Input current to a basic adjustable frequency drive.

IV DISTORTION WITHH STABILITY ANALYSIS

The objective in this section is to develop a dynamic model of the system, a model that is linear and time invariant and,

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therefore, enables evaluation of dynamic phenomena, such as stability and transients. This model also provides a framework for designing a suitable loop compensator. A main challenge toward a linear model is that the bus voltage loop is not linear and not time invariant, because several key signals include harmonic components that are synchronized to the ac line. For example, the output current is generated by a multiplication of the amplitude signal with a reference sinusoidal signal, an operator that is not time invariant and is modelled by convolution in the frequency domain. Another challenge emerges from the dynamics in the bus capacitor voltage, which are governed by the output power, a signal that is generated by the multiplication of the sinusoidal output current and voltage. Due to these nonlinear operators, a direct analysis of the loop leads to a dynamic model that is highly complex and inefficient. To overcome such complexities, a simpler approach is to model the interactions between signals that are averaged over half a line cycle . This approach is useful because it leads to a simple model that predicts the major dynamic phenomena in the system. Several key signals in the bus voltage loop may be expressed as a sum of a slowly changing average signals, and a harmonic component at 2ωac. For example, a typical spectrum of the bus voltage Vbus(t) is shown in Fig. 8. It includes low frequency components, which correspond to the slowly changing average voltage, and a second harmonic component at 2ωac, which describes the ripple. The second harmonic

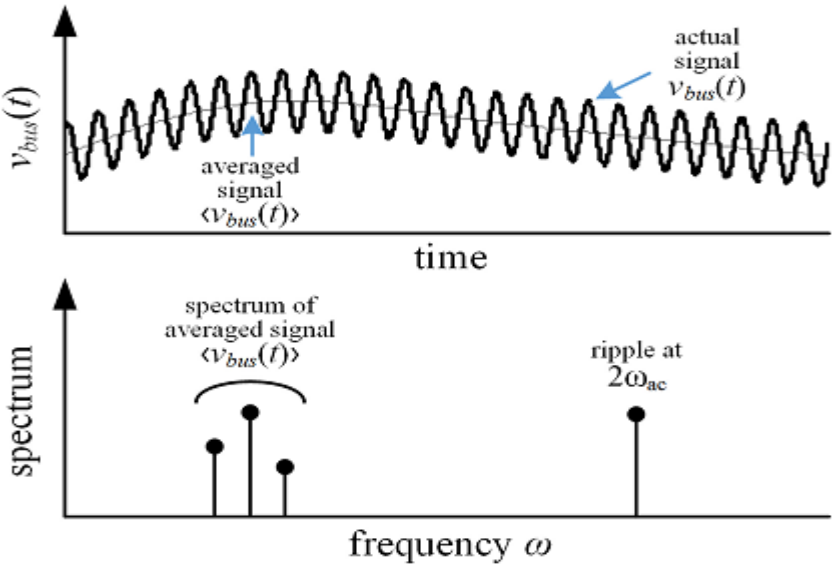

Figure 6:. Spectrum of the bus voltage signal, showing the low-frequency components and the second harmonic ripple.

V. EXPERIMENTAL RESULTS WITH A MICROINVERTER PROTOTYPE

The proposed digital feedback loop was tested on a microinverter prototype whose power topology is shown in Fig. 8. The microinverter is based on a two-stage topology, and includes a step-up stage, which boosts the input PV voltage to the high voltage on the bus capacitor, and a step-down inverter stage, which generates the output ac line current. The prototype is designed for a 300-W PV panel. It interfaces to an output voltage of 220-V rms and a 60-Hz frequency. The bus voltage is regulated to 425 V. The bus capacitor is 20 μF and is rated at 700 V. With this small bus capacitor, the amplitude of the second harmonic ripple is 93 V peak-to-peak at full power. At nominal voltage and 75% power, the efficiency of the inverter system is 95.8%. A summary of the design parameters is shown in Table I. A primary function of the step-up stage is to boost the voltage efficiently, while maintaining the input voltage constant at the PV panel MPP. Because the input PV voltage is constant, and the voltage on the bus capacitor is fluctuating, the voltage gain of the step-up stage is continuously varying.

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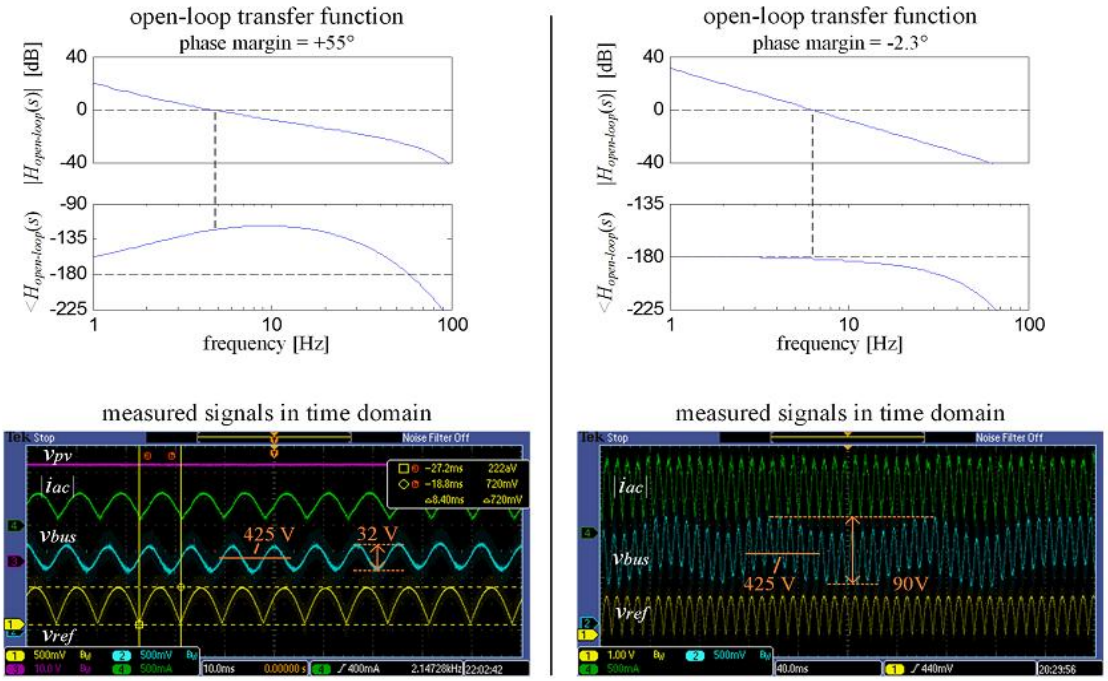

Figure 7:. Dynamics of a stable compensator (left), with phase margin of +55°, and unstable compensator (right), with phase margin of −2.3°. In the scope images: Vpv is the input PV voltage, iac is the (rectified) output ac, Vbus is the bus capacitor voltage, and vref is the current reference signal that is generated by the control loop.

V. CONCLUSION

A conclusion of this analysis is that both the distortion and the bandwidth are affected by one main parameter, the loop gain. To eliminate this tradeoff, this paper proposes a digital controller that operates with low distortion and high bandwidth simultaneously. Instead of reducing the distortion by lowering the loop gain or employing additional hardware for mitigating the ripple, the digital controller uses a FIR filter that samples the bus voltage at a rate that is an integer multiple of the second harmonic frequency, and presents a notch that removes the second harmonic ripple. This enables a simple and low cost design, a design that has high bandwidth, causes negligible distortion in the ac line current, can be implemented with an inexpensive microcontroller, and operates well with a small bus capacitor.

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