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A Novel Multilevel Inverter Topology with Reduced Component count

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ABSTRACT: This paper presents a multilevel inverter that has been conceptualized to reduce component count, particularly for a large number of output levels. It comprises floating input dc sources alternately connected in opposite polarities with one an-other through power switches. Each input dc level appears in the stepped load voltage either individually or in additive combinations with other input levels. This approach results in reduced number of power switches as compared to classical topologies. The working principle of the proposed topology is demonstrated with the help of a single-phase five-level inverter. The topology is investigated through simulations and validated experimentally on a laboratory prototype. An exhaustive comparison of the proposed topology is made against the classical cascaded H-bridge topology.

KEYWORDS: Classical topologies, multilevel inverter (MLI), pulse width modulation (PWM), reduced component count, total harmonic distortion (THD).

I.INTRODUCTION

The last few decades, multilevel voltage-source inverters have emerged as a viable solution for high-power dc-to-ac conversion applications [1]. A multilevel inverter (MLI) is a linkage structure of multiple input dc levels (obtained from dc sources and/or capacitors) and power semiconductor devices to synthesize a staircase waveform. Voltage stresses experienced by the power switches are lower as compared to the overall operating voltage level [2]. In addition, the multilevel waveform has a better harmonic profile as compared to a two-level wave-form obtained from conventional inverters. Other advantages of MLIs are reduced *dv/dt* stress on the load and possibility of fault-tolerant operation [3]. Researchers are also exploring avenues to employ MLIs for low-power applications [4].

The quality of the multilevel waveform is enhanced by increasing the number of levels. However, it inadvertently leads to a large number of power semiconductor devices and accompanying gate driver circuits. This increases system complexity and cost and tends to reduce the system reliability and efficiency. For a high-resolution waveform, therefore, practical considerations necessitate reduction in the number of switches and gate driver circuits [5]. The topologies which have been extensively studied and are commercially available for multilevel voltage output are neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FC) converters [1], [3], [5]–[7]. However, there is a significant increase in the number of power switches, the number of switches conducting simultaneously, and the overall cost of the system with the increase in the number of output levels. Researchers, therefore, continue to focus on reducing the component count in multilevel topologies through various approaches. These approaches can be classified into three categories: topological changes [8]–[12], use of asymmetric sources [13]–[15], and combination of topological changes and asymmetric source configurations.

In this paper, a new topology is proposed in which alternate dc sources are linked in opposite polarities via power switches. This approach significantly lessens the number of power switches needed as compared to the classical topologies. Moreover, for symmetric input dc sources, the proposed topology shows similarity with the CHB topology in two ways: 1) It needs multiple isolated input dc voltages; and 2) input dc voltage levels can be combined into all additive values. Thus, the topology can be used as a utility interface for renewable energy systems where a large number of isolated dc sources are available [2], [7], [9]. It can also be used in medium-voltage drive applications where a phase-shifting transformer with multiple secondary windings is generally employed (mainly for the reduction of line current distortion), thus providing isolated dc sources [6]. The proposed topology may also be appropriate for battery-powered applications (such as electric vehicles and submarine propulsion).

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II. PROPOSED MULTILEVEL TOPOLOGY

In this section, the structure of the proposed topology is introduced, and its working principle is explained with the help of a single-phase five-level inverter. Expressions for out-put voltage, source currents, voltage stresses, etc.,

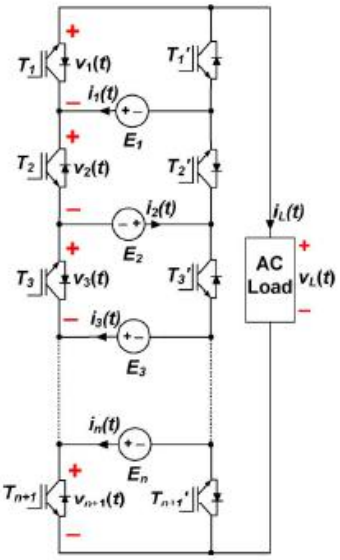

Fig. 1 Generalized single-phase structure of the proposed topology.

A. Generalized Structure

The generalized single-phase structure of the proposed topology is shown in Fig. 1. It has *n* number of isolated input dc sources. The linkage structure is such that the higher potential terminal of the preceding source is connected to the lower potential terminal of the succeeding source and vice versa through power switches. Input sources are designated as E_j (where $j = 1$ to n). Source current from each source is designated as $i_j(t)$. Power switches can be implemented using a transistor device [e.g., MOSFET and insulated-gate bipolar transistor (IGBT)] with an antiparallel diode. In Fig. 1, power switches are illustrated with IGBTs with antiparallel diodes, and

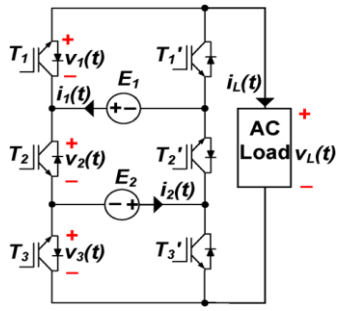

Fig. 2 Single-phase inverter based on the proposed topology with two input sources

complementary pairs are designated as (T_j, T^{0}) (where $j = 1$ to $n + 1$). Various nodal voltages are indicated as $v_j(t)$ (where $j = 1$ to $n + 1$). Load volt-age and load current are designated as $v_L(t)$ and $i_L(t)$, respectively.

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B. Working Principle

The working principle of the proposed topology is described with the help of a single-phase inverter with two input dc sources E_1 and E_2, as shown in Fig. 2. It has three pairs of active switches (T_j, T^0) $(j = 1, 2, 3)$. Since the elements of these pairs are complementary, there are eight valid operating modes. These modes are shown in Fig. 3 and are summarized in Table I along with nodal voltages and source currents. With the use of the operating modes shown in Fig. 3, the load is supplied with five-levels, viz., $\pm V_{dc}$, $\pm 2V_{dc}$, and zero for $E_1 = E_2 = V_{dc}$. With such a symmetric source configuration, modes 3 and 4 become redundant for output level $+V_{dc}$, while modes 6 and 7 become redundant for output level $-V_{dc}$. It is important to note here that, for all positive

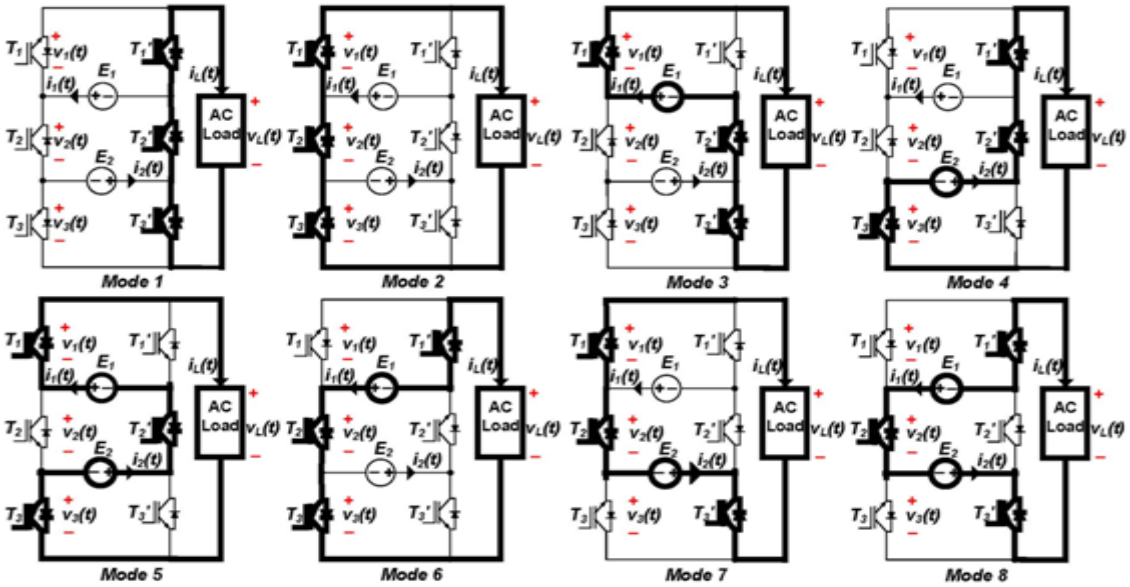

Fig. 3 Valid operating modes for the inverter shown in Fig. 2.

TABLE I

MODES, SWITCHING STATES, NODAL VOLTAGES, AND SOURCE CURRENTS FOR THE PROPOSED TOPOLOGY WITH TWO INPUT SOURCES

Mode	Switch States (1=ON;0=OFF)			Nodal Voltage			Source Current		Output Voltage $v_L(t)$
	T_1	T_2	T_5	$V_1(t)$	$V_2(t)$	$V_5(t)$	$i_L(t)$	$I_2(t)$	
1	0	0	0	$-E_1$	E_1+E_2	$-E_2$	0	0	0
2	1	1	1	0	0	0	0	0	0
5	1	0	0	0	E_1+E_2	$-E_2$	$i_L(t)$	0	E_1
4	0	0	1	$-E_1$	E_1+E_2	0	0	$i_L(t)$	E_2
5	1	0	1	0	E_1+E_2	0	$i_L(t)$	$i_L(t)$	E_1+E_2
6	0	1	1	$-E_1$	0	0	$-i_L(t)$	0	$-E_1$
7	1	1	0	0	0	$-E_2$	0	$-i_L(t)$	$-E_2$
8	0	1	0	$-E_1$	0	$-E_2$	$-i_L(t)$	$-i_L(t)$	$-(E_1+E_2)$

voltage levels and one "zero" level (modes 1, 3, 4, and 5), switch T^0 always conducts, while for all negative voltage levels and another "zero" level (modes 2, 6, 7, and 8), switch T_2 always conducts. Therefore, it is possible to operate these two switches at the fundamental frequency to obtain five output levels. To do so, modes 1, 3 (or 4), and 5 need to be employed for the synthesis of positive levels (including a "zero" level), and modes 2, 6 (or 7),

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and 8 need to be employed for the synthesis of negative voltage levels (including a "zero" level). A procedure to achieve such operation is described in Section IV.

It is also important to mention here that dc source volt-ages have been assumed to be equal in this work. In practice, they might differ (e.g., due to different states of charge of batteries or due to shading of some cells if the sources are coming from a photovoltaic (PV) system). To account for this variation, both hardware-based solutions (e.g., using separate dc–dc converters [8]) and control-algorithm-based solutions (e.g., battery balancing methodology [19]) can be implemented.

III. SWITCHING SCHEME

High-switching-frequency modulation methods like multi-carrier PWM and space vector modulation techniques have been used for MLI modulation control [22], [23]. On the other hand, active harmonic elimination, selective harmonic elimination, and fundamental frequency method are considered as low-switching-frequency methods [24]–[26]. The proposed topology can be modulated with any one of these methods with suitable adaptation. In the present work, the multicarrier PWM scheme is used. In a multicarrier PWM scheme, carrier signals are compared with the reference signal, and the pulses obtained are used for switching of devices corresponding to respective voltage levels. In the proposed topology, one switch may contribute for synthesis of more than one level at output terminals. Moreover, as mentioned in Section II-B, proper utilization of six modes (viz., modes 1, 2, 3, 5, 6, and 8) will lead to fundamental switching of T_2 and T_2 which bear voltage stress of $2V_{dc}$ each as compared to the remaining switches which bear voltage stress of V_{dc} each. Therefore, in this section, a control scheme is described where these modes are utilized to obtain a five-level output. The treatment can, however, be extended for higher level inverter.

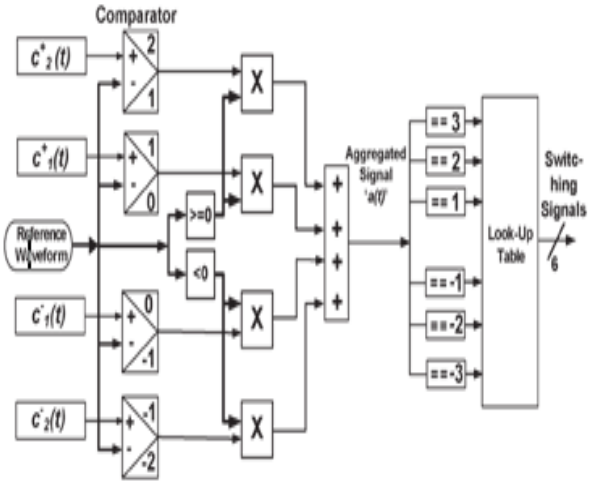

Fig. 4 Proposed control scheme for a five-level inverter

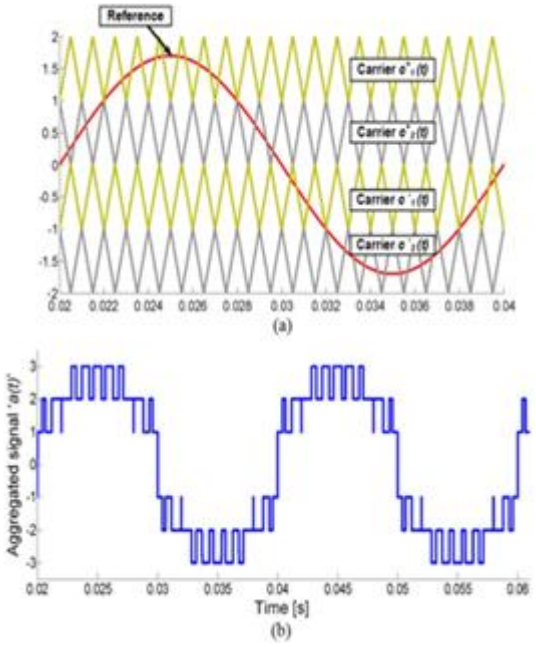

Fig. 5(a) Reference and carrier waveforms for the proposed scheme for a five-level output.
(b) Aggregated signal " $a(t)$."

A. Modulation Scheme

The schematic diagram of the modulation scheme is shown in Fig. 4, and the corresponding waveforms are shown in Fig. 5.Four triangular waveforms of 1-kHz frequency each are used as carriers. Carrier signals are configured in alternate phase opposition disposition [3]. A sinusoidal waveform of 50-Hz frequency is taken as the reference signal. Carrier signals above the zero reference are designated as $c^+(t)$ $(k = 1, 2)$, and those below the zero

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Table II Lookup Table for Five-Level Inverter

Level of Aggregated Signal a(t)'	Mode	Load voltage $v_L(t)$ [V]	Switches in ON state
1	1	0	T_1',T_2',T_5'
2	5	24	T_1, T_2',T_5'
5	5	48	T_1, T_2', T_5
-1	2	0	T_1,T_2,T_5
-2	6	-24	T_1', T_2, T_5
-5	8	-48	T_1',T_2,T_5'

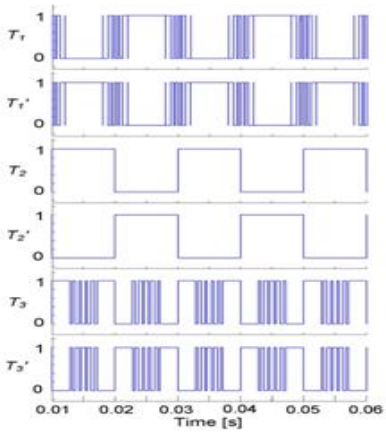

Fig. 6 Switching Pulses for Five-Level Inverter

reference are designated as $c^{-}(t)$ $(k = 1, 2)$. A continuous comparison of the reference with the carriers is executed. If the reference is greater than carrier $c^{+}(t)$, the com-parator gives "k" otherwise, it gives "$k - 1$." If the reference is greater than carrier $c^{-}(t)$, the comparator gives "$-(k - 1)$" otherwise, it gives "$-k$." Signals so obtained are added so as to obtain an aggregated signal $a(t)$. A one-to-one relationship of the levels contained in signal $a(t)$ with corresponding levels in the output waveform is utilized to obtain switching pulses from signal $a(t)$.

IV. SIMULATION RESULTS AND DISCUSSION

A. Five-Level Inverter

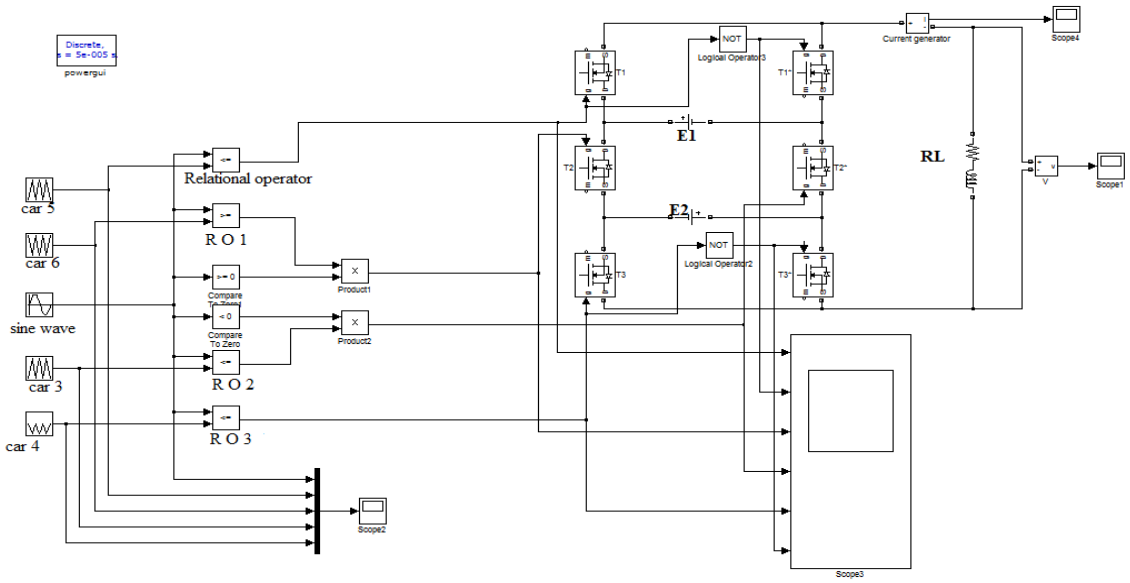

Fig. 7 Simulation Circuit Of Single Phase Inverter With Five Level Output

The figure 7 shows single phase MLI with 5-level output consisting of two dc sources of equal rating and three pair of active switches with 5-level multicarrier PWM control scheme. The circuit of single phase inverter with five level

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output contains 6 switches which are voltage controlled devices the control of switches can be done by using multi carrier sinusoidal pulse width modulation technique as shown in figure 7 The following control circuit four carrier signals & one reference signal the carrier signal of 1kHz frequency & reference signal of 50Hz frequency for soft switching of the T2 &T2'.

Table III Time and output values for five level repeating sequence generator

CARRIER	TIME VALUES	OUTPUT VALUES
3	[0 .0001 .0002 .0003 .0004]	- [1 1.5 2 1.5 1]
4	[0 .0001 .0002 .0003 .0004]	- [1 0.5 0 0.5 1]
5	[0 .0001 .0002 .0003 .0004]	[1 1.5 2 1.5 1]
6	[0 .0001 .0002 .0003 .0004]	[1 0.5 0 0.5 1]

The individual MOSFET is controlled by subjecting the SPWM technique by providing time values and output values to the carrier signals as mentioned in Table III

The parameters of the circuit are
E1 = E2 = 24 V;
L= 2 mH , R= 10Ω ;
MOSFET
Internal diode resistance Rd=0.01Ω, Internal diode inductance = 0H
FET resistance Ron=0.1Ω, snubber resistance is = 0Ω

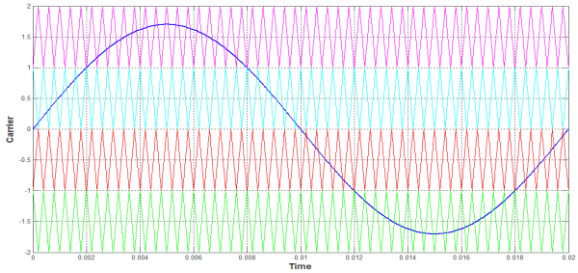

Fig. 8 Reference and carrier waveform of five-level output

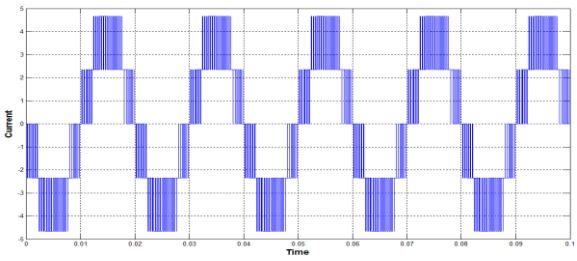

Fig. 9 Five-Level Current Waveform

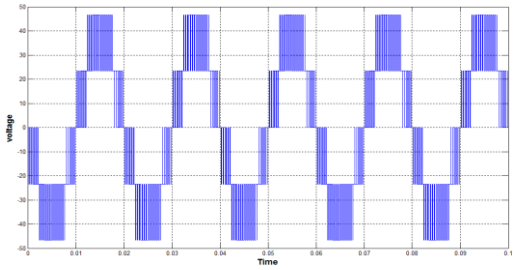

Fig. 10 Five-Level Voltage Waveform

The harmonic spectrum of the five level load voltages is obtained with powergui FFT Analysis Tool. Here for output voltage of 48V the THD obtained is 37.25% and for output current of 4.79A is 37.25%.

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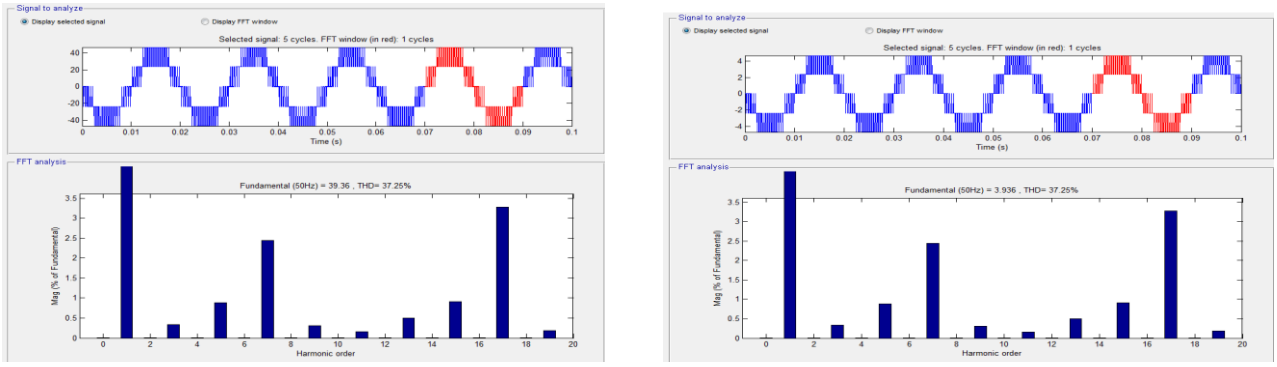

Fig 11 Harmonic Spectrum of Five Level Load Voltage and Current

B. Seven-Level Inverter

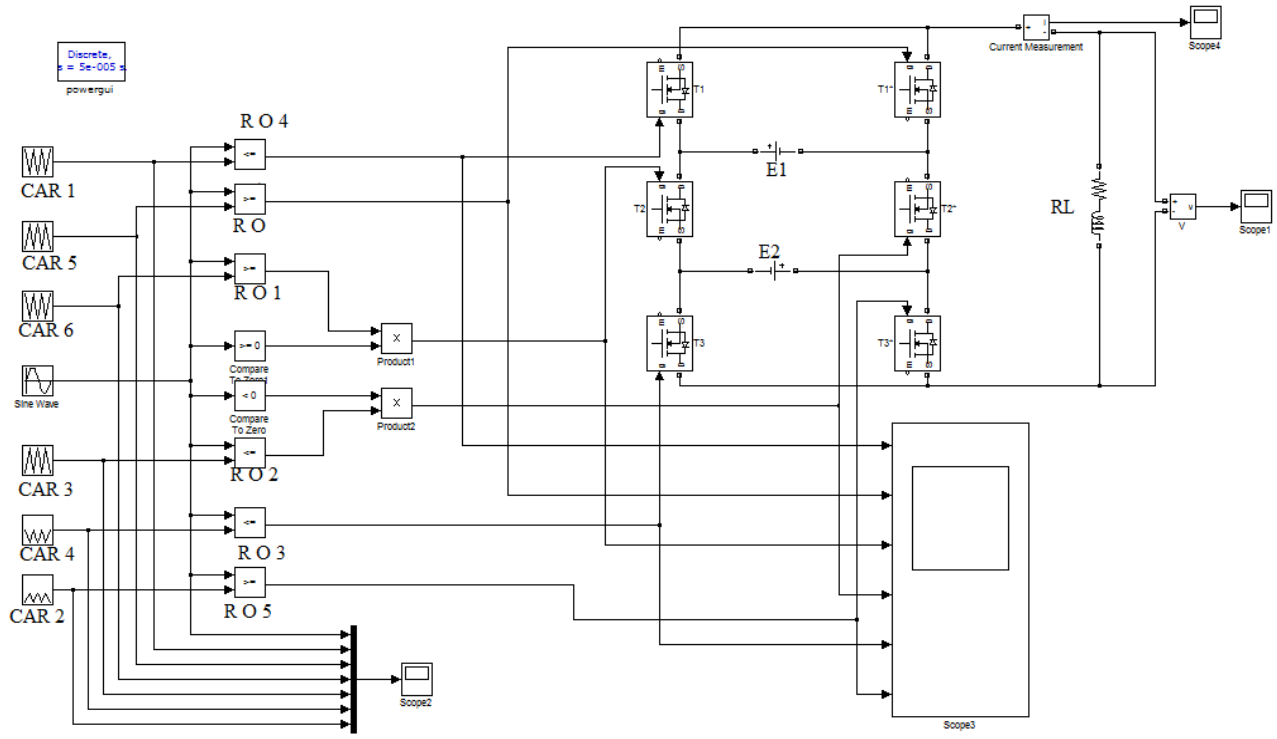

Fig. 12 Simulation Circuit of Single Phase Inverter With Seven Level Output

The figure shows single phase MLI with 7-level output consisting of two dc sources of equal rating and three pair of active switches with 7-level multicarrier PWM control scheme.The circuit of single phase inverter with seven level output contains 6 switches which are voltage controlled devices the control of switches can be done by using multi carrier sinusoidal pulse width modulation technique as shown in figure 5.7.The following control circuit four carrier signals & one reference signal the carrier signal of 1kHz frequency and reference signal of 50Hz frequency for soft switching of the T2 &T2'.

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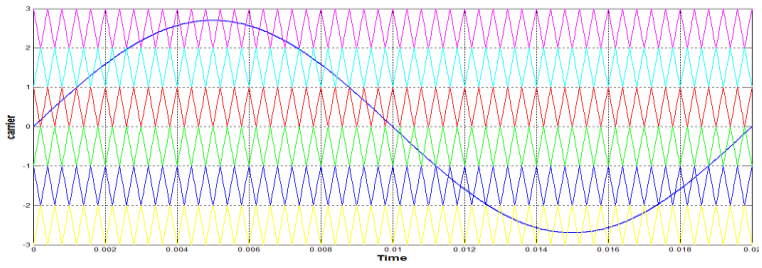

Fig. 13 Reference and carrier waveform for Seven-level output

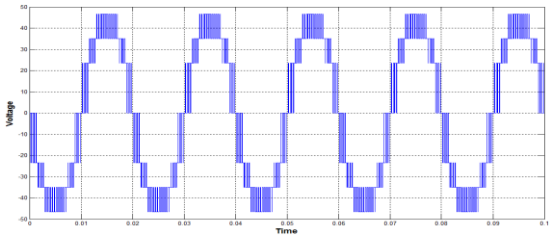

Fig. 14 Seven-level output voltage

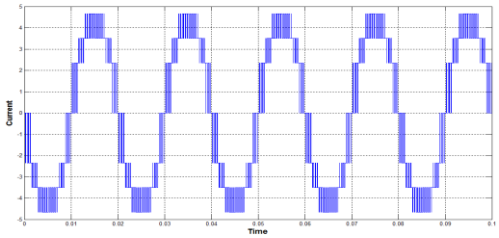

Fig. 15 Seven-Level Current Waveform

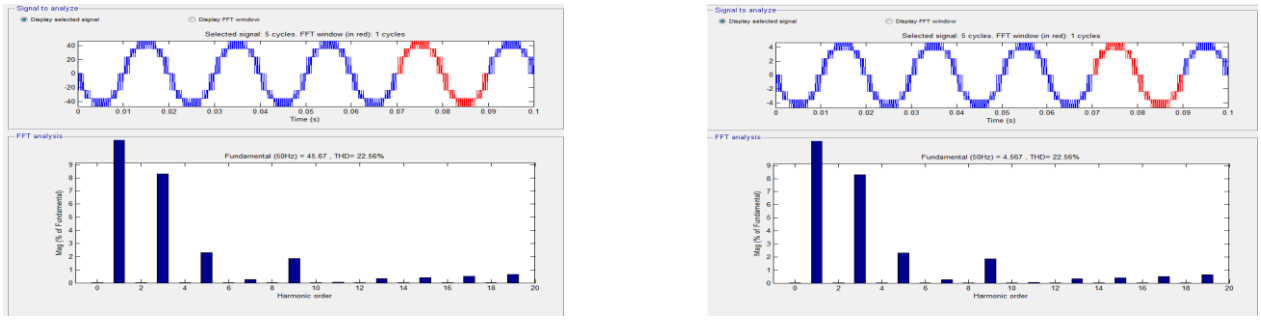

Fig. 16 Harmonic Spectrum Of Seven Level Load Voltage and current

The harmonic spectrum of the five level load voltage is obtained with powergui FFT Analysis Tool. Here for output voltage of 48V the THD obtained is 22.56%& for output current of 4.79A is 22.56%.

V. CONCLUSION

As MLIs are gaining interest, efforts are being directed toward reducing the device count for increased number of output levels. A novel topology for MLIs has been proposed in this project to reduce the device count. The working principle of the proposed topology has been explained, and mathematical formulations corresponding to output voltage, output currents, have been developed. The results of a five-level and seven-level inverter based on the proposed structure have been validated by simulating using MATLAB/SIMULINK. Comparison of the proposed topology with conventional topologies reveals that the proposed topology significantly reduces the number of power switches and associated gate driver circuits.

The figure's shown above represents, fig 7 & 12 represent the simulation circuit's of proposed 5-Level & 7-Level simulation circuit respectively.Fig 8 & 13 represents the referrence & carrier waveforms for triggering of transistors used for the proposed circuit. Fig 9 & 14 & fig 10 & 15 represents the output voltage & current respectively of the proposed level inverters. Fig 11 & 16 shows the THD as 37.25% & 22.56% of proposed 5-level & 7-level inverter respectively.

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