ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

Design and Implementation of 8-Bit SAR ADC with Built-in-Self- Calibration and Digital-Trim Technique

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ABSTRACT: The successive approximation register (SAR) topology is probably the one that has benefited most from CMOS technology evolution, and is now a strong competitor with other architectures as the pipeline, for medium-resolution medium speed ADCs, and the flash, for low-resolution high-speed ADCs. In this system, propose a SAR ADC with a very low-power background calibration technique that continuously nullifies the comparator offset and operates within the supply-voltage range of the ADC. This method allows the comparator to be implemented with small transistors, reducing the power consumption. Furthermore, being a continuous calibration procedure, it is automatically adapting to changes in process, voltage, and temperature (PVT).For operating with a supply voltage as low mV compare with existing methods, close to the transistors threshold voltage V , the ADC employs local voltage boosting for all the MOS switches. To avoid this TH solution to be a strong penalty to the available area/power budget, a voltage-booster (VB) with minimal complexity is employed.

KEYWORDS: Successive Approximation Register (SAR),Analog-to-Digital coverter(ADC),process, voltage, and temperature (PVT),voltage-booster (VB)

I.INTRODUCTION

Successive approximation register analog-to-digital converters (SAR ADCs) are used in medium-resolution and medium-speed applications, such as motor control, battery monitoring, touch-screen control, and other sensor interfaces, requiring low latency, monotonicity, and low quiescent power consumption . A high-voltage input range operation is enabled by directly sampling on the bottom plate of the capacitor array to achieve higher input impedance at a lower operating frequency specifically for industrial motor control applications. In conventional high-performance and high-resolution SAR converters, the fundamental bottleneck in achieving lower integral and differential nonlinearity (INL/DNL) is the mismatches found between the binary weighted capacitors in the capacitive DAC due to process mismatches.

The SAR-ADCs enable direct connection to inputs, minimizing the need for voltage scaling. However,in SAR-ADCs, apart from the mismatches between the capacitors, linear and quadratic voltage coefficients ofcapacitors also dominate the INL. In addition, sampling switches need to maintain constant impedance over the entire input range in order to reduce distortion. Also, these devices are prone to leakage and low speed with pronounced memory effect. Finally, it takes up a huge area to facilitate higher breakdown voltages, thereby increasing parasitics. Therefore, SAR-ADCs typically achieve lower linearity performance than low-voltage SAR ADCs. In this paper, a fully integrated self-calibration and digital trimming algorithm is proposed. The proposed approach does not require any physical trim capacitors on the SAR ADC and performs calibration upon power-up.

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The successive approximation register (SAR) topology isprobably the one that has benefited most from CMOS technologyevolution, and is now a strong competitor with other architectures as the pipeline, for medium-resolution mediumspeed ADCs, and the flash, for low-resolution high-speed ADCs. In most of the implementations, the input signal is sampled directly in the digital-to-analog converter (DAC).

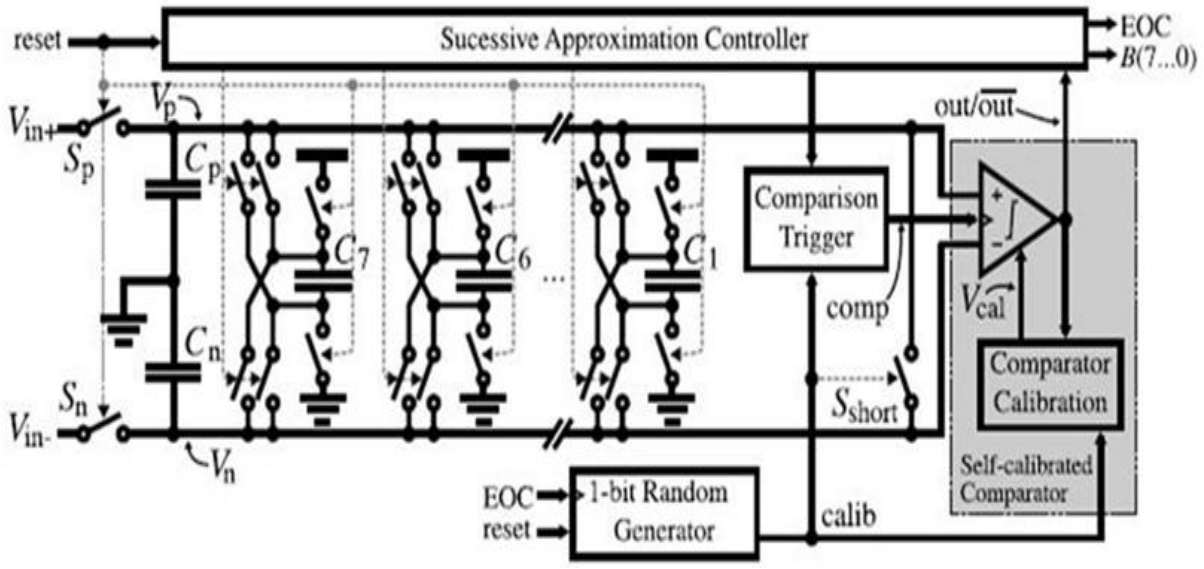

Fig.1. shows the DAC SAR A/D architecture utilizing the proposed self-calibration method in the sampling phase.

The CS-based SAR ADC operates as follows. Initially, a conversion is requested when the reset signal is pulled to 1. Consequently, switches *Sp*and *Sn*are closed and the input signal is tracked by *Cp*and *Cn*, and the DAC capacitors (*C*7...*C*1) are charged to *V*DD. When reset returns to 0, switches *Sp*and *Sn*are opened and the voltage is held on the nodes *Vp*and *Vn*, at the same time as the DAC capacitors hold *V*DD. Then, the successive approximation controller starts operating by initially sending a request to the comparison trigger, which will consequently activate the comparator. Depending on the comparison result *k* (+1 or −1), the controller adds or removes charge from the TH, by closing the corresponding switches in the DAC. This process is repeated for all the bits and as the difference between *Vp*and *Vn*is reduced toward zero, the comparison results are stored by the controller. They will be used to generate the ADC output and the end-of-conversion is close to zero. The process is depicted through the waveforms.

II.CIRCUIT DESCRIPTION

The proposedDAC SAR A/D architecture utilizing the proposed self-calibration method in the sampling phase is shown in Fig.1. uses a memory for storing the errors occurring in each capacitor of the main arrayand corrects it through an extra error correction trim DAC array . The conventional SAR ADC [comprising track-and-hold (TH), binary-weighted capacitive DAC, and successive approximation logic and comparator] is complemented with a comparator trigger, a comparator calibration block, and a random binary generator. The calibration block feeds the comparator with the calibration voltage *V*cal, which controls the comparator offset. These two blocks compose the self-calibrated comparator.

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A. CONVENTIONAL SAR A/D CONVERTERS

An analog to digital converter converts an original input analog signal into an N-bit equivalent output digital codes. A conventional N-bit SAR A/D converter in particular takes N clock cycles for one full complete conversion process. This A/D converter consists of a sample-and-hold (S/H) circuit, a comparator, a digital-to-analog converter
(DAC) and a digital logic. The ADC employs a binary-search algorithm that uses the digital logic circuitry to determine the value of each bit in a sequential or successive manner based on the outcome of a comparison between the outputs of the S/H circuit and DAC. Fig. 2 shows a basic block diagram of a conventional binary search SAR A/D converter.

A Successive approximation ADC is a type of Analog-to-Digital converter that converts a continuous analog waveform inton a discrete digital rprsntation via a binary search through all possible levels bfore finally converging upon a digital output for each conversion.

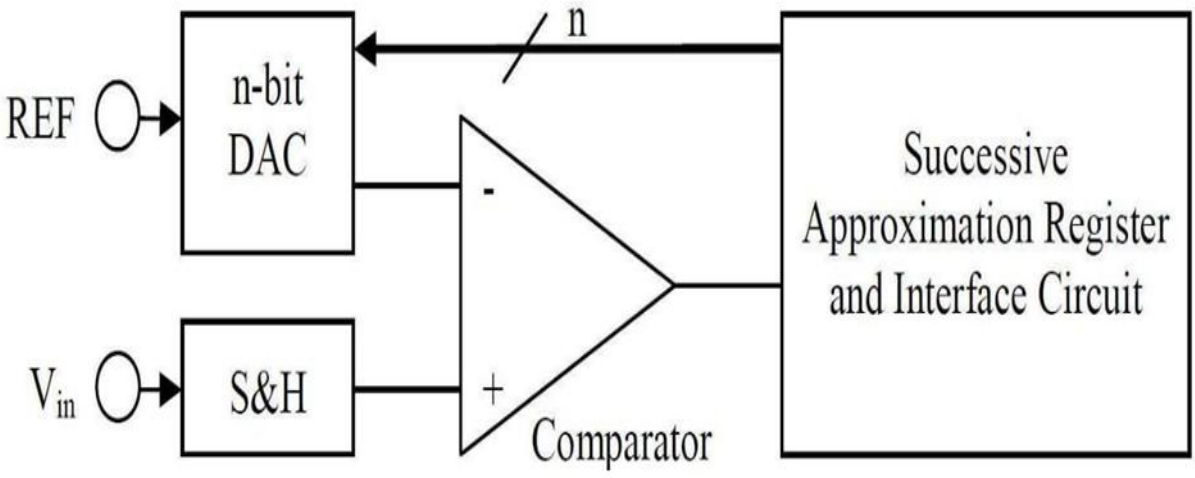

Fig.2. Block Diagram of Conventional SAR A/D Converter

B.SAMPLE AND HOLD CIRCUITRY (SHA)

A Samble and Hold (S&H)circuit is an analog device that samples the voltage of a continuously varying analog signal and holds its value at a constant level for a specified minimum period of time,a typical sample and hold circuit stores electric charge in a capacitor and contains atleast one fast FET switch and atleast one operational amplifier.
Ittakes samples of its analog input signal and holdsthese samples in a memory element. These held samples are used by the A/D converter in each and every clock cycle and converts them into an equivalent digital output codes. The operation of S/H circuit is divided into two modes, sample and hold. During the samplemodethe output of the circuit can either track the input or reset to some fixed value. In Sample and Holdthe hold-mode, the output of the S/H circuit is equal to the input value obtained (sampled)at the end of the sample mode . Although there is an obvious difference between the sampling and tracking, the majority of the circuits used today with the name sample and hold are all track and hold circuits.

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C.DIGITAL –TO- ANALOG CONVERTERS(DAC)

A digital-to-analog converter (DAC) receives a digital code at the input and generates an analog output signals equivalent to the digital code. The analog voltage generated could be anywhere from 0 to *Vref*where *Vref*is the reference voltage. The reference could also be current or charge as well depending upon the architecture. The output voltage of the DAC can be expressed as

$$V_{OUT} = V_{ref}^{*}\left(\sum_{b=0}^{N-1} D_b {}^{*} 2^{-b}\right) \quad \text{----(1)}$$

where*Vref*is the reference voltage, N is the number of bits in this DAC which is also equal to the number of bits of the A/D converter, *Db*is the bthbit of the digital code. The summing term in the equation represents the binaryweighting produced by the division ofthe reference voltage. The accuracy with which the DAC works determine the linearity of this A/D converter.

$$DNL = \frac{Obtained\ Quantization\ Level - ExceptedQuantizationLevel}{Expected\ Quantization\ Level} \text{----(2)}$$

There are many different types of DAC architectures such as voltage scaling, currentscaling, charge scaling etc. All these parallel DAC architectures which produce the output analog voltage in a single clock cycle. There are also many configurations of a serial DAC which takes N clock cycles for a N-bit DAC. But in SAR ADCs where the binary search is carried out, usually parallel DACs are used in order to finish one complete conversion process within N clock cycles.

D.COMPARATORS

A comparator is a module whose function is to compare the analog signals present inthe inputs. Depending on the polarity of the differential input, the logic output would be produced. As it is the case with several types of ADCs, usually one of the comparator's input is connected to a constant potential or reference. When the analog voltage present in the positive input terminal (*VA*) of the comparator is greater than the analog voltage present in the negative input terminal (*VB*), a logic high (*VOH*) output would be produced. When the voltage present in the negative input terminal (*VB*) is greater, then logic low (*VOL*) output would be produced.

Comparators can be classified as open-loop comparators and regenerative (positivefeedback) comparators. The main difference resides on whether or not feedback is appliedto the op amp used. To obtain the benefits offered by both types of comparators, manyconfigurations have been developed that employ a combination of open-loop stages withregenerative stages that uses positive-feedback.An open-loop comparator is an operational amplifier designed to operate with its outputsaturated, close to the supply rails, based on the polarity of the applied differential input.The op-amp does not employ the use of feedback and hence no compensation is requiredto achieve stability in the system. This doesn't pose a serious problem since the linearoperation is of no interest in comparator design. The main advantage of not compensatingthe op amp is that it can be designed to obtain the largest possible bandwidth, therebyimproving its time response.

The main advantage of open-loop comparators is that, if enough gain is provided, theminimum detectable differential input can be very small. It would be reasonable to thinkthat by simply designing the comparator with the largest possible gain, an almost infiniteresolution can be achieved. However, increasing the gain also reduces the bandwidth ofop amps. This means that although the resolution will improve, the time response of thecomparator will degrade. Thus, a trade off between speed and resolution must be made.The absolute maximum resolution of open-loop comparators is limited by input-referrednoise and the offset voltage present in the op amp used.Unlike open-loop comparators, regenerative comparators make use of positivefeedback to realize the comparison between the two signals.They operate with a clockthat divides the operation of the circuit into two phases. During the first phase thecomparator tracks the input and during the second phase the positive

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feedback is enabled.Depending on the polarity of the input, one of the latch's output will go high and theother will go down.

It is a device that compares two voltages or currents and output a digital signal indicating which is larger,it has two terminals V_+ and V_- and on binary digital output V_o

V_o={1 if V_+>V_-
{0 if V_+<V_-

A comparator consist of specialized high-gain differential amplifier,they are commonly used in device that measure and digialized analog signals such as ADC as well as relaxation oscillators.

III.PROPOSED WORK

The SAR-ADCs enable direct connection to HV inputs, minimizing the need for voltage scaling. However, in SAR-ADCs, apart from the mismatches between the capacitors, linear and quadratic voltage coefficients of capacitors also dominate the INL. In addition, HV sampling switches need to maintain constant impedance over the entire input HV range in order to reduce distortion. Also, these HV devices are prone to leakage and low speed with pronounced memory effect. Finally, it takes up a huge area to facilitate higher breakdown voltages, thereby increasing parasitic. Therefore, SAR-ADCs typically achieve lower linearity performance than low-voltage SAR ADCs. In this paper, a fully integrated self-calibration and digital trimming algorithm is proposed. The proposed approach does not require any physical trim capacitors on the SAR ADC and performs calibration upon power-up. The proposed all-digital self-trim algorithm is implemented on a 8-bit SAR ADC with integrated dynamic error correction (DEC) capacitors and the results were verified on a standalone SAR-ADC.

IV.CONCLUSION

In this paper,we analyze SAR ADC with built in self calibration and digital trim technique,A power-on self-calibration and digital-trimming algorithm for a 8-bit HV SAR ADC converter is presented. By using the proposed approach, even a larger mismatch of around 261 LSBs can be corrected to improve yield. The algorithm can be adopted for SAR ADCs with both differential DACs and single-ended ones. This is the only calibration algorithm known in literature to correct for mismatches occurring on any bit capacitance between the P-side and N-side arrays in addition to correcting for mismatches within the binary weighted capacitors inside any array. Also, this algorithm is unique to detect and correct for charge injection-based offset error in self-calibration, and at the same time, it eliminates mismatches occurring between the dynamic error correction capacitors and normal capacitors. This algorithm is also more robust since it finds the errors on capacitors of both P-side and N-side arrays individually and so it could correct a wide range of errors including the mismatch between the arrays. Also, this self-calibration routine could be run on SAR ADCs during each power-on so that the capacitive mismatches that could occur due to environmental conditions, such as temperature and process variations affecting the linearity of the ADCs could be totally eliminated.

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