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On 26th & 27th March 2015

Modelling and Comparison of Two DVR System Topologies using MATLAB

Jimson Varghese[1]

Assistant Professor, Dept. of EEE, Mar Baselios Institute of Technology and Science, Nellimattom, Kerala, India [1]

ABSTRACT: The DVR (Dynamic Voltage Restorer) is a series connected device, which primarily can protect sensitive electric consumers against voltage dips and surges in the low voltage distribution grid. The paper presents a comparison study of two system topologies of DVR for voltage sag and harmonics compensation with an independent energy source or constant dc voltage supply and without using an energy source or taking voltage from the supply itself. The THD values of the output waveform is also taken separately to confirm the comparison study between the two topologies. The two DVR's are modelled and simulated using SIMULINK/MATLAB environment. Time domain simulations are given to verify the operation of the DVR with linear loads.

KEYWORDS: Power Quality, Dynamic Voltage Restorer, Custom Power Devices, Voltage Sag Mitigation.

I.INTRODUCTION

Power quality has been a topic of great interest for decades and several issues have triggered interest in monitoring and improving the power quality. The power disturbances were categorized into four major events: low RMS events, high RMS events, transients and interruptions. More than 26% of the power disturbances came from the low RMS events, while 13% of that came from the high RMS events. The majority of the low RMS events (90%) lasted less than one minute, while 4% lasted more than thirty minutes.

Voltage sags and swells in the medium and low voltage distribution grid are considered to be the most frequent type of power quality problems based on recent power quality studies. Their impact on sensitive loads is severe. The impact ranges from load disruptions to substantial economic losses up to millions of dollars. Different solutions have been developed to protect sensitive loads against such disturbances but the DVR is considered to be the most efficient and effective solution. Its appeal includes lower cost, smaller size and its dynamic response to the disturbance. This paper presents the DVR principles and voltage restoration methods for voltage sags and swells in a distribution system. Simulation results were presented to illustrate and understand the performances of DVR under voltage sags/swells conditions.

The dynamic voltage restorer (DVR) [12], [14] is a series connected device, which by voltage injection can control the load voltage. In the case of a voltage dip the DVR injects the missing voltage and it avoids any tripping of the load. Fig. 1 illustrates the operating principle of a DVR.

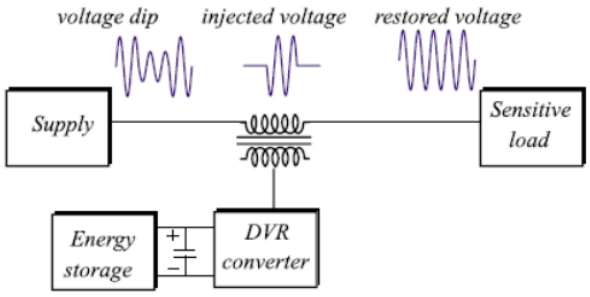

Fig. 1: Operating principle of a DVR.

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Using the 'SimPowerSystems' library controls in MATLAB/SIMULINK an adequate simulation model of DVR is developed. Two system topologies, DVR with no energy storage device is compared with DVR with constant DC voltage energy source. DC-to-DC step up converter has been introduced in DVR without energy storage device. Both the proposed DVR's can compensate deep and long duration voltage sag and compensate steady-state harmonics.

II. CONFIGURATION OF DVR

The configuration of the DVR [2] without separate energy source is shown in Fig. 2. The shunt converter connected to the load side is uncontrolled rectifier, which has uncontrollable dc output voltage V_{dc1}. The uncontrolled rectifier is connected to the load bus through a step down transformer. The dc output voltage of the rectifier Vdc1 is the input voltage of the dc-to-dc step up converter. The output voltage of the step up converter V_{dc2} is the input dc voltage of the VSC in the DVR. Although, with this configuration, the uncontrolled rectifier draws non-linear current, the DVR is able to eliminate all harmonics associated with the load voltage [15]. The load applied is an R - L linear load. In the Fig. 2 if we apply a constant dc voltage to the inverter instead of using the charging rectifier and dc-to-dc step up converter it will give the DVR configuration with separate dc energy source [7], [16] .

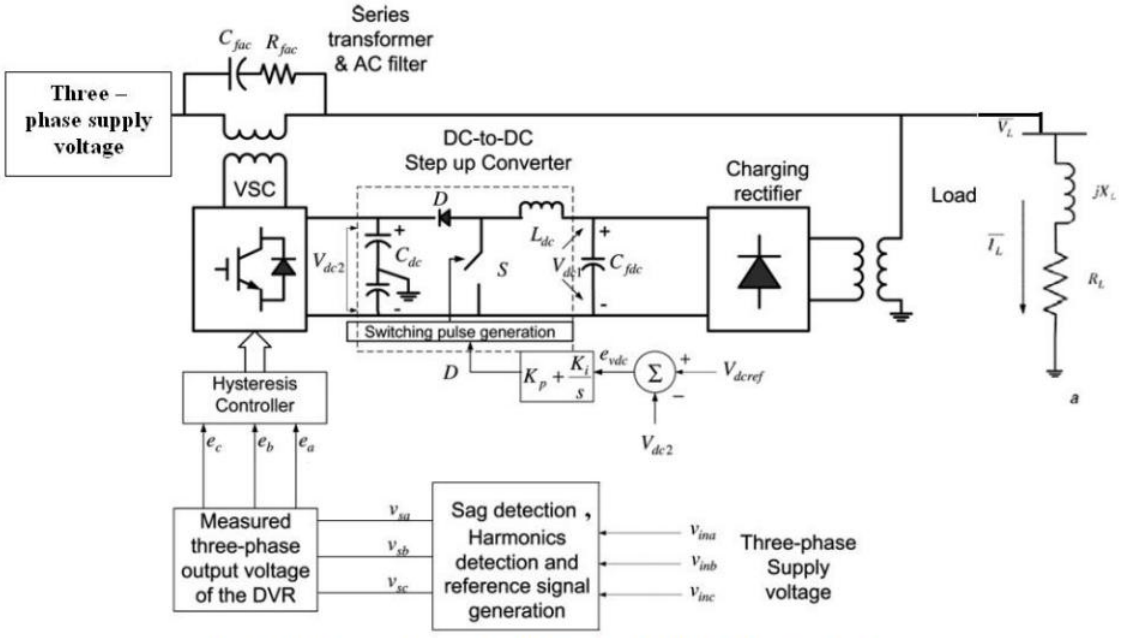

Fig. 2. Schematic diagram of the proposed DVR without energy source.

II.A. DC Voltage Control of DVR

The step up converter controls the duty cycle, D to maintain its dc output voltage V_{dc2} at the reference set value V_{dcref}. This is done by using proportional and integral (PI) controller as shown in Fig. 2. The PI controller compares between V_{dcref} and V_{dc2} to produce the error e_{vdc}. The error e_{vdc} is passed through the PI controller to produce the suitable duty cycle, D which in turns fed into the switching pulse generation block to generate the switching pulses of the MOSFET. Here, the switching frequency of the MOSFET is selected to be 1027Hz [1] .

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II.B. Voltage Sag Detection Scheme

The sag detection method used here is Software Phase Locked Loop (SPLL) system [9], [13]. The SPLL operating principle is based on the concept of voltage tracking where the SPLL tracks the positive sequence of the utility voltage. When voltage sag takes place in a three-phase power system, it causes voltage unbalance by generating negative and zero sequence voltages. The voltage unbalance causes an oscillation error in the measurement of the phase angle.

In Fig. 3, the SPLL output vector V_{SPLL}. The Phase shift between the actual normalised utility voltage vector V_s' and the nominal unity vector V_{SPLL} can be described as:

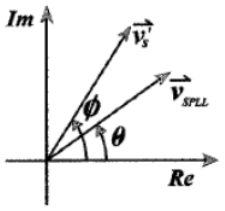

Fig.3. Phase Shift of Vectors

$$\phi - \theta = \arctan\left(V'_{s\beta} / V'_{s\alpha}\right) - \theta \approx \sin(\phi - \theta) = V'_{s\beta}\cos\theta - V'_{s\alpha}\sin\theta \quad (1)$$

This phase shift [11] could be eliminated by using a PI controller or loop filters. Under locked conditions, the argument of the nominal unity vector is equal to the argument of the fundamental positive sequence vector of the utility voltages. The actual implementation of the above idea is shown in Fig. 4 where the instantaneous phase utility and α voltages, V_{sa}, V_{sb}, V_{sc} are sampled and converted into $V_{s\alpha}$ and $V_{s\beta}$

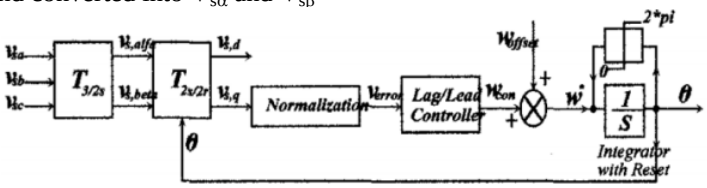

Fig. 4. Block Diagram of Software Phase-Locked Loop (SPLL)

The transformed voltages are converted into Synchronous Rotating Frame (SRF), producing V_{sd} and V_{sq}, by using the output angle of the SPLL.

$$\begin{bmatrix} V_{s\alpha} \\ V_{s\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_{s\alpha} \\ V_{s\beta} \end{bmatrix} \quad (3)$$

In order to simplify the control, V_{sq} is normalized using the following equation.

$$V_{sq} = V_{s\beta}\cos\theta - V_{s\alpha}\sin\theta \quad (4)$$

When the utility voltages are ideal and balanced, the dq components of the utility voltage vector, V_s appear as DC values. Therefore, by regulating V_{sq}, it's possible to track accurately the argument of the positive space vector of utility voltages. Typically, a second order feedback control system is implemented for regulating V_{sq} and filtering the higher order harmonics.

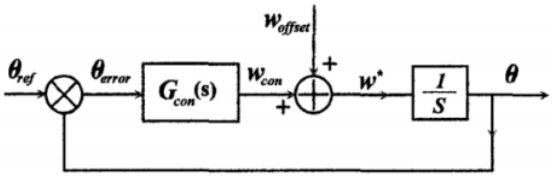

Fig. 5. Simplified Linear Model of SPLL.

In the SRF frame, if the output angle θ is identical to the argument of the positive sequence space vector of the utility voltages, then the phase shift is equal to zero. This results in the dq components of the utility voltage vector V_s to appear as DC values. When the phase shift is small enough, (ϕ-θ) becomes valid. The SPLL can thus be treated as a linear control system shown in Fig.5. If $G_{con}(S)$ is a PI controller or a lag/lead controller, the whole SPLL becomes a second order linear system.

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For the PI controller, $G_{con}(s)$ can be described as $G_{con}(S)= (K_p + K_i /s)$ and the open and closed loop transfer functions of the SPLL [13] are given by:

$$G_{open}(s)=\frac{1}{s}(K_p+K_i/s); G_{close}(s)=\frac{2\xi\varpi_n s+\varpi_n^2}{s^2+2\xi\varpi_n s+\varpi_n^2} \quad (5)$$

$$where, \xi(DampingRatio)=\frac{K_p}{2}.\frac{1}{\sqrt{K_i}}=0.707,$$

$$\varpi_n(NaturalFrequncy)=\sqrt{K_i}=22.36$$

$$and, K_p=31.61, K_i=499.97$$

The proposed experimental SPLL system is shown in the flowchart diagram in Fig.6. The angle and frequency information is used to control the PWM converter applied to a Dynamic Voltage Restorer.

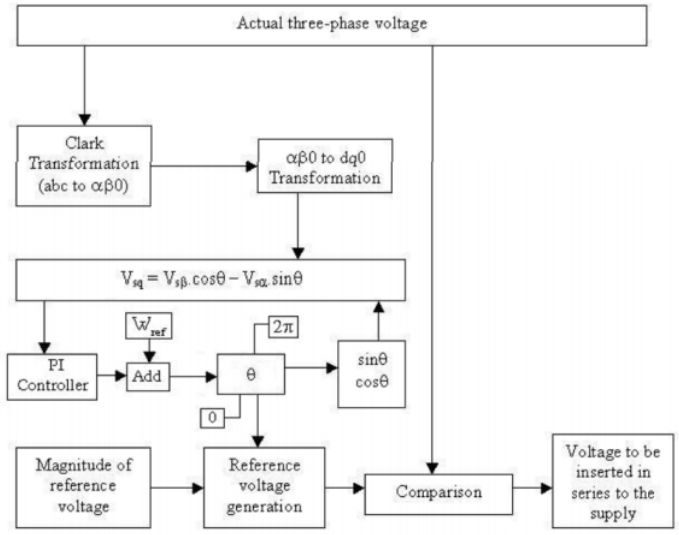

Fig.6. Flowchart showing the working of SPLL

The three-phase instantaneous output voltage (v_{sa}, v_{sb} and v_{sc}) from the voltage sag/swell detection block is the input to the hysteresis controller block.

II.C. Harmonic's Compensation

Harmonic's compensation is done by using a single tuned filter. The signal generation is done by the voltage sag compensation subsystem itself. Here, the filter is used only to eliminate the fifth harmonics. It has the same configuration as the linear load connected to the system [4] .

II.D. AC voltage control of DVR

Conventional two-level hysteresis voltage control, which is one type of non-linear voltage control based on the voltage error, is implemented [5] in the DVR . It consists of a comparison between the output voltage V_0 and the tolerance limits (V_H, V_L) around the reference voltage V_{ref}. While the output voltage V_0 is between upper limit V_H and lower limit V_L, no switching occurs and when the output voltage crosses to pass the upper limit (lower band) the output voltage is decreased (increased). The hysteresis band is given as $h = V_H - V_L$. Here, the hysteresis band is taken as 0.000208pu. The hysteresis controller generates the switching pulses that are fed to the VSC. The generated three-phase voltage of the DVR is injected through a series transformer. As shown in Fig. 2, ac filters (R_{fac} and C_{fac}) are connected across the series transformer to eliminate the switching ripples produced by the VSC.

III. DESIGN OF DVR COMPONENTS

The design of the dc capacitor C_{fdc} of the uncontrolled rectifier, the dc capacitor C_{dc} and the inductor L_{dc} of the dc-to-dc step up converter based on single-phase voltage sag which induces a voltage fluctuation with twice the line frequency of the dc capacitor [6] is discussed. The parameters of the series and shunt transformers are the default parameters of the transformer model in SIMULINK/MATLAB. The voltage sag factor Ksag is defined as

$$\overline{K}_{sag}=\frac{\overline{V}_{ssag}}{\overline{V}_{spre-sag}} \quad (6)$$

where V_{ssag} is the sag load voltage and $V_{spre\text{-}sag}$ is the pre-sag load voltage.

$$D_{sag}=\left|\overline{K}_{sag}\right| \quad (7)$$

The magnitude of the voltage sag factor K_{sag} is equal to the depth of the voltage sag D_{sag}; that is, the power ratings of the series PWM and the shunt uncontrolled (passive) converters in per unit of the load power are given as [10]

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$$S_{shunt} = S_{series} = \left| \frac{1 - \overline{K}_{sag}}{\overline{K}_{sag}} \right| \qquad (8)$$

where S_{shunt} is the pu power rating of the shunt converter and S_{series} is the pu power rating of the series converter.

III.A. Sizing the dc capacitor C_{fdc}

Single-phase voltage sag brings a negative-sequence component to the source voltage. In this case, the series converter injects the three-phase compensating voltages including the negative-sequence component, the amplitude of which is the same as that of the positive-sequence component. The negative-sequence voltage induces a voltage fluctuation with twice the line frequency to the dc capacitor. This section discusses the required capacity of the dc capacitor to smooth the voltage fluctuation when voltage sag occurs in the u-phase. When voltage sag occurs in the u-phase, the voltage depth is given as follows [6]:

$$\Delta V_{Su} = \sqrt{\frac{2}{3}} \delta V_s \cos \omega t$$
$$\Delta V_{Sv} = 0 \qquad (9)$$
$$\Delta V_{Sw} = 0$$

It is assumed that both the load current i_L, and the input current to the shunt converter, i_R are sinusoidal with unity power factor. Moreover, the u-phase source current is also assumed to be sinusoidal as follows:

$$i_{Su} = i_{Lu} + i_{Ru} = \sqrt{2} I_s \cos \omega t, \qquad (10)$$

where I_s is the rms value of i_{su}. The series converter injects a compensating voltage to the load. The released active power PC is given by

$$P_C = \frac{\delta V_s I_s}{\sqrt{3}} + \frac{\delta V_s I_s}{\sqrt{3}} \cos 2\omega t. \qquad (11)$$

The first term on the right hand side in above equation means an average value of P_C. The shunt converter should take in the average power to maintain the dc mean voltage across the dc capacitor. The power taken in, P_R is given by

$$P_R = \sqrt{3} V_s I_R = \frac{\delta V_s I_s}{\sqrt{3}}, \qquad (12)$$

where I_R is the rms value of i_R. Substituting this equation to i_{su} yields,

$$I_s = \frac{3 I_L}{3 - \delta}. \qquad (13)$$

On the other hand, the second term in P_C causes a voltage fluctuation to the dc capacitor. The energy stored in the dc capacitor, W_{store} is given by

$$W_{store} = \int (P_R - P_C) dt = -\int \frac{\delta V_s I_s}{\sqrt{3}} \cos 2\omega t dt$$
$$= \overline{W}_{store} - \frac{\delta V_s I_s}{2\sqrt{3}\omega} \sin 2\omega t \qquad (14)$$

where $\overline{W}_{store}$ is the average energy of W_{store}.

It is assumed that the dc-capacitor voltage v_{dc} is the sum of the average voltage V_{dc} and the voltage fluctuation Δv_{dc}. The stored energy W_{store} is given by

$$W_{store} = \frac{C_{dc}}{2} v_{dc}^2 = \frac{C_{dc}}{2} (V_{dc}^2 + 2 V_{dc} \Delta v_{dc} + \Delta v_{dc}^2). \qquad (15)$$

Assuming that $\Delta v_{dc} << V_{dc}$, the voltage fluctuation is represented by

$$\Delta v_{dc} = -\frac{\delta V_s I_s}{2\sqrt{3}\omega C_{dc} V_{dc}} \sin 2\omega t = -\frac{\delta P_L}{2\omega C_{dc} V_{dc} (3 - \delta)} \sin 2\omega t \qquad (16)$$

Thus, the required capacity of the dc capacitor, C_{dc} is obtained by

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$$C_{dc} = \frac{\delta P_L}{2\omega\varepsilon V_{dc}^2(3-\delta)} \qquad (17)$$

where ε is the ratio of the amplitude of the voltage fluctuation where with respect to the dc capacitor voltage V_{dc}. The experimental setup rated at 415 V and 4.2 kW requires a dc capacitor of C_{dc} = 30μF when the voltage fluctuation is limited within ε = 2.5% for compensation of a single-phase voltage sag with δ = 0.3. The unit capacitance constant H is given by

$$H = \frac{\delta}{4\omega\varepsilon(3-\delta)}. \qquad (18)$$

Substituting the previous conditions to the above equation yields H = 7.5 ms. Now the required capacitance of the dc capacitor C_{fdc} is given as follows:

$$C_{fdc} = \frac{D_{sag}V_{SL-L}I_L Cos\phi}{2\sqrt{3}\omega\varepsilon V_{dc1}^2(3-D_{sag})} \qquad (19)$$

where V_{sL-L} is the line-to-line rated load voltage, I_L is the rated load current, cos ϕ is the power factor of the load, ω is the angular speed (ω = 2ΠIf), ε is the allowable dc voltage fluctuation (ε = Δv_{dc1} / V_{dc1}) and V_{dc1} is the dc voltage of the uncontrolled rectifier.

The dc voltage of the uncontrolled rectifier (V_{dc1}) is almost equal to the magnitude of line-to-line load voltage (V_{dc1} = V_{sL-L}). Therefore the above equation can be rewritten as

$$C_{fdc} = \frac{D_{sag}I_L Cos\phi}{2\sqrt{3}\omega\varepsilon V_{SL-L}(3-D_{sag})} \qquad (20)$$

With the line-to-line voltage V_{sL-L} = 415 V, ω = 2ΠIf (f = 50Hz) and ε = 2.5%, the C_{fdc} is selected to be 200μF for 0.3 voltage sag depth and 0.8 lagging power.

III.B. Sizing the inductor L_{dc} and the dc capacitor C_{dc}

The inductor L_{dc} and the capacitor C_{dc} of the dc-to-dc step up converter are given by [1]

$$L_{dc} = \frac{V_{dc1}D}{\Delta I_{dc2} f_s} \qquad (21)$$

$$C_{dc} = \frac{I_{dc2}D}{\Delta V_{dc2} f_s} \qquad (22)$$

where D is the duty cycle of the dc-to-dc step up converter, f_s is the switching frequency of the switch (MOSFET) of the dc-to-dc step up converter (f_s = 1027 Hz), ΔI_{dc2} output current ripple of the dc-to-dc step up converter (ΔI_{dc2}= 0.02%), I_{dc2} is the dc output current of the dc-to-dc step up converter and ΔV_{dc2} is the ripple dc output voltage of the dc-to-dc converter (ΔVdc2 = 0.02%).

The inductor L_{dc} is directly proportional to the duty cycle D and the dc voltage of the uncontrolled converter V_{dc1}. Since V_{dc1} = V_{sL-L} [10] and by setting D = D_{max}, we can write,

$$L_{dc} = \frac{V_{SL-L}D_{\max}}{\Delta I_{dc2} f_s} \qquad (23)$$

The maximum duty cycle Dmax is given by

$$D_{\max} = \frac{V_{dc2} - V_{dc1\min}}{V_{dc2}} \qquad (24)$$

where V_{dc2} is the dc output voltage of the dc-to-dc converter (V_{dc2} = 500V) and V_{dc1min} is the minimum dc voltage of the uncontrolled rectifier.

The minimum dc voltage of the uncontrolled (V_{dc1min}) corresponds to the maximum voltage sag occurred in the distribution system. Therefore V^{dc1min} can be given by

$$V_{dc1\min} = 1 - D_{sag}V_{sL-L} \qquad (25)$$

By substituting V_{dc1min} into D_{max} and then the result is substituted in L_{dc}, the value of the inductor L_{dc} can be given by

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$$L_{dc} = \frac{V_{SL-L}(V_{dc2} + D_{sag}V_{SL-L} - 1)}{\Delta I_{dc2} f_s V_{dc2}} \qquad (26)$$

Since D_{sag} = 0.3, the value of the inductor L_{dc}, which corresponds to the same voltage sag depth, is selected to be L_{dc} = 12 mH.

Following the same procedure, the dc capacitor of the dc-to-dc step converter C_{dc} can be given by

$$C_{dc} = \frac{I_{dc2}(V_{dc2} + D_{sag}V_{SL-L} - 1)}{\Delta V_{dc2} f_s V_{dc2}} \qquad (27)$$

The active power injected by the DVR during the voltage sag, ignoring the losses in the PWM converter, is given [6] by

$$P_{inj} = D_{sag}\frac{V_{SL-L}}{\sqrt{3}} I_L \cos\phi = V_{dc2} I_{dc2} \qquad (28)$$

The expression of the dc output current from the dc-to dc converter I_{dc2} can be obtained from the above equation and then substituted in C_{dc}. Thus, the dc capacitor C_{dc} can be given by

$$C_{dc} = D_{sag}\frac{V_{SL-L}}{\sqrt{3}} I_L \cos\phi \frac{(V_{dc2} + D_{sag}V_{SL-L} - 1)}{\Delta V_{dc2} f_s V_{dc2}^2} \qquad (29)$$

For voltage sag depth D_{sag} = 0.3 and power factor of 0.8, the value of capacitor C_{dc} = 30μF. It has to be mentioned that the size of C_{dc} is much smaller than the size of C_{fdc} since its main function is to reduce the ripple in the output dc voltage of the dc-to-dc step up converter V_{dc2} [1] .

IV. SIMULATION RESULTS

IV.A. DVR without any energy source

Fig. 7 shows the three phase source voltage and load voltage waveform of the system when 70% (0.3pu) voltage sag is applied to it. Here the sag was introduced for 0.3sec (0.2sec – 0.5sec). The first graph shows the sag affected source voltage and second graph shows the compensated load voltage.

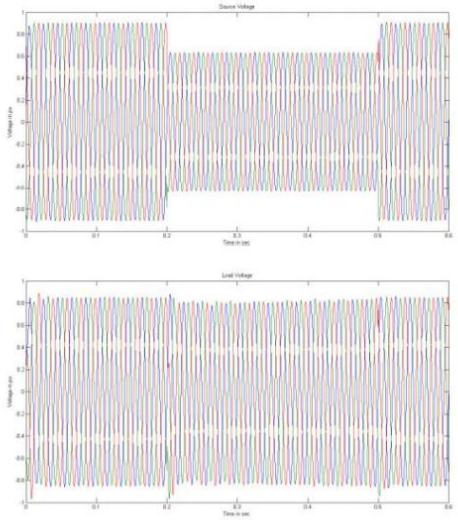

Fig.7.Source and load voltage waveform of DVR with 0.3pu voltage sag.

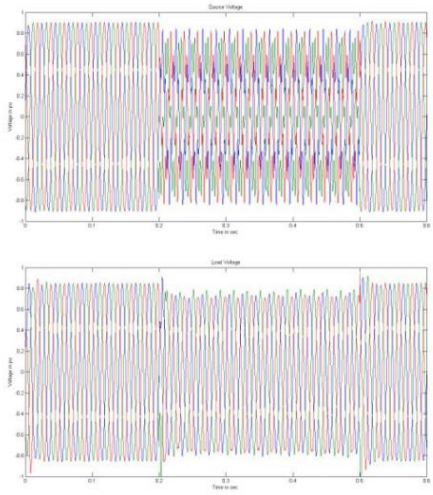

Fig.8. Source and load voltage waveform with combined 0.3pu voltage sag and fifth harmonics.

Fig. 8 shows the three phase source voltage and load voltage waveform, when 70% (0.3pu) voltage sag and fifth harmonics was applied to the system for 0.3sec (0.2sec – 0.5sec). The first graph shows the source voltage waveform and second graph shows the load voltage waveform.

IV.B. DVR with any energy source

Fig. 9 shows the three phase source voltage and load voltage waveform of the system when 70% (0.3pu) voltage sag is applied to it. Here the sag was introduced for 0.3sec (0.2sec – 0.5sec). The first graph shows the sag affected source voltage and second graph shows the compensated load voltage.

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Fig. 10 shows the three phase source voltage and load voltage waveform, when 70% (0.3pu) voltage sag and fifth harmonics was applied to the system for 0.3sec (0.2sec – 0.5sec). The first graph shows the source voltage waveform and second graph shows the load voltage waveform.

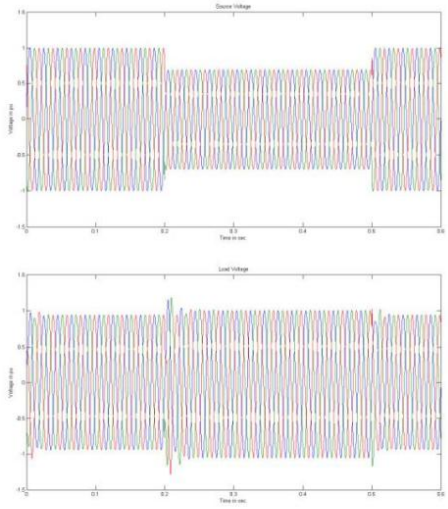

Fig.9.Source and load voltage waveform of DVR with 0.3pu voltage sag.

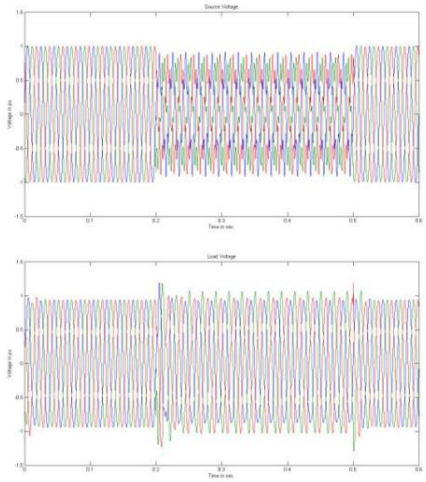

Fig.10. Source and load voltage waveform with combined 0.3pu voltage sag and fifth harmonics.

Each topology has been rated by its expected performance for same main parameters. Although the best topology cannot be absolutely stated some main differences can be seen.

With the comparison system adopted, System 2 has the highest total point score, with a generally high performance score and relatively low cost and complexity. However, the negative grid effects and requirement for a high rated series converter could disqualify this solution for certain applications. System 1 is ranked as the second best topology with the highest performance scores, particularly for deep voltage sags, but with significant drawbacks regarding complexity, converter rating and overall cost (energy storage and power converter). System 1 and System 2 represent two conceptually different topologies (without energy storage and with energy storage) and might be the best alternatives depending on the applications.

TABLE I

THD values of the test system

Sl. No.	Conditions	Converter with Stored Energy Source	Constant DC Link Voltage with No Stored Energy Source
1	Voltage sag of 0.3pu	4.91	4.49
2	Voltage swell of 0.3pu	4.91	4.49
3	Fifth harmonics in the system	4.89	4.37
4	Voltage sag and fifth harmonics combined	4.91	4.49
5	Load current during 0.3pu sag	4.74	4.25
6	Load current during fifth harmonics	4.79	4.1
7	Load current during combined distortions	4.74	4.25
8	Voltage sag of 0.5pu	4.25	4.49

TABLE II

Comparison of the two different DVR topologies

Sl. No.	Properties	Load Side Connected Converter with Stored Energy Source	Constant DC Link Voltage with No Stored Energy Source
1	Long voltage sag duration compensation	Good (-)	Better (+)
2	Deep voltage sag compensation	Better (+)	Good (-)
3	DC link for voltage control	No need (+)	Needed (-)
4	Size of energy storage	Large size (-)	No need (+)
5	Effects on grid	Medium (-)	Less (+)
6	Rating of shunt converter	Less rating (-)	No need (+)
7	Rating of series converter	Less rating (+)	Less rating (+)
8	System complexity	Less (+)	More (-)
9	Cost estimation	More (-)	Less (+)
10	Control of complexity	More (-)	Less (+)
	Total (+)	**4**	**7**

V. CONCLUSION

Power electronic solutions have gained increased interest, to solve well-known power quality problems. Voltage dips have been reported as a major power quality problem and a series connected converter, like the DVR, is considered to be an effective and cost-effective solution to mitigate voltage dips. Two system topologies for DVR have been

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compared through modeling and analysis. It includes one topology with stored energy and the other which uses the supply voltages and increase the supply current to restore the load voltages. The result shows that the topology without stored energy has got the better performance.

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