ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization *Vol. 4, Special Issue 1, March 2015*

National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015)

Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India

On 26th & 27th March 2015

Bit Stream Implemented PLL Based Frequency Synthesizer for Power Line Communication

Renu Mary George, Mathew George

Assistant Professor, Dept. of EEE, Mar Baselios Institute of Technology and Science, Kerala, India [1]

Senior Design Engineer (Analog & Mixed Signal), Wipro Technologies, Bangalore, India[2]

ABSTRACT: Power line communication (PLC) has been the branch of wired communication in high voltage (HV) for a very long time and these days, PLC application in medium voltage (MV) power networks has been taken into account. Frequency synthesizer is an effective way to realize multi carrier generation suitable for frequency hopping in power line communication. Phase-locked loop facilitates more and more extensive application in the modern frequency synthesized technology. Bit-stream implemented phase locked loop based frequency synthesizer increases the controllability. The proposed system is one in which the phase locked loop based frequency synthesizer for power line communication is implemented using bit stream technique which is expected to increase the reliability and controllability of the whole system.

KEYWORDS: Phase Locked loop; Bit stream; Frequency synthesizer; Power line communication Security.

I.INTRODUCTION

Power line communication or power line carrier (PLC), are systems for carrying data on a conductor which is being used for electric power transmission. The electric power distribution grid offers a tremendous potential for extended fast and reliable communication services. But there indeed exist many difficulties such as large transmission attenuation, high noise level, high voltage isolation, variation of power line impedance. The frequency shift keying (FSK) with the single carrier couldn't ensure the reliability of communication, while the frequency-hopping can better overcome the frequency-selective attenuation of channel and the effects of various narrow-band interferences The combination of FSK and frequency-hopping technology is a better option for PLC system. Frequency synthesizer is an effective way to realize carrier generation in fast frequency hopping communication systems.

By the phase-locking characteristic of PLL, the new frequencies with certain multiples of the reference frequency can be obtained. Phase-locked loop facilitates more and more extensive application in the modern frequency synthesized technology. Frequency synthesizers are widely used in frequency hopping wireless applications. Frequency synthesis can output a large number of carrier signals with a certain frequency interval and the same stability as reference frequency through a series of arithmetic operations.

Bit stream technique is a novel method of signal representation where signals are represented using uniformly weighted single bit streams. The fundamental difference between bit-stream and other digital control methods is in the representation of the signals. While a standard digital controller, such as a microprocessor, represents an integer using several wires in parallel, a bit-stream system represents a signal as a stream of uniformly weighted bits which pass through a single wire. This single-bit representation offers significant advantages over multibit representations since they mitigate the fan-in and fan-out issues and also only one physical wire is required to complete a source-destination link which immediately reduces the interconnect density when compared to multibit representations and thus reducing interconnect resources. Moreover, this technique allows the implementation of complex control schemes directly in digital logic chips such as FPGAs, and all control parameters such as sampling rate and resolution can be adjusted as

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization *Vol. 4, Special Issue 1, March 2015*

National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015)

Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India

On 26th & 27th March 2015

per the designer's wish and also analogue to bit-stream conversion can be implemented using simple one-bit Sigma Delta modulator.

The bit-stream-based PLL is simple and flexible, operates independently of other systems on the FPGA owing to the inherently parallel nature of bit-stream systems, and consumes fewer logic resources than a 'soft-core' microprocessor implementation.

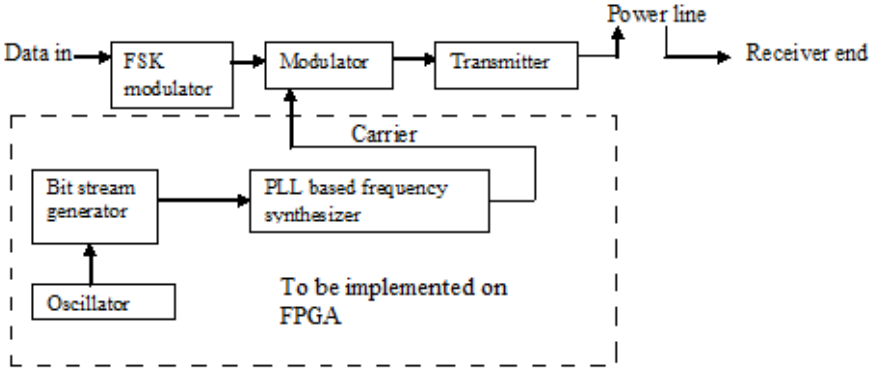

Fig 1.Block diagram of power line communication system

Power line communication technology is being used for various applications such as Automatic meter reading, Home control and automation, Home networking, Transmission of radio programs, Internet access.

The implementation of this bit stream implemented PLL frequency synthesizer for power line communication is done on XILINX SPARTAN 3E FPGA kit.

II.BIT STREAM CONCEPT

The bit-stream technique uses a sequence of two uniformly weighted quanta, namely, $+Q$ and $-Q$, to represent any analog or binary signal. A logical value of "1" is assigned a $+Q$, while a logic "0" is assigned a $-Q$. Thus, a digital square wave, which is an alternating stream of logic 1s and logic 0s, will encode a zero value over a collection of several logic transitions. Signal *z* in Fig 1 shows a zero-valued signal.

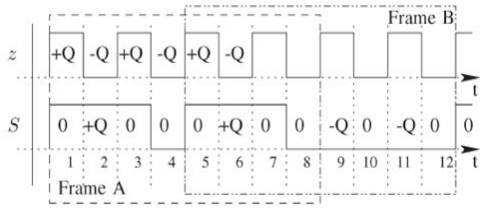

Fig. 2. Bit stream representation

A.ZERO MAGNITUDE

Since a logic "1" is defined to be a positive quantum +Q and a logic "0" to be a negative quantum -Q, then an alternating stream +Q and -Q will cancel each other and result in a zero value. This perfect zero is shown as signal z in Fig.4.1 and will be denoted by *zero*. This *zero* signal will be used to determine the instantaneous value of any bit stream and can be easily generated within any functional element [2]. Over a frame of several quanta, the inversion of a few logic 0s to logic 1s will result in a positive-valued bit stream, while the inversion of a few logic 1s to logic 0s will lead to a negative-valued bit stream. Signal *S* in Fig.1 shows an arbitrary bit-stream signal. The magnitude of *S* can be extracted by comparing *S* and the zero-valued bit stream on a bit-by-bit basis.

The resolution of a bit-stream system is set by defining a fixed frame length N in which these quanta are summed. The frame length is normally defined as a power of two – where N = 2^R bits – so that R is the equivalent number of bits of resolution of the system

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization *Vol. 4, Special Issue 1, March 2015*

National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015)

Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India

On 26th & 27th March 2015

The PLL in this paper is implemented using an equivalent number of bits R =8, which allows for the expression of bit-stream values in the range of +127 to-128 quanta (Q). Internal bit-stream signals will saturate at +127 Q or -128 Q in an intuitive manner. In some applications, the inputs may be analog, and hence, will require conversion to a digital value. These can be easily converted into a bit stream using sigma–delta convertor [1]. These convertors (also known as modulators) have been in regular use, mostly in non real-time applications. The bit-stream can be regarded either as a digital or an analogue signal.

B. BIT STREAM GENERATION

Analogue to bit-stream conversion can be implemented using simple Σ-Δ modulators.

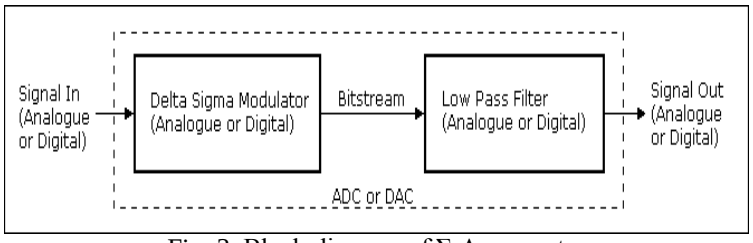

Fig. 3. Block diagram of Σ-Δ converter

A delta sigma ADC or DAC always consists of a delta sigma modulator which produces the bit-stream and a low pass filter. The delta sigma modulator is the core of delta sigma converters. As mentioned above it produces a bit-stream output. The average level of this bit-stream represents the input signal level. A simple analogue delta sigma modulator block diagram looks like this:

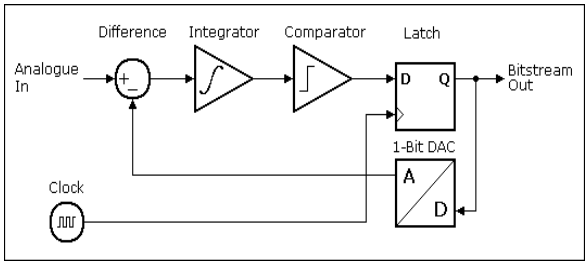

Fig. 4. Block diagram of Σ-Δ modulator

In order for hardware implementation of this bit-stream generator on FPGA, hardware description has been made in VHDL for realization in FPGA. For this purpose we have pursued by considering the transfer function. [5]

III. ARCHITECTURE OF PLL FREQUENCY SYNTHESIZER

PLL frequency synthesizer is a negative feedback control system, which is composed of phase detector (PD), loop filter (LPF), controlled oscillator, reference divider and variable divider.

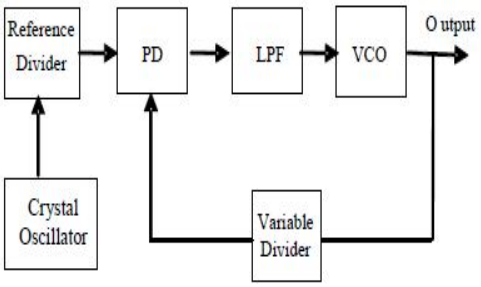

Fig 5. Frequency synthesizer based on PLL

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization *Vol. 4, Special Issue 1, March 2015*

National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015)

Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India

On 26th & 27th March 2015

PD compares the reference input with the feedback of the VCO's output, and controls the VCO, (in our case NCO) according to the two signals. At last, the output signal of VCO synchronizes with the reference input signal in frequency as well as in phase PLL has a good narrow-band filtering characteristic. After loop locking, the temperature and time stability of the output signal is the same as the reference input. When PLL locks onto a reference signal, the output frequency is given by

$$f_y = f_i * N / M$$

Where M and N are the division ratio of the reference divider and variable frequency divider, and f_i is the input frequency. A series of output frequencies in a desired frequency range can be obtained by changing the division ratio N and M. Counters can be used as frequency divider, which are realized by programmable devices FPGA.

IV. SIMULATION AND RESULT

For simulating the proposed system, the entire unit was modeled using Modelsim VHDL simulator and compared the response with that of a Matlab/Simulink model. XILINX SPARTAN 3E FPGA kit is used for implementation of the system. The bit-stream generation is achieved with the help of sigma-delta modulator. The whole system of PLL based frequency synthesizer is simulated with the help of simulink.

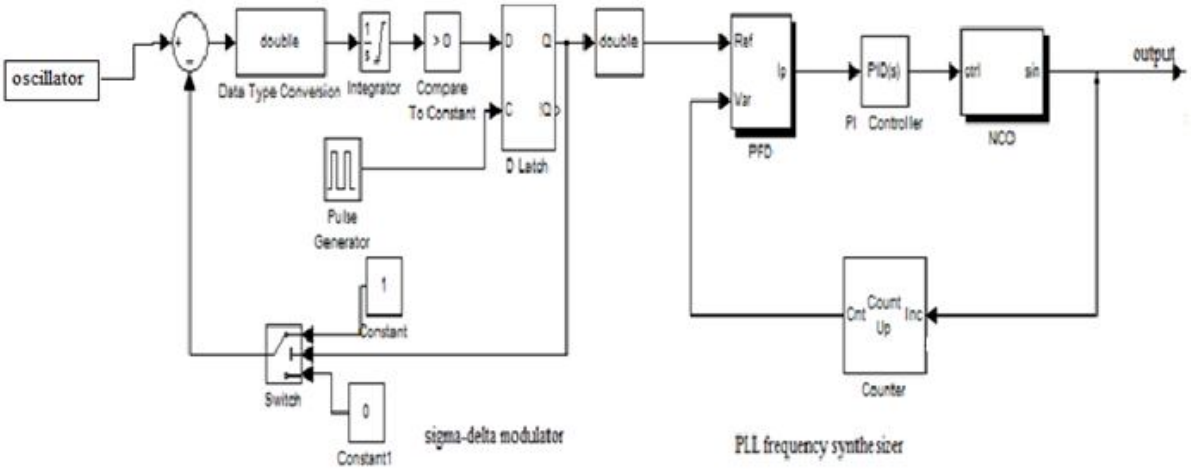

Fig 6 Block diagram of carrier generation system

Here in this paper phase detector is implemented using an XOR gate. A proportional integral(PI) controller is used for implementing the loop filter. Numerical controlled oscillator is used for the implementation of controlled oscillator. The variable divider required for the frequency synthesizer is implemented using counter. Receiver synchronization should be done for the whole system at the receiver end. So counter is implemented in such a manner that the output frequency varies in the required frequency range.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization *Vol. 4, Special Issue 1, March 2015*

National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015)

Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India

On 26th & 27th March 2015

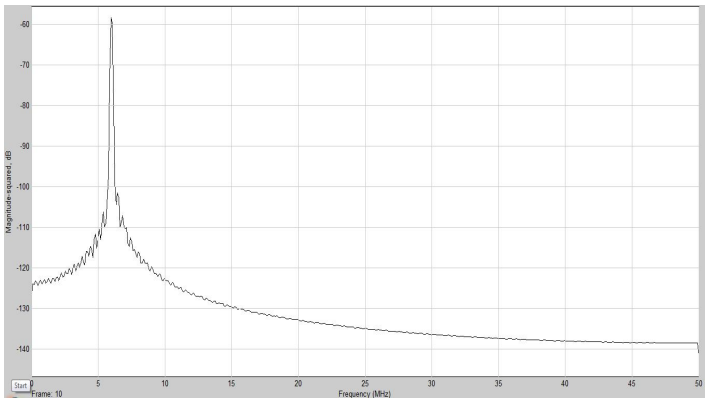

Fig.7 Output waveform of spectrum scope

Here in the above waveform locking happens at frequency of 6 MHz when the maximum count of counter is given as 3 and reference frequency as 2 MHz. As the maximum count is changed locking frequency also changes.

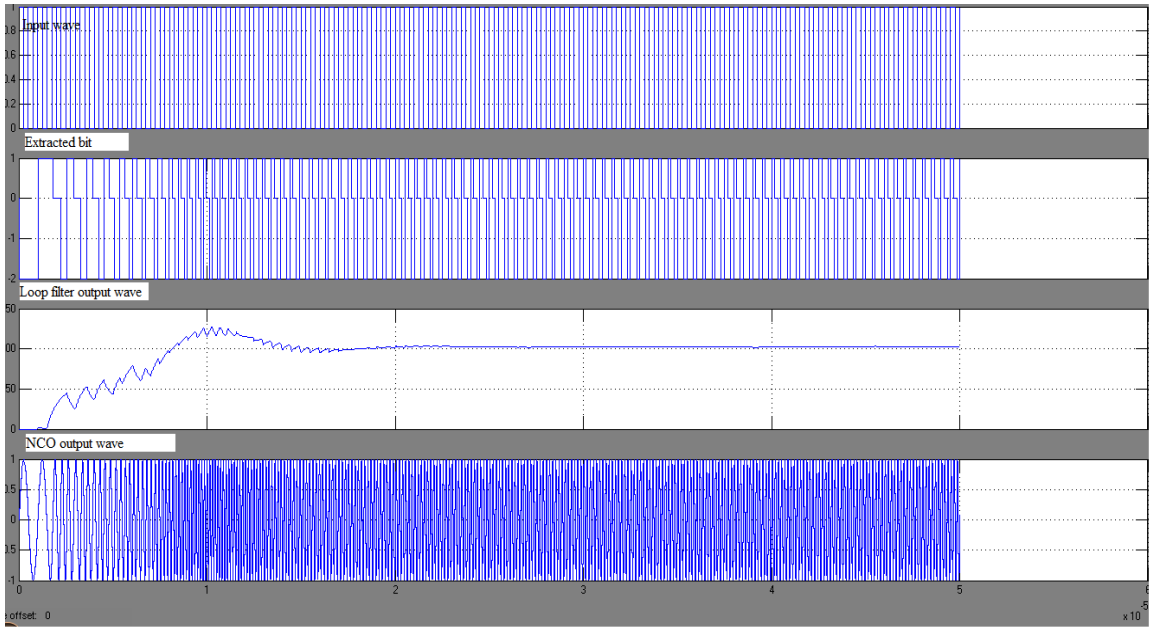

Fig.8 Output waveforms of PLL frequency synthesizer

Here as we change the maximum count of counter, the locking frequency also changes .Thus we can control it by changing the count of the counter. Our application is broadband over power line (BPL) whose carrier frequency is specified within a band of 2-80MHz.A range of 4 -8 MHz has been obtained. The table shown below gives an idea about the locking frequencies obtained for various maximum counts.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization *Vol. 4, Special Issue 1, March 2015*

National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015)

Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India

On 26th & 27th March 2015

Max count for counter	Max frequency in Spectrumscope (locking frequency)(MHz)
1	2
2	4
3	6
4	8

Table 1 Locking frequencies obtained for various maximum counts

The simulation has proceeded by the VHDL simulation of bit stream generator i.e sigma-delta modulator, phase detector, controlled oscillator, in our case NCO , PI controller, counter .As we know ,all these blocks were combined using structural programming so that it works as a PLL based frequency synthesizer. This combined block was compiled and loaded for simulation in Modelsim environment. The output obtained is shown below.

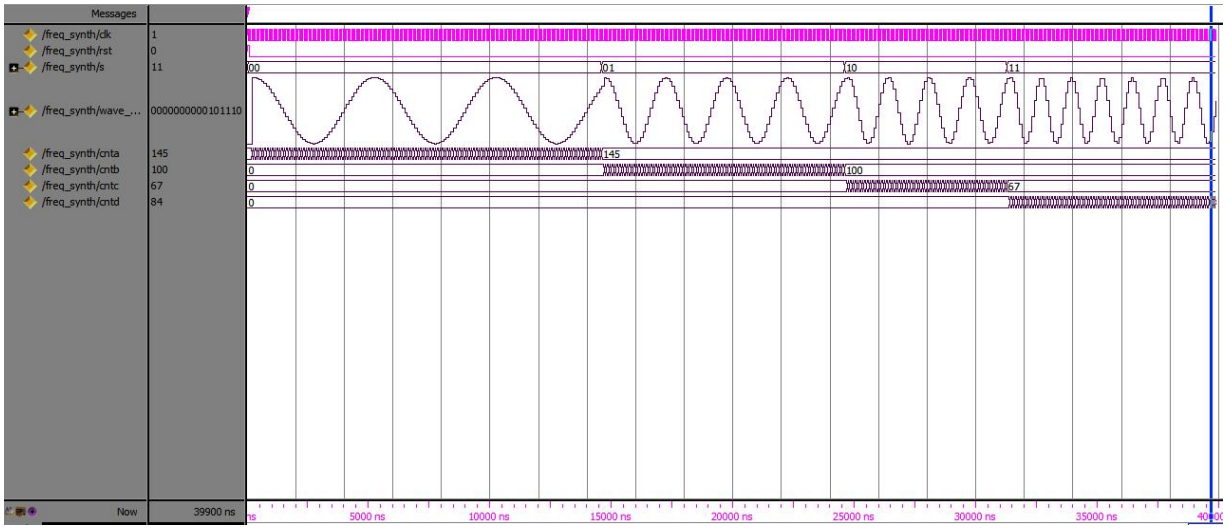

Fig 9 Waveform of a PLL based frequency synthesizer

A.HARDWARE REALIZATION

The Behavioral Synthesized HDL code is synthesized and realized using **Spartan-3E** kit having the configuration 3s3500efg320-4.Programming file is generated for synthesized codes and the generated bit file is downloaded into FPGA. Thus the whole design is downloaded into FPGA.

Fig 10. Hardware realization using FPGA.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization *Vol. 4, Special Issue 1, March 2015*

National Conference on Recent Advances in Electrical & Electronics Engineering (NCREEE 2015)

Organized by

Dept. of EEE, Mar Baselios Institute of Technology & Science (MBITS), Kothamangalam, Kerala-686693, India

On 26th & 27th March 2015

VI.CONCLUSION

Power line communication in medium voltage power networks is an emerging wired communication branch. Bit stream technique is a novel method for representation of signals which improves the reliability and controllability and it is realized using a sigma-delta modulator which considerably reduces the issues related to aliasing and also helps in reducing fan-in and fan-out issues and thus hardware requirements. Frequency synthesizer is an effective way to realize multi-carrier generation. The proposed new PLL frequency synthesizer implemented using bit stream technique for power line communication application thus synthesizes frequency with the above mentioned advantages. Matlab and Modelsim simulation is done. Implementation is performed using HDL (Hardware Description language). The implementation is done on XILINX Spartan 3E. As the responses matches with each other bit stream implemented PLL is an apt option for frequency synthesizers for power line communication.

REFERENCES

1. J. Bradshaw ,U. Madawala, N. Patel : 'Bit-stream implementation of a phase-locked loop', IET Power Electron., 2011, Vol. 4, Iss. 1, pp. 11–20
2. Patel N., Nguang S.K., Coghill G.: 'Neural network implementation using bit streams', IEEE Trans. Neural Netw., 2007, 18, (5), pp. 1488–1504
3. Patel N., Madawala U.: 'Brushless dc motor control using bit-streams'. Tenth Int. Conf. on Control, Automation, Robotics and Vision, 2008, ICARCV 2008, December 2008,pp. 85–90
4. An Introduction to *Delta Sigma* Converters, www.beis.de/Elektronik/DeltaSigma/DeltaSigma.html
5. Michael Melin, Magnus Nilsson: 'Realization of a sigma-delta modulator in FPGA', Bachelor thesis 1999 at Ericsson Microwave Systems AB
6. Bradshaw J., Patel N., Madawala U: 'Implementation of phase locked loops using Bit-Stream control techniques'. Proc. IEEE Int. Conf. Industrial Technology, ICIT,Melbourne, Australia, February 2008, pp. 1–6
7. Best R.: 'Phase locked loops', in Chapman S. (Ed.):(McGraw-Hill, 6th edn., 2007)
8. Patel N., Madawala U.: 'Brushless dc motor control using bit-streams'. Tenth Int. Conf. on Control, Automation, Robotics and Vision, 2008, ICARCV 2008, December 2008, pp. 85–90
9. Cordesses L.: 'Direct digital synthesis: a tool for periodic wave generation (part 1)', IEEE Signal Process. Mag., 2004, 21, (4), pp. 50–54
10. Yihe Guo, Zhiyuan Xie: ' Design of PLL Frequency Synthesizer in Frequency Hopping Communication System', 2010 IEEE International Conference on Communications and Mobile Computing
11. Gotz M, Rapp M, and Dostert K, ' Power line channel characteristics and their effect on communication system design,'IEEE Communications Magazine, vol. 42, no. 4, pp.78–86, April 2004.
12. Power Line Communication Modem - TI.com, www.ti.com › Applications