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A Bridgeless PFC SEPIC Converter for low voltage Switched Mode Power Supplies

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ABSTRACT: Active power factor correction (PFC) circuits are been widely used in ac–dc converters and switched-mode power supplies due to an increase in demand for high power factor and low harmonic pollution. This paper discuss A new Bridgeless PFC SEPIC converter for switched mode power supplies. Due to bridgeless configuration, input diode bridge is eliminated thereby reducing conduction losses, also the input current ripple of the new converter is considerably low. A control scheme for the converter is also discussed here. The proposed scheme provides power factor correction, which will be useful in low power switched mode power supplies

KEYWORDS: power factor correction (PFC), SEPIC converter.

I.INTRODUCTION

There has been a tremendous increase in use of power electronic equipment due to recent advancement in field of power electronics. AC–DC converters/rectifiers are found in several applications such as switch-mode power supplies (SMPs), uninterrupted power supplies (UPSs), etc. Switched mode power supplies replaces linear power supplies when higher efficiency, smaller size or lighter weight are required. They uses smaller transformer or inductors due to higher operating frequency. They are, however, more complicated as their switching currents can cause harmonics problems if not carefully suppressed, and simple designs usually have a poor power factor.

Various standards like IEC 61000-3-2 has set limits on the distortion from harmonic currents that these device can place on its AC mains supply [1]. Harmonics reduction with a consequent increase of power factor can be realized by using either passive or active power factor correction (PFC) methods. Passive methods include the use of LC filters. However, in such methods line frequency components are large and heavy which increases the weight and volume as a result. Moreover, the passive filter needs to be redesigned as load characteristics changes. Active PFC methods are more efficient by using controlled power semi converter switches in association with passive elements such as resistors, inductors, and capacitors. Active PFC is more preferable since it makes the load to appear like a pure resistor to the line, leading to near-unity power factor and creating negligible harmonics in the input line current .The active power factor correction (PFC) circuits are widely used to effectively draw the energy from the mains via an AC to DC converter[2]-[4].

A diode bridge rectifier followed by a suitable converter topology has been the most commonly topology of PFC circuits. PFC circuits can be realized without using a full-bridge rectifier circuit, called as a bridgeless PFC topology. The very first bridgeless PFC topology was proposed D.M Mitchell in 1983. The bridgeless PFC topology has less number of components conduct at each switching cycle compared to the conventional PFC circuit. Among the bridgeless PFC converters, boost PFC circuit operating in continuous-conduction mode (CCM) is, by far, the popular choice for medium- and high-power applications. Fig 1 shows a bridgeless boost converter. A bridgeless boost converter is commonly used PFC due to its advantages of reduced input current ripple and high efficiency. However, its dc output voltage is always higher than the peak input voltage the continuous nature of the boost converter's input current results in low conducted electromagnetic interference (EMI), but its output voltage should be higher than the peak voltage of the input [5].

In low-voltage switched mode power supplies, it is preferred to have the output voltage lower than the input ac voltage. Buck-type converter are used in such cases. But in certain cases when the line voltage is lower than the output voltage,

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PFC buck rectifier does not shape the line current during the time intervals , there exist is a strong trade-off between the THD and PF performance and output voltage selection.

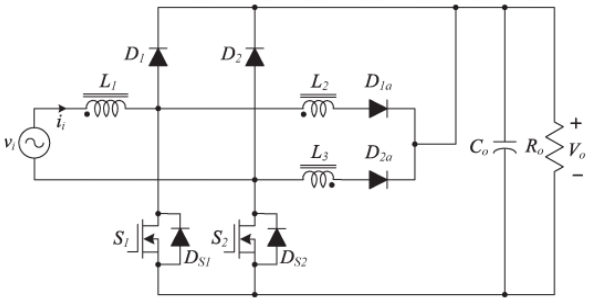

Fig 1. Bridgeless boost converter

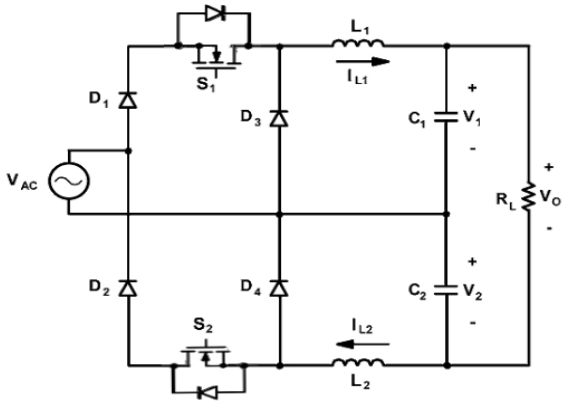

Fig 2. Bridgeless buck converter

Relatively low output voltage of PFC converters is required in many applications such as low-voltage switched-mode power supplies. PFC buck converters are more suitable for these applications due to their low output voltage. Like conventional buck converters, the output voltage of the PFC buck converter is lower than the peak value of the input voltage. The input current of the PFC buck converter has dead angles during the time intervals when the input voltage is lower than the output voltage, there is a strong trade-off between power factor and output voltage selection .In such cases, output should be increased to reduce the size of storage capacitor. But this cause increase in THD and lowers the power factor [6].

A buck-boost converter can give the desired step up and step down functions but its output is inverted. A SEPIC (Single-Ended Primary Inductor Converter) topology can provides the desired output voltage. Thus, a SEPIC converter operate from an input voltage that is greater or less than the output voltage by varying its duty cycle. A SEPIC converter has become popular in recent years in many non-isolated applications. The SEPIC PFC converter can provide high power factor regardless its output voltage due to its step up/down function. Several bridgeless single-ended primary inductor converters (SEPIC) were discussed in[7]-[9]. Coupled inductors have been used in converters to provide ripple-current steering. Switching ripple currents can be directed away from a source or a load .Coupled inductor techniques involves simultaneous parallel energy transfer pathways: electrical and magnetic. A coupled inductor filter is third order and is more effective than an inductor[10]-[11].

This paper presents a PFC Bridgeless SEPIC converter for low voltage power supplies and a control scheme for the converter is also discussed here. The discussed scheme provides power factor correction, which will be useful in low power switched mode power supplies.

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II. PREFERRED TOPOLOGY

Bridgeless SEPIC converter

A new bridgeless SEPIC converter is introduced here .The new topology has coupled inductor and its auxiliary circuit. Auxiliary circuit includes small inductor, and a capacitor. This is utilized to reduce the input current ripple. Coupled inductors are often used in circuits to reduce current ripple, passive component size and to increase power density. The auxiliary circuit is used here for achieving the input current ripple cancellation. Fig. 4 shows the gate signals for the switches. For a half period of the input voltage, one switch is turned ON continuously and the current via an intrinsic body diode is forced to flow through the channel of the switch. It reduces the conduction loss on the switch further and the efficiency can be improved .Fig.3 shows the circuit diagram of the preferred bridgeless SEPIC PFC converter.

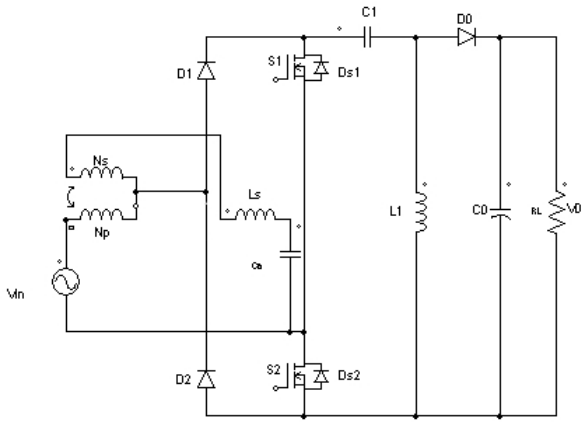

Fig.3 The discussed Bridgeless SEPIC converter.

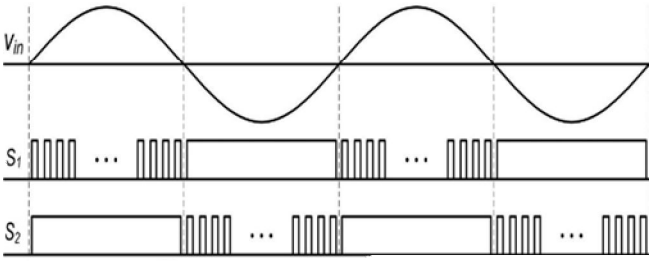

Fig. 4. Gate driving signals for switches

The auxiliary circuit includes an auxiliary inductor L_s and a capacitor C_a .The coupled inductor L_c a turn ratio of 1:n (n=Ns/Np). The leakage inductance of the coupled inductor is included in the auxiliary inductor Ls. The capacitance of C_a is large enough, so it is considered as a voltage source during a switching period. According to the volt-second balance law ,for steady state operation of an inductor in a Converter, net inductor voltage in a switching period must be zero. So the average capacitor voltage V_{Ca} is equal to the input voltage V_{in} during a switching period. In the same way, the average capacitor voltage V_{C1} is equal to V_{in}. D_1 and D_2 are the input rectifiers Diodes. D_{S1} and D_{S2} are the intrinsic body diodes of the switches S_1 and S_2. The switches S1 and S2 are operated with the gate signals shown in Fig. 4. The other components are capacitor C_1, inductor L_1 and a diode D_o . The operation of the converter is symmetrical in two half-line cycles of input voltage. Therefore, the converter operation can be analysed during one switching period in the positive half-line cycle of the input, so the output diode D_o will be turned OFF before the main switch is turned ON. The capacitance of the output capacitor C_o is assumed sufficiently large to consider output voltage as a constant. Its assumed that input voltage V_{in} is a constant in a switching period T_s.

The circuit operates in discontinuous conduction mode .There are three modes of operation varying from different time intervals t_0 to t_3. The magnetizing current i_m varies from its maximum value I_{m1} to its minimum value I_{m2} .It moves towards maximum from time period $t_0 - t_1$and settles back to minimum value from t_1- t_2 .Similarly the inductor current

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is varies from its maximum value I_{s1} to its minimum value – Is_2. The input current is the sum of the freewheeling currents I_{s2} and I_{L2} in the time interval t_2-t_3.

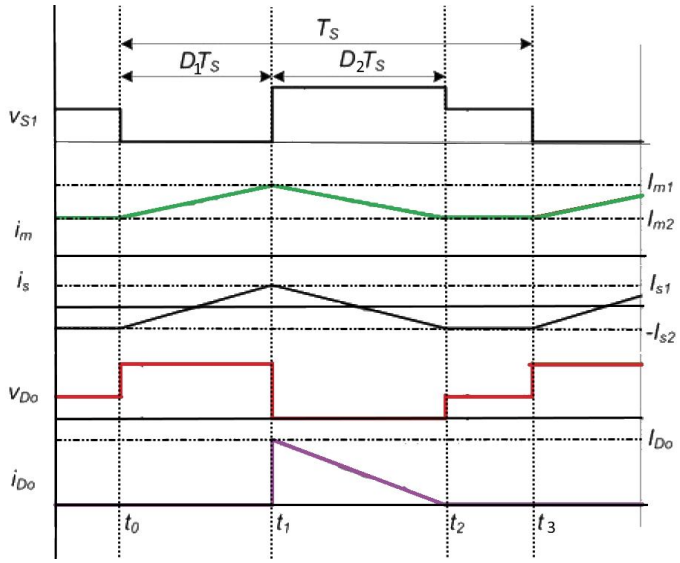

Fig.5 Key waveforms of the discussed Converter

Thus, the operation of the converter in one switching period T_s can be divided into three modes. Fig. 5 shows key waveforms when the operating modes in the positive input voltage.

III. CONTROL STRATEGY

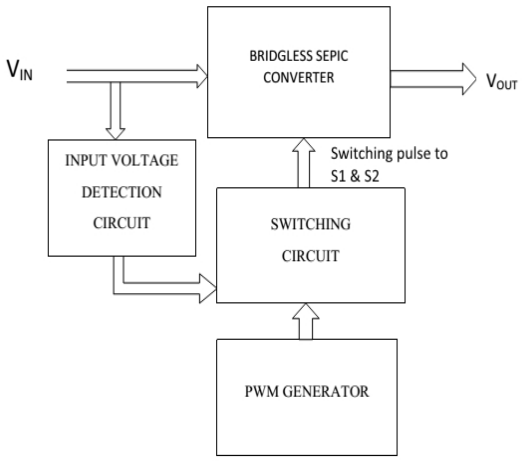

Fig.6. Control block of the converter

Fig.6 shows the control strategy for the converter. In includes input voltage sensing unit, switching circuit and a PWM generator .The PWM generator generates suitable pulse for switches with a given duty ratio. By varying the duty ratio we can set the circuit for operating in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). In CCM, a control circuit is required, but in DCM, the converter can be made to operate at a fixed duty cycle. This corrects the input power factor (PF) [12].Here the circuit is assumed to be operating in DCM mode. The switching circuit accepts signal from input voltage sensor. The input voltage sensor is zero crossing detector which determine s polarity of the input voltage. This determines type of switching pulse send to the switches. In a half cycle of input

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voltage one switch is fed with PWM signal and other switch is made to continuously conduct through body diode. Gate drive isolation is required as a safety norm and operating conditions because the switch voltage floats with respect to ground.

IV. SIMULATION RESULT AND DISCUSSION

Simulation is done using matlab Simulink. Simulink model is designed for a power out of 100 watts with 36-volt dc, 3 ampere out for use in applications like embedded system, LED power supplies, low power SMPS etc.

Design specifications:

V_{in} = 130 Vac, V_{Out}= 36 volt DC, line frequency f_L = 50 Hz, switching frequency f_{sw} = 100 kHz, L_m = 600 µH, n = 0.7, Ls = 127 µH, L_1 =17µH, C_1 = 0.4 µ F, Co = 7.7 mF, load R_L = 12 Ω .Ripple voltage = 5% V_{Out}

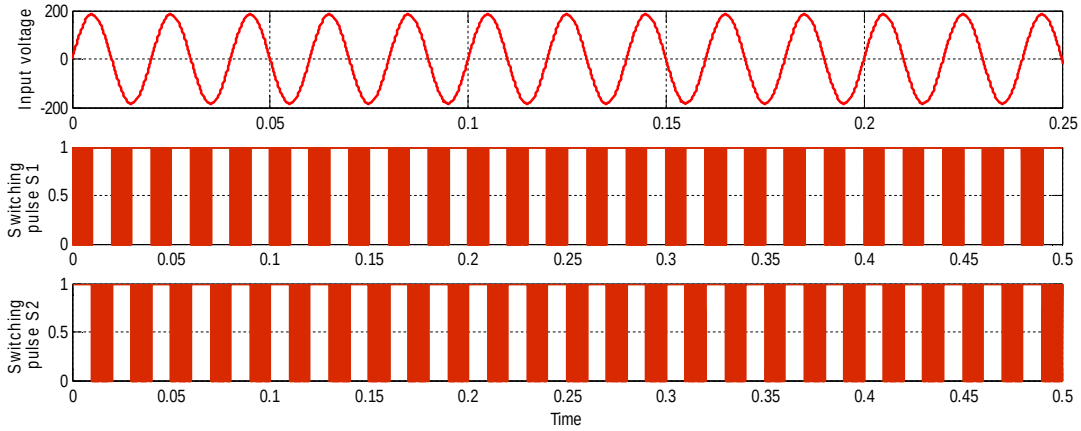

Fig. 7 Input voltage, Switching pulse to S1, S2 of the converter vs. simulation time

In the fig 7, it shows the input voltage, switching pulses of switches S_1 and S_2 vs. simulation time.

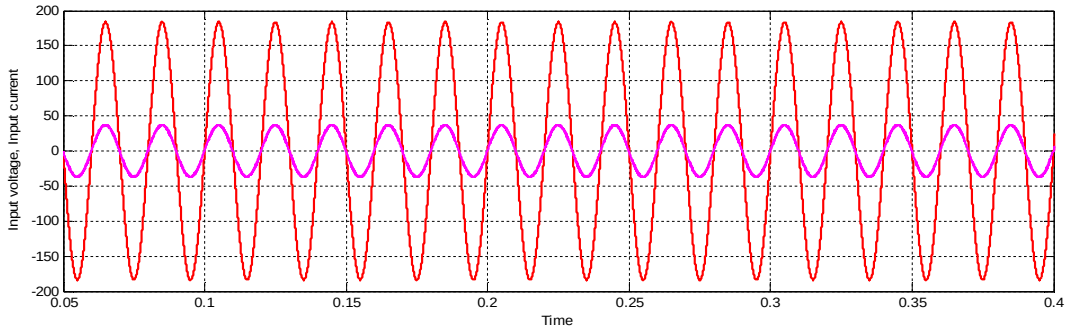

Fig. 8 Input voltage and input current vs. simulation time

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Above graph shows that input voltage and a scaled up input current, here they are in phase i.e. PFC is achieved.

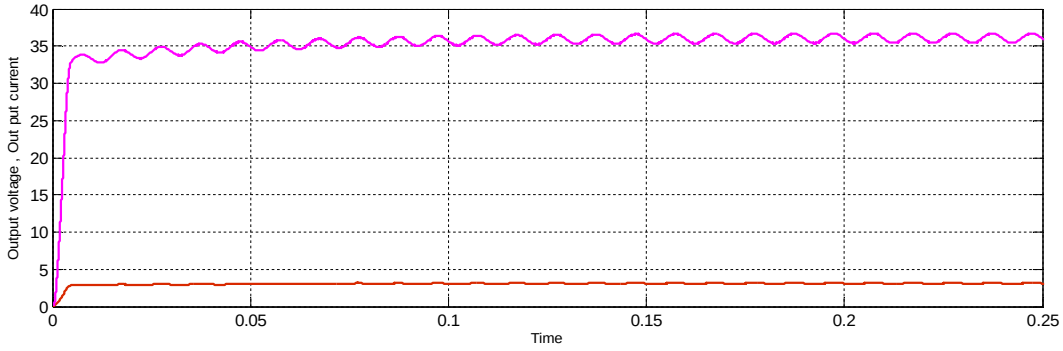

Fig. 9 Output voltage and Input current waveforms of the converter at rated load (load = 12 Ohms) vs. simulation time

V.CONCLUSION

This paper presented a bridgeless SEPIC converter and its control. The advantage of SEPIC converter includes reduced input ripple, power factor correction and low conduction losses. Simulation results of converter waveform were provided for verifying the control scheme. PFC and low ripple input current are the important features of the Converter. The converter circuit can be made as closed loop by incorporating voltage regulator; which can be used in a switched mode power supply.

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