Design and Simulation of Two Phase Interleaved Buck Converter

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ABSTRACT: Interleaved Buck DC DC converters have presently acquired a wide importance owing to their application in voltage regulator modules. Interleaved Buck Converter (IBC) is adopted as a good solution for low voltage and high current applications. This paper presents the design of two phase interleaved buck converter and closed loop simulation of IBC against sudden variations in supply voltage conditions. Operating principle of IBC for (D<0.5) along with waveforms are clearly illustrated in this paper and it has been successfully verified using MATLAB simulink.

KEYWORDS: Buck converter, Interleaving Technique, Two Phase Interleaved Buck Converter, Continuous Conduction Mode.

I.INTRODUCTION

Investigation of interleaving technique for step down topology mainly points out the benefits interleaving offers to future microprocessors. Most of today's Voltage Regulator Modules (VRMs), which are used to power the microprocessors in computers, make use of conventional buck or synchronous buck topology [1]. At present, VRMs require output voltage lower than 1 V while output currents above 100A or so which makes the existing topologies inadequate. One of the circuits that are suitable for the low-voltage/ high-current output is an interleaved dc-dc converter. Interleaved Buck converters have proved to be very beneficial for future VRMs [1]-[6].

Interleaving can be thought of as a method of paralleling converters. In a broader view, interleaving means that N identical converters are connected in parallel as in Fig. 1 and the current through each switch is dispersed. When each converter provides the same current as the non-interleaved converter, the output current is N times higher. Therefore, the interleaved dc-dc converter is suitable to the low-voltage/high-current applications. Moreover, when the driving signals of N converters have $2\pi/N$ phase-shift one another, the output filter of the converter could be downsized [2]. Using interleaving, power stage of a converter is divided into several and smaller power stages thereby reducing the size of each component [7].
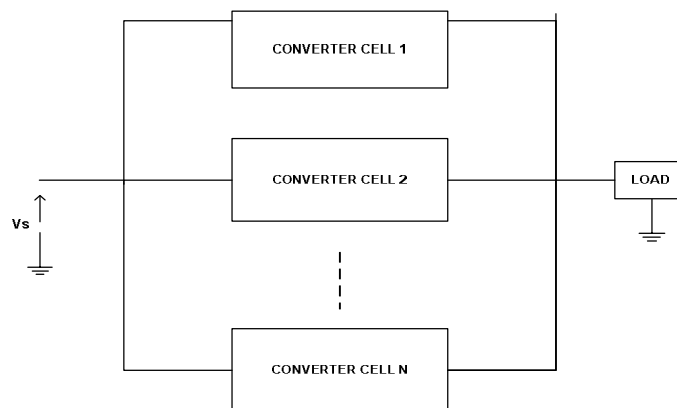

Fig. 1 Illustration of Interleaved Converter

The main goal of this paper is to present the state space analysis of two-cell IBC operating in continuous conduction mode (CCM) with D<0.5 .Section II presents operating principle of the IBC in CCM   and section III discusses the design aspects of interleaved buck converter , Sections IV   and V contain simulation results. Finally, paper is concluded in Section VI.

II. OPERATING PRINCIPLE – IBC

The circuit diagram of IBC is given as shown in Fig. 2. This is equivalent to a parallel combination of two sets of switches, diodes and inductors connected to a common filter capacitor and load [6].The switches are operated 180^0 out of phase. Assume the converter operates with duty ratio less than 50% and in continuous conduction mode (CCM).
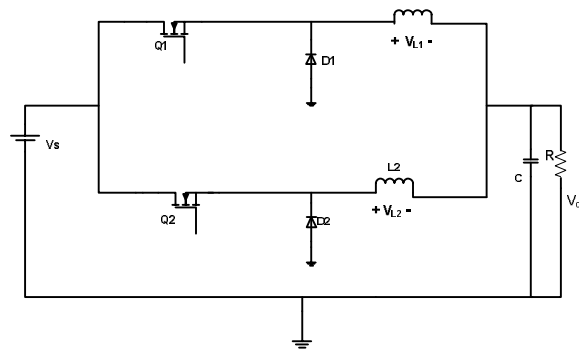

Fig. 2 circuit diagram of 2 phase IBC

A two phase IBC will operate in four different modes and is explained as follows:

Mode 1: In mode 1 switch Q1 is turned on by giving a gate pulse. At the same time switch Q2 is off. Current flows through the switch Q1, inductor L_1 and load, making current through L_1 to increase as long as Q1 is turned on. During this time current in L_2 decreases linearly. The equivalent circuit is as in Fig. 2.a. The variations of i_{L1} and i_{L2} during T_1 are given by,

$$\Delta i_{L1} = \left(\frac{V_s - V_o}{L_1}\right) T_1 \tag{1}$$

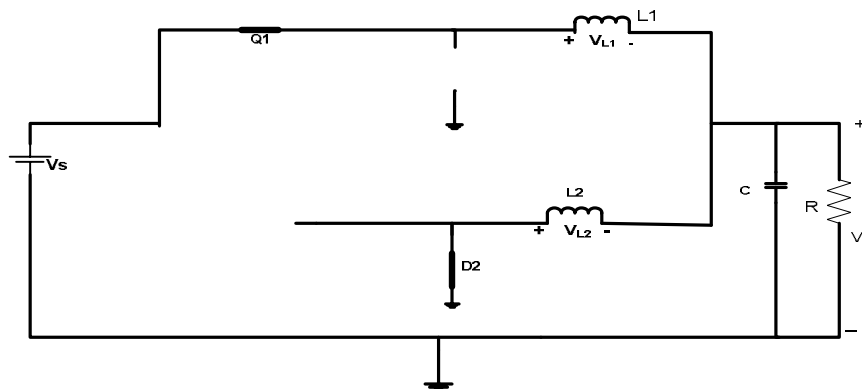$$\Delta i_{L2} = \left(\frac{-V_o}{L_2}\right) T_1 \tag{2}$$

Fig. 2(a) Equivalent Circuit of IBC in Mode 1

Mode 2: Since IBC operates with a duty cycle less than 0.5, in this mode both the switches are OFF. Diodes D1 and D2 are the conducting devices. The equivalent circuit is illustrated in Fig. 2.b.The energies stored in L_1 and L_2 are released to the load through the forward biased diodes. So i_{L1} and i_{L2} are decreased linearly. Thus the variations in i_{L1} and i_{L2} during T_2 are given by,

$$\Delta i_{L1} = \left(\frac{-V_o}{L_1} \right) T_2 \qquad (3)$$

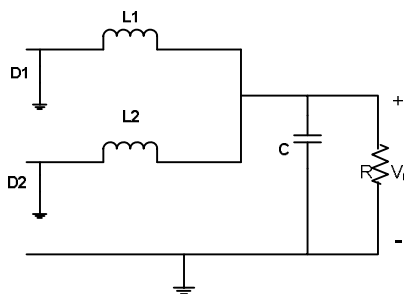$$\Delta i_{L2} = \left(\frac{-V_o}{L_2} \right) T_2 \qquad (4)$$

Fig. 2(b) Equivalent Circuit of IBC in Mode 2

Mode 3: During T_3 Q2 is turned On and Q1 turned off. The equivalent circuit is illustrated in Fig. 2.c.
The turning on of Q2 charges the inductor L_2 and since Q1 is off inductor L_1 is discharged to the load..The variations in i_{L1} and i_{L2} during T_3 are given by,

$$\Delta i_{L1} = \left(\frac{-V_o}{L_1} \right) T_3 \qquad (5)$$

$$\Delta i_{L2} = \left(\frac{V_s - V_o}{L_2} \right) T_3 \qquad (6)$$

Equation (5) shows i_{L1} linearly decreasing during T_3 since the slope is negative and a constant.
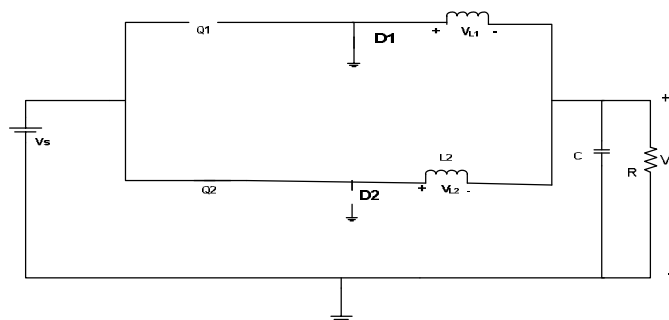

Fig. 2(c) Equivalent Circuit of IBC in Mode 3

Mode 4: The operating mode is same as mode 2. The variations in i_{L1} and i_{L2} during T_4 are given as in equation (3) and (4).
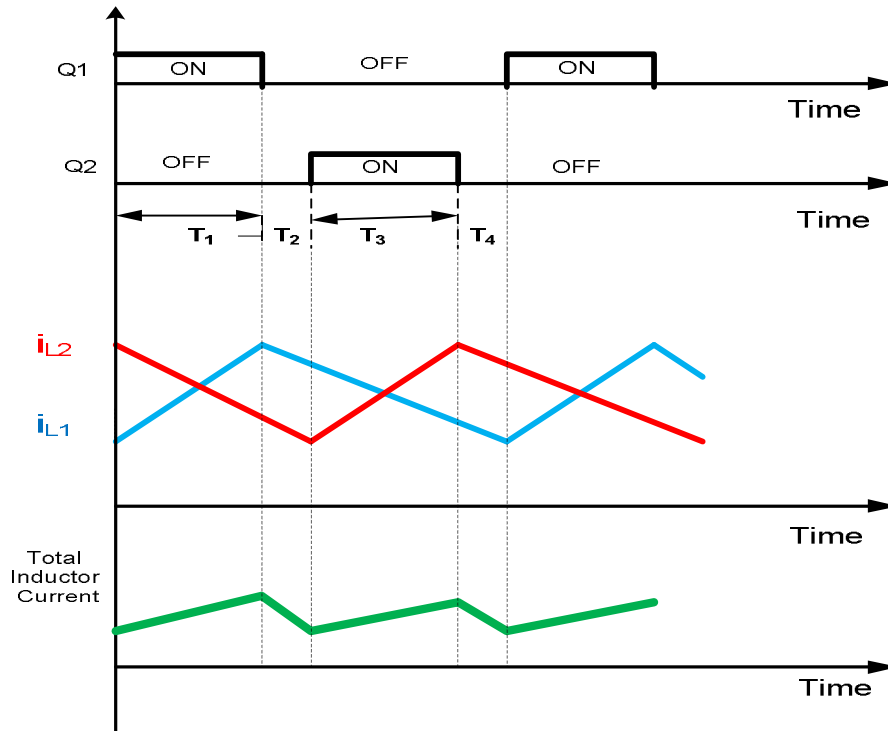
Fig.3 Inductor Current Waveforms

III. DESIGN OF IBC

Here in Interleaved converters discrete components are typically placed in parallel to split/share the current stresses. The total load current I_o Amperes is split into two power trains. So the effective load current for each power train is set to $I_o = \frac{I_o}{2}$ .The current ripple ratio for each of the two stages is represented as 'r' and the swing is $\Delta I = r \times I_o$.

a.Inductor and Output Current

Looking at the total inductor current as depicted in Fig. 3 in section II, the combined output current has a repetition rate of 2f where f is the switching frequency. Its duty cycle is not D but 2D.It is because the ON time for each converter has remained the same, but the effective time period has been cut to half. So, the effective duty cycle for the total inductor current is

$$\frac{T_{ON}}{0.5 \times T} = \frac{2 \times T_{ON}}{T} = 2D \ [8].$$

Since, peak to peak ripple in each phase is proportional to 1-D; the total current ripple in inductor is given by,

Total Inductor Ripple Current $(\Delta i_L) = \frac{1-2D}{1-D} \times Inductor\ current\ ripple\ per\ phase$

i.e, $\Delta i_L = \frac{1-2D}{1-D} \times \Delta I$

Alternatively stated,

$$\frac{I_o\ ripple\ total}{I_o\ ripple\ per\ phase} = \frac{1-2D}{1-D}\ for\ D \leq 50\%$$

The inductor design equation is similar to that of conventional Buck converter, with the exception that L here is the total inductance value.

Ie, $L = \left(\frac{V_S - V_O}{\Delta i_L 2f}\right) D$

And inductors in both the phases can be taken as L1=L2=L/2

b. OutputCapacitor

The capacitor design equation is the same as in conventional Buck converter except that instead of the switching frequency (f), the frequency here effectively doubles i.e., it becomes 2f. Thus output capacitor value is given by:

$$C = \frac{1 - 2D}{8L\left(\frac{\Delta V_o}{V_o}\right)(2f)^2}$$

Parameter	Value
Number of Phases	2
Input Voltage, Vs	12 V
Output Voltage, Vo	1.2 V
Switching Frequency, f (per Phase)	100 kHz
Per phase Ripple current , ΔI	10%
Output Current, Io	12A
Indutors per phase, L1, L2	22.5 µH
Output voltage ripple, $\frac{\Delta V_o}{V_o}$	≤ 20 mV
Output Capacitor, C	10 µF

Table.1 Design Values of Two Phase IBC

IV. CLOSED LOOP SIMULATION OF TWO PHASE IBC

Based on the design values of various parameters of IBC, a simulink model operating in open loop and closed loop is developed using Sim Power System Tool Box. To investigate the performance of IBC against variations in supply voltage , simulation is carried out and results of both steady state and transient conditions are presented

V. RESULT AND DISCUSSION

The open loop simulation result shown in Fig 4.a and 4.b throws an insight into the reduction of ripple in the total inductor current. From the steady state waveform of i_L in Fig 4.b, frequency doubling can also be observed.

In order to investigate the performance of IBC against input supply variations, sudden increase in input voltage from12V to 14 V at 0.004 s is done. Fig 5.a clearly illustrates all parameters of two phase IBC, with input source voltage variations from 12 V to 14V at 0.004 seconds and a sudden decrease in supply voltage from 14 V to 11 V in 0.007 seconds. Dynamic Response of two phase IBC with input supply variations is shown in Figs 5.b and. 5.c. Fig. 5.b gives the dynamic response against increase in voltage from 12 to 14 volts at time 0.004sec till 0.007 sec. Figure 5.c gives the dynamic response with decrease in voltage from 14 to 11 volts at time 0.007sec till 0.01 sec.
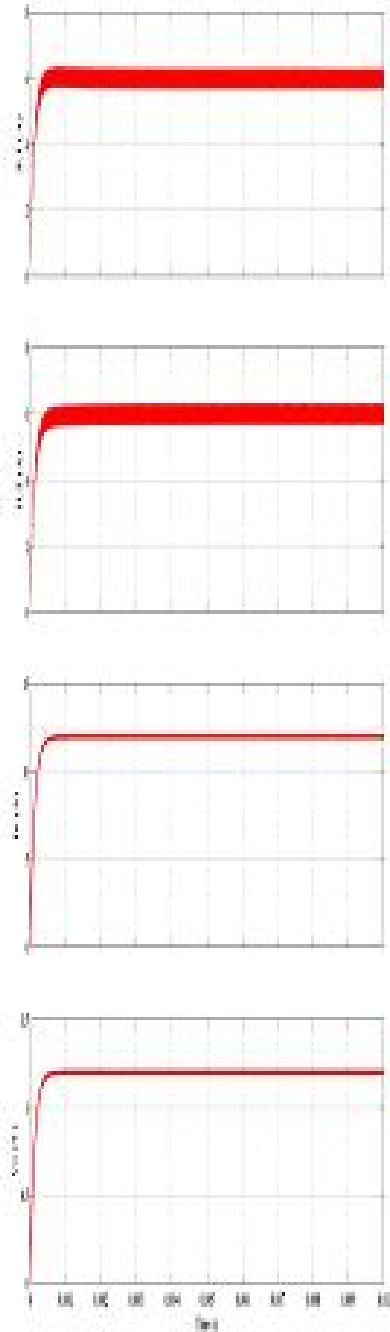
Fig 4.a Inductor Currents (i_{L1}, i_{L2}) Output Current (I_o) and Output Voltage (V_o)
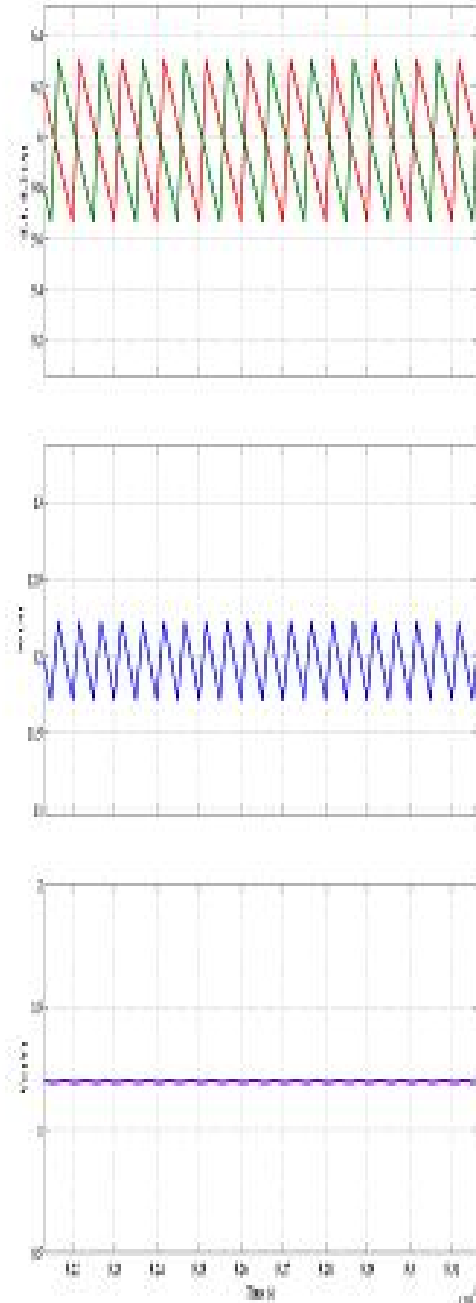
Fig 4.b Inductor Currents (i_{L1}, i_{L2}) Output Current (I_o) and Output Voltage (V_o)- Steady State
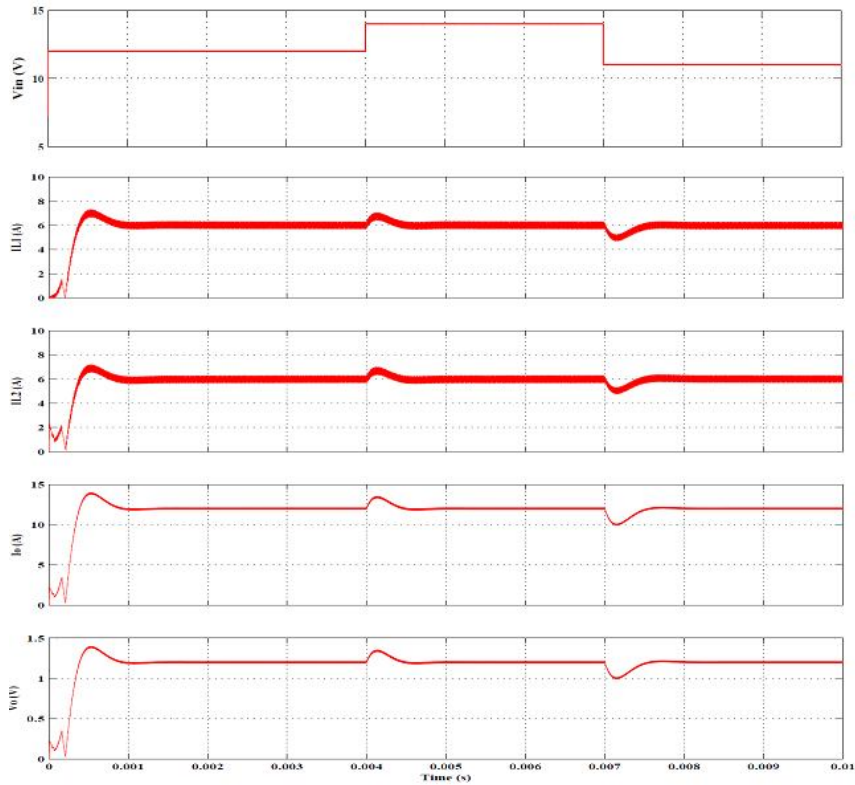
Fig 5.a Source Voltage (V_{in}),Inductor Currents (I_{L1},I_{L2}), Output Current (I_o) and Voltage Waveforms
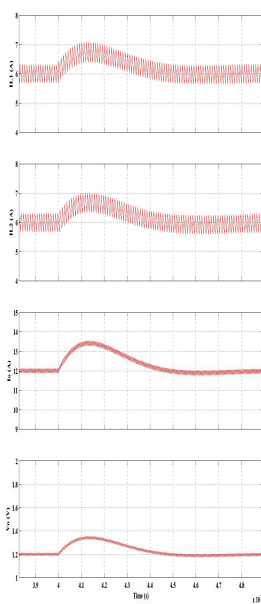

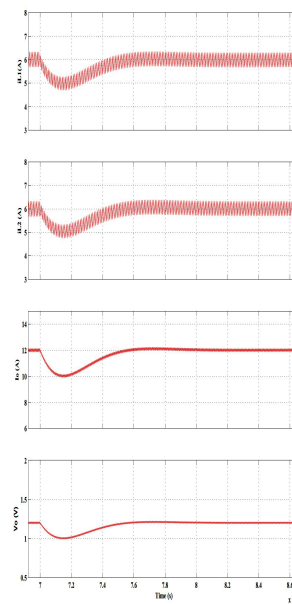Fig 5.b Dynamic Behaviour of IBC Against Sudden Increase in Input Voltage

Fig 5.c Dynamic Behaviour of IBC Against Sudden Decrease in Input Voltage

VI.CONCLUSION

An interleaved DC DC step - down converter for low output voltage and high output current suitable for VRM application is presented here. The paper explains clearly the operating principle of two phase IBC with equivalent circuits. A prototype circuit of the proposed converter with 12 V input voltage, 1. 2 V output voltage and 12 A output current is simulated and steady state ripple waveforms are obtained. The doubling of effective frequency in the total inductor cuurent is also illustrated here. The performance of IBC against sudden variations in supply voltage is also investigated and simulation results are clearly illustrated in the paper.

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