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Improved Current Fed Switched Inverter

Ishani Varghese[1], Aathira K. V[2]

PG Student [PE], Dept. of EEE, Jyothi Engineering College, Cheruthuruthy, Kerala, India[1]

Assistant Professor, Dept. of EEE, Jyothi Engineering College, Cheruthuruthy, Kerala, India[2]

ABSTRACT: This paper proposes a new topology namely Improved Current Fed Switched Inverter which is derived from the current fed switched inverter. The new topology improves the value of modulation index from its previous topology where the value of modulation index was restricted. The system is suitable for the renewable applications since it draws continuous input current. Single stage high boost inversion is also possible with the new topology. In this paper the inverter is designed for the UPS application. Pulse width modulation (PWM) control strategy is devised for the proposed inverter. The simulation is done using MATLAB/ SIMULINK and the performance parameters are also presented in this paper.

KEYWORDS: CFSI-current fed switched inverter, ZSI-Z source impedence, SBI-switched boost inverter

I.INTRODUCTION

Nowadays voltage source inverters (VSIs) are being widely used in industries due to its various advantages. Uninterruptible power supplies, solar photovoltaic (PV) and fuel-cell applications, wind power systems, hybrid electric vehicles, industrial motor drives, etc. are the main applications of voltage source inverters [1]-[2]. But only buck operation is possible with the traditional VSI [3]. As the voltage level of the PV panel is low (typically 40-50V), high boost inversion is in the small rooftop solar PV/fuel-cell applications. Either a two-stage boost-inverter structure or a step-up transformer can be used for this purpose. But, when cost, size, and efficiency of the inverter system is considered, its better to employ transformerless conversion topologies [4]-[6]. To achieve the maximum gain, conventional boost converter is to be operated at duty ratio (*D*) near unity. But the high current with small pulse width has to be suffered by the diode and output capacitor. This results in severe reverse recovery of the diode, which increases the conduction loss and produces electromagnetic interference (EMI). This problem is aggravated at high switching frequencies as the reverse recovery time (t_{rr}) of the device may be larger than the time available during (1-*D*) interval [7]. Moreover, maximum output to input voltage conversion ratio of a boost converter is about 4–5. When a VSI follows a high-gain dc-dc boost topology, which is called a two-stage conversion. The output of the dc-dc stage is voltage-stiff. EMI is the major problem associated with a two-stage dc-ac inversion. EMI may cause malfunction of the inverter and damaging of the inverter switches.

Z-source inverter (ZSI) [3] uses an "X" shaped LC impedence network between the source and the voltage source inverter. Buck and boost operations are possible with ZSI. The gain (boost factor) for ZSI is given by

$$B_{ZSI} = \frac{\hat{V}}{V_g} = \frac{1}{1-2D} \quad (1)$$

where *D* denotes the shoot-through duty ratio.

Switched boost inverter (SBI) has lesser number of passive components than ZSI by replacing the "X"-shaped impedance network with an active network [12]-[14]. SBI has only one *L*-*C* pair which leads significant reduction in the size, weight and cost. The boost factor of SBI is (1-D) times that of ZSI. It is the major drawback of SBI. Therefore, it is not suited for very high boost inversion. Both ZSI and SBI have maximum gain near $D = 0.5$.

Current fed switched inverter [18] is an inverter which has same gain as that of ZSI and same component count as that of SBI. It is a single stage inverter with high gain. Buck and boost operations are possible with CFSI. High boost operation is possible without operating at extreme duty ratio. CFSI draws continuous input current from the dc source which makes it suitable for the renewable applications. But the limitation of CFSI is the limitation in the value of its modulation index M.

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This paper proposes an improved current fed switched inverter without the limitation in the value of modulation index. In the next section, current fed switched inverter topology is reviewed. The proposed topology and its operations are described in the section III. Section IV provides the simulation results.

II.REVIEW OF THE CURRENT FED SWITCHED INVERTER TOPOLOGY

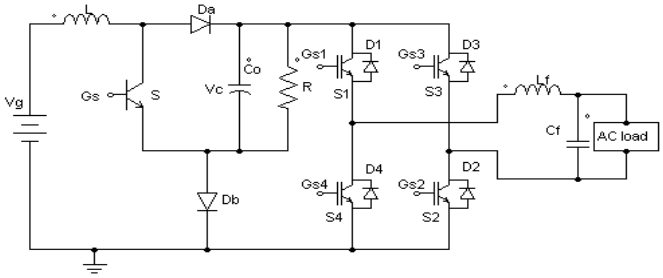

Fig 1: CFSI topology

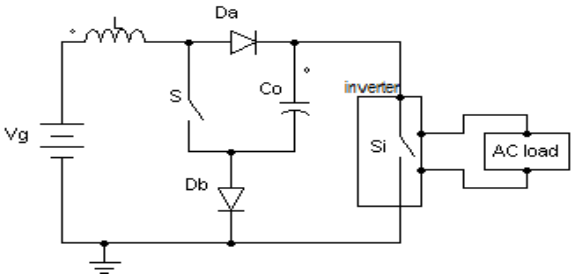

Fig 2: Simplified CFSI topology

The current fed switched inverter [18] is shown in Fig. 1. The main components of CFSI are one active switch (S), two diodes (D_a, D_b), one capacitor (C_o) and one inductor (L) and which are connected in between voltage source V_g and the inverter bridge. A low pass LC filer is used at the output of the inverter bridge to filter the switching frequency components in the inverter output voltage.

The CFSI topology inserts the shoot- through state (gating upper and lower switches of a phase leg) in its operation to boost the input voltage V_g to V_c. Therefore, the inverter is able to buck and boost the input voltage to a desired output voltage. Since the shoot-through state is present, reliability of the inverter is improved. Thus, inverter provides efficient single stage dc-ac inversion as well as buck boost power conversion. Similar to ZSI and SBI, inverter input is a switched voltage.

Consider the Fig. 2 for better understanding the operation of the inverter. Here, the H-bridge inverter is represented by a single switch Si and turning on of Si represents the shoot-through state. Initially, the capacitor C_o is charged to the voltage V_g and the initial inductor current is zero before switching signals are started. The two operation intervals of CFSI are

(1) shoot-through interval

(2) non-shoot-through interval

During shoot-through interval (D interval), switches S and Si (S_1-S_4 or S_3-S_2) are turned on and diodes D_a and D_b become reverse biased as they are now in parallel with C_o. In this interval, source V_g and capacitor C_o charge inductor L together. Equivalent circuit of CFSI in D interval is shown in the Fig 3. Equations of inductor voltage and capacitor current in D interval are given in (2) & (3).

$$v_L = V_g + V_c \quad (2)$$

$$i_c = -I_L \quad (3)$$

During non-shoot-through interval (D' interval), switches S and Si are turned off, which forces diodes D_a and D_b to turn on. Inductor charges C_o and power is delivered to the ac load through the inverter. Here, turning off switch Si denotes

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the power interval or zero interval of the inverter (turning on of switches S_1-S_2 or S_4-S_3). Fig 4 shows the equivalent circuit of CFSI in D' interval and equations of inductor voltage and capacitor current in D' interval are given in (4) & (5).

$$v_L = V_g - V_c \tag{4}$$

$$i_c = I_L - I_i \tag{5}$$

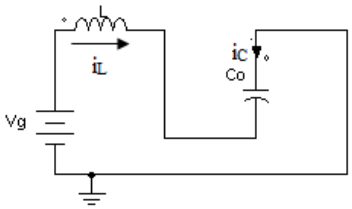

Fig 3:equivalent circuit of CFSI in D interval

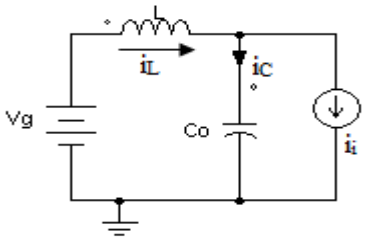

Fig 4: Equivalent circuit of CFSI in (1-D) interval

In steady state equilibrium, using inductor volt-second balance and capacitor charge-second balance, we get

$$B_{CFSI}(D) = \frac{V_c}{V_g} = \frac{1}{1-2D} \tag{6}$$

$$I_L = \frac{1-D}{1-2D} I_i \tag{7}$$

From equation (6) it is clear that this topology gives maximum gain at duty cycle close to 0.5. The equation of peak ac output is

$$V_{ACpeak} = M \times V_c = \frac{M}{1-2D} V_g \tag{8}$$

where M is the modulation index of the inverter.

The relation between duty ratio and modulation index is given by

$$D < 1 - M \tag{9}$$

So the value of M is depends on the value of D. To avoid this limitation of CFSI, the new topology is proposed in this paper which is named as Improved Current Fed Switched Inverter.

IV. IMPROVED CURRENT FED SWITCHED INVERTER

In order to improve the modulation index value, a combination of switch-diode-capacitor is connected in front of the H-bridge inverter as shown in figure 5. The shoot-through state is avoided and the switch ST is capable of doing the same function of the shoot-through state. Initially, the capacitor C_o is charged to the voltage V_g and the initial inductor current is zero before switching signals are started. The two operating intervals of the new topology are

1. D interval
2. (1-D) interval

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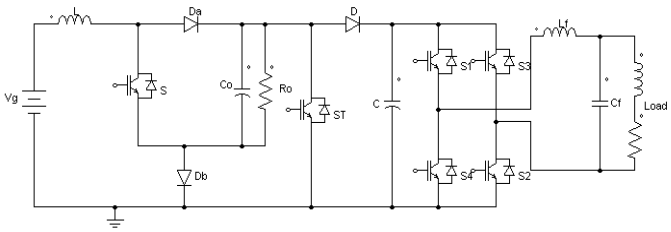

Fig 5:improved current fed switched inverter topology

During D interval, switches S and ST are ON state and D1 and D2 become reverse biased as they are now in parallel with C. In this interval, source V_g and capacitor C_o charge inductor L together. In D interval, either S1 & S2 or S3 & S4 are turned on and capacitor C is feeding the load.

During (1-D) interval switches *S* and *ST* are turned off, which forces diodes D1 and *D2* to turn on, and the inductor charges C_o and power are delivered to the ac load through the inverter. There is no zero interval is present in the inverter. The gain is same as that of CFSI.

The inductor current ripple and capacitor voltage ripple are given by

$$\Delta i_L = \frac{V_g + V_c}{L} D T_s \tag{10}$$

$$\Delta v_c = \frac{I_c}{C} D T_s \tag{11}$$

Sine PWM technique is used here for controlling the switches. Fig. 6 shows the generation of the PWM control signals of the proposed inverter. Similar to unipolar sine-triangle PWM, gate signals G_{s1} and G_{s2} are generated by comparing the sinusoidal modulation signals $V_m(t)$ and $-V_m(t)$ with high-frequency carrier signal $V_{tri}(t)$. In order to generate the switching signals for the switches S and ST by comparing V_{ST} and $-V_{ST}$ with $V_{tri}(t)$. The relation between the V_{ST} and D is given by

$$D = \left(1 - \frac{V_{ST}}{\hat{V}_{tri}}\right) \tag{12}$$

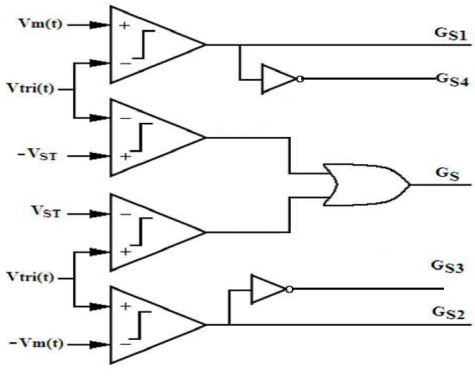

Fig 6. Generation of the PWM control signals

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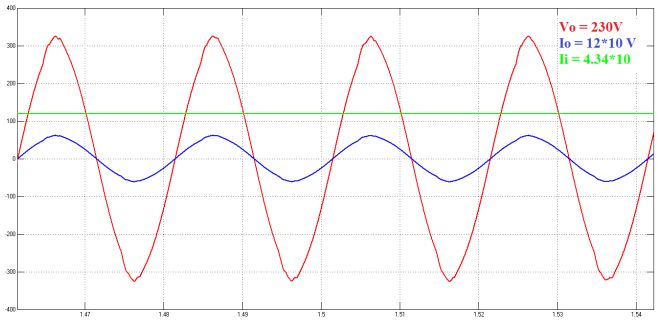

Fig 7: simulation waveforms of output voltage, output current and input current

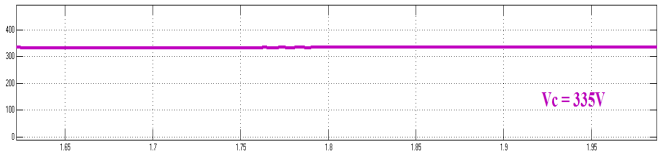

Fig 8: dc-link voltage Vc

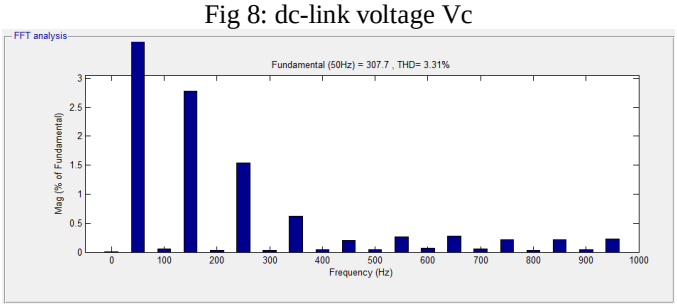

Fig 9: THD and harmonic order of output voltage

V. SIMULATION RESULTS

A 12V input voltage and 230V output voltage improved current fed switched inverter circuit with power rating of 1000VA is designed and simulated to verify the proposed concept. The simulation of the improved current fed switched inverter (fig. 6) is carried out in MATLAB/ SIMULINK. The parameters are used as follows: input voltage V_g =12V, V_{out}=230V, modulation frequency f_m=50Hz, carrier frequency f_{tri}=9.5kHz, inductor L=225µH, capacitor C_o=3878µF, output filter inductor L_f=4.6mH, output filter capacitor C_f=10µF.

Figure 7 shows the simulation result of improved CFSI. The output voltage is a sinusoidal signal with rms voltage of 230V. The value of D is 0.483 and modulation index is 0.9. The output current obtained is 4.34A. Here, the output current and input voltages are multiplied by a factor of 10 for better visibility. Figure 8 shows the voltage across the capacitor C which is called the dc-link voltage and the value of Vc is 335V.

THD and harmonic order of the output voltage is shown in fig. 9. The THD content in the output voltage of the proposed inverter is 3.31%.

VI.CONCLUSION

Proposed inverter is a single stage high-boost inverter with continuous input which is suitable for the renewable applications. Gain of the inverter is same as that of the ZSI and CFSI. Modulation index of the proposed topology varies from 0 to 1. PWM control strategy is used for the inverter. Simulations results of improved current fed switched inverter are also presented in this paper. Theoretical values are verified by the simulation results.

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