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Simulation & Comparative Analysis of Diode Clamped Multilevel Inverter Using Sinusoidal PWM

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ABSTRACT:In industrial application there are requirements of such apparatus which could work at higher power and higher voltages. Traditionally we have been using two level inverters. These inverters are found not fit in case of high voltage. Multilevel inverter become very popular for high voltage and high power application. These multilevel start from three level converters. The concepts of these multilevel converter is that to achieve high power to use a series of power semiconductor switches with several lower voltage dc source to perform the power conversion by synthesizing a staircase voltage waveform. However, the output voltage is smother with smaller harmonics. At more level inverter the system become more complex and difficult to control but total harmonic distortion (THD) become reduced. In this paper, study of five level or seven level inverter with SPWM is investigated using MATLAB.

KEYWORDS: Multilevel Inverter, Total Harmonics Distortion.

I.INTRODUCTION

One of the biggest problems in power quality aspects is the harmonic contents in the electrical system. Generally, harmonics may be divided into two types: 1) voltage harmonics, and 2) current harmonics. Current harmonics is usually generated by harmonics contained in voltage supply and depends on the type of load such as resistive load, capacitive load, and inductive load. Both harmonics can be generated by either the source or the load side. Harmonics generated by load are caused by nonlinear operation of devices, including power converters, arc-furnaces, gas discharge lighting devices, etc.

Load harmonics can cause the overheating of the magnetic cores of transformer and motors. On the other hand, source harmonics are mainly generated by power supply with non-sinusoidal voltage waveform. Voltage and current source harmonics imply power losses, Electromagnetic Interference (EMI) and pulsating torque in AC motor drives. Any periodic waveform can be shown to be the superposition of a fundamental and a set of harmonic components. By applying Fourier transformation, these components can be extracted. The frequency of each harmonic component is an integral multiple of its fundamental. There are several methods to indicate of the quantity of harmonics contents.

The most widely used measure in North America is the total harmonics distortion (THD) [3], which is defined in terms of the amplitudes of the harmonics, *Hn*, at frequency $n\omega 0$, where $\omega 0$ is frequency of the fundamental component whose amplitude of *H1* and *n* is integer. The THD is mathematically given by

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}{}^2}}{H_1}$$

The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels

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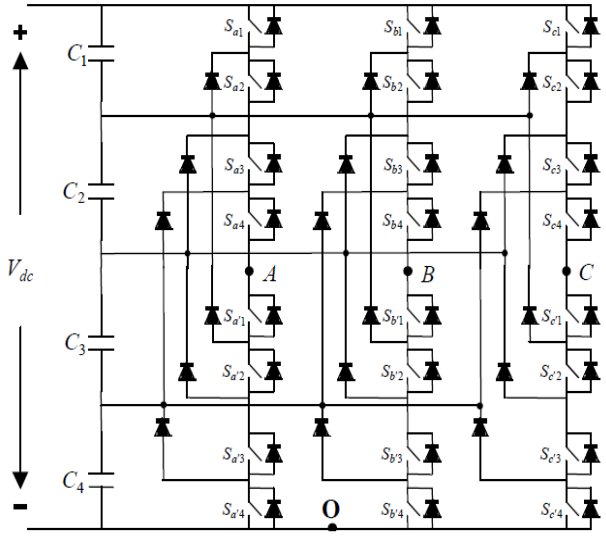
reach infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints.

II.MULTILEVEL INVERTER TOPOLOGY

The basic three types of multilevel topologies used are
1) Diode-Clamped Multilevel Inverter.
2) Flying-Capacitor Multilevel Inverter.
3) Cascaded-Inverters with Separated DC Sources.

1) Diode-Clamped Multilevel Inverter (DCMI)

The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m leveldiode-clamp inverter needs m-1 capacitors on the dc bus. A three-phase five-level diode-clamped inverter is shown in Fig. 2.1. The dc bus consists of four capacitors, i.e. C1, C2, C3, and C4. For a dc bus voltage *Vdc*, the voltage across each capacitor is *Vdc*/4, and each device voltage stress will be limited to one capacitor voltage level, *Vdc*/4, through clamping diodes. DCMI output voltage synthesis is relatively straightforward. To explain how the staircase voltage is synthesized, point O is considered as the output phase voltage reference point. Using the five-level inverter shown in Fig. 2.1, there are five switch combinations to generate five level voltages across A and O. Table 1 shows the phase voltage level and their corresponding switch states.
From Table 1, state 1 represents that the switch is on, and state 0 represents the switch is off. In each phase leg, a set of four adjacent switches is on at any given time.There exist four complimentary switch pairs in each phase, i.e., Sa1-Sa'1, Sa2-Sa'2, …, and Sa4-Sa'4



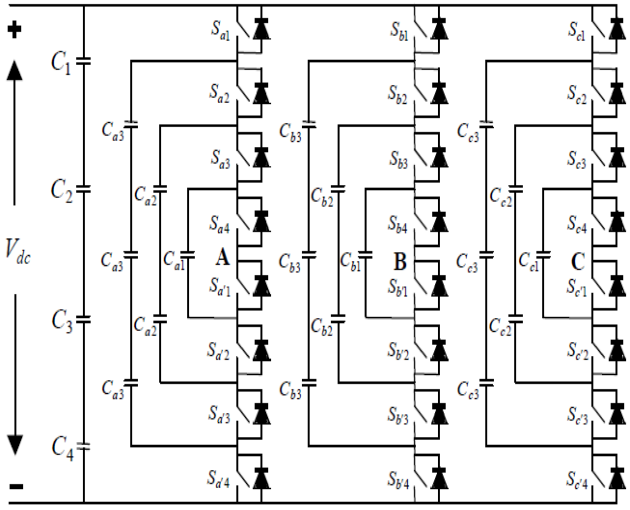


Figure 2.1 A three-phase five-level diode-clamped inverterFigure 2.2 A 3 Φ five-level flying-capacitor inverter

2) Flying-capacitor Multilevel Inverter (FCMI)

A FCMI shown in Fig. 2.6 uses a ladder structure of dc side capacitors where thevoltage on each capacitor differs from that of the next capacitor. To generate *m*-level staircase output voltage, *m*-1 capacitors in the dc bus are needed. Each phase-leg has an identical structure. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output waveform.
It is obvious that three inner-loop balancing capacitors for phase leg A, Ca1, Ca2, and Ca3 are independent from those for phase leg B. All phase legs share the same dc link capacitors, C1-C4. Table 2 shows a possible switch combination of the voltage levels and their corresponding switch states.

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Output V_{AO}	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3Vdc/4$	0	1	1	1	1	0	0	0
$V_3=Vdc/2$	0	0	1	1	1	1	0	0
$V_2=Vdc/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

Output V_{AO}	Switch State							
	S_{a1}	S_{a2}	S_{am-1}	S_{am}	$S_{a'1}$	$S_{a'2}$	$S_{a'm-1}$	$S_{a'm}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3=V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2=V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

Table 1 Diode-clamped five-level inverter voltageTable 2 A possible switch combination of the voltage levels and their switch states.levels and their corresponding switch states.

.In fact, there is more than one combination to produce output voltages V2, V3, and V4. That makes the FCMI more flexibility than DCMI. Table 2, however, shows only one possible combination.

3) Multilevel Inverter Using Cascaded-Inverters with Separated DC Sources

The last structure introduced in this thesis is a multilevel inverter, which uses cascaded inverters with separate dc sources (SDCSs). The general function of this multilevel inverter is the same as that of the other two previous inverters. The multilevel inverter using cascaded-inverter with SDCSs synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from either batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clampingdiodes or voltage balancing capacitors. A single-phase m-level configuration of such an inverter is shown in Fig 2.3.

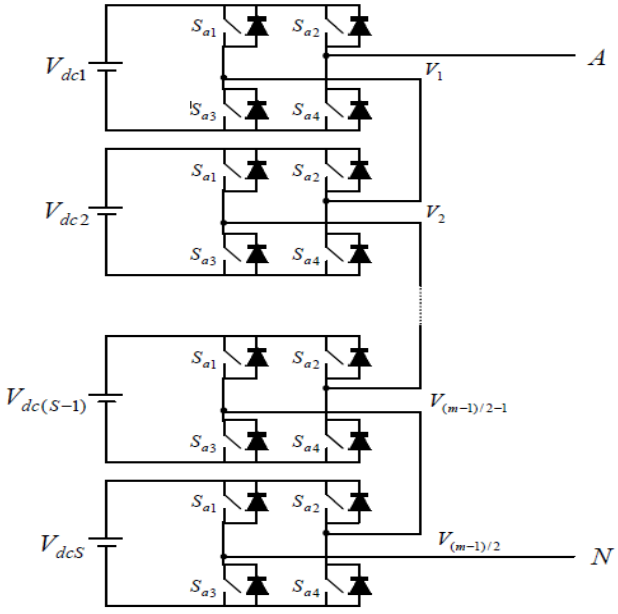

Figure 2.3 Single-phase structure of multilevelcascaded inverter

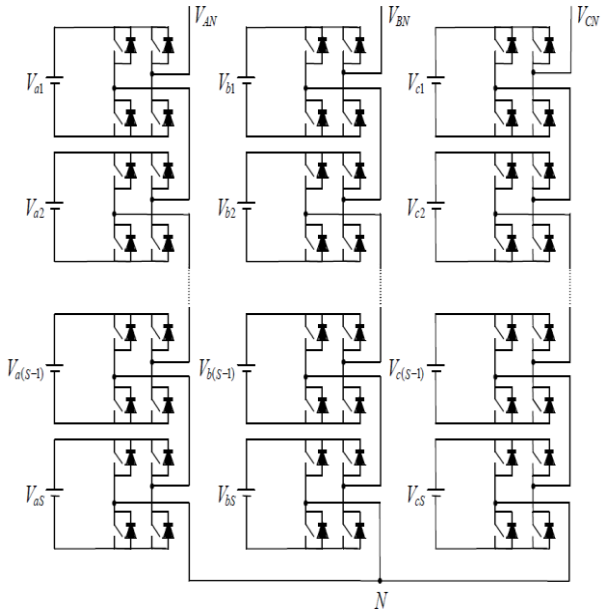

Figure 2.4: A general three-phase Wye-configuration cascaded-inverters based inverter.

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Vol. 4, Issue 5, May 2015

Each SDCS is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. By different combinations of the four switches, S1-S4, each inverter level can generate three different voltage outputs, *+Vdc*, *-Vdc*, and zero. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. Note that the number of output phase voltage levels is defined in different way from those of two previous inverters. In this topology, the number of output phase voltage levels is defined by $m = 2s+1$, where s is the number of dc sources.

A 7-level cascaded-inverters based inverter, for example, will have three SDCSsand three full-bridge cells. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter level, which will be proposed in section IV.For a three-phase system, the output voltage of the three cascaded inverters can be connected in either wye or delta configuration. For example, a wye-configured m-level inverter using cascaded-inverters with s separated capacitors is illustrated in Fig. 2.4.

III. SIMULATION & RESULT

FIVE-LEVEL DCMI

The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m-level diode-clamp inverter needs m-1 capacitors on the dc bus. A three-phase five-level diode-clamped inverter is shown in Fig. 3.1. The dc bus consists of four capacitors, i.e., C1, C2, C3, and C4. For a dc bus voltage Vdc, the voltage across each capacitor is Vdc/4, and each device voltage stress will be limited to one capacitor voltage level, Vdc/4, through clamping diodes. DCMI output voltage synthesis is relatively straight forward.

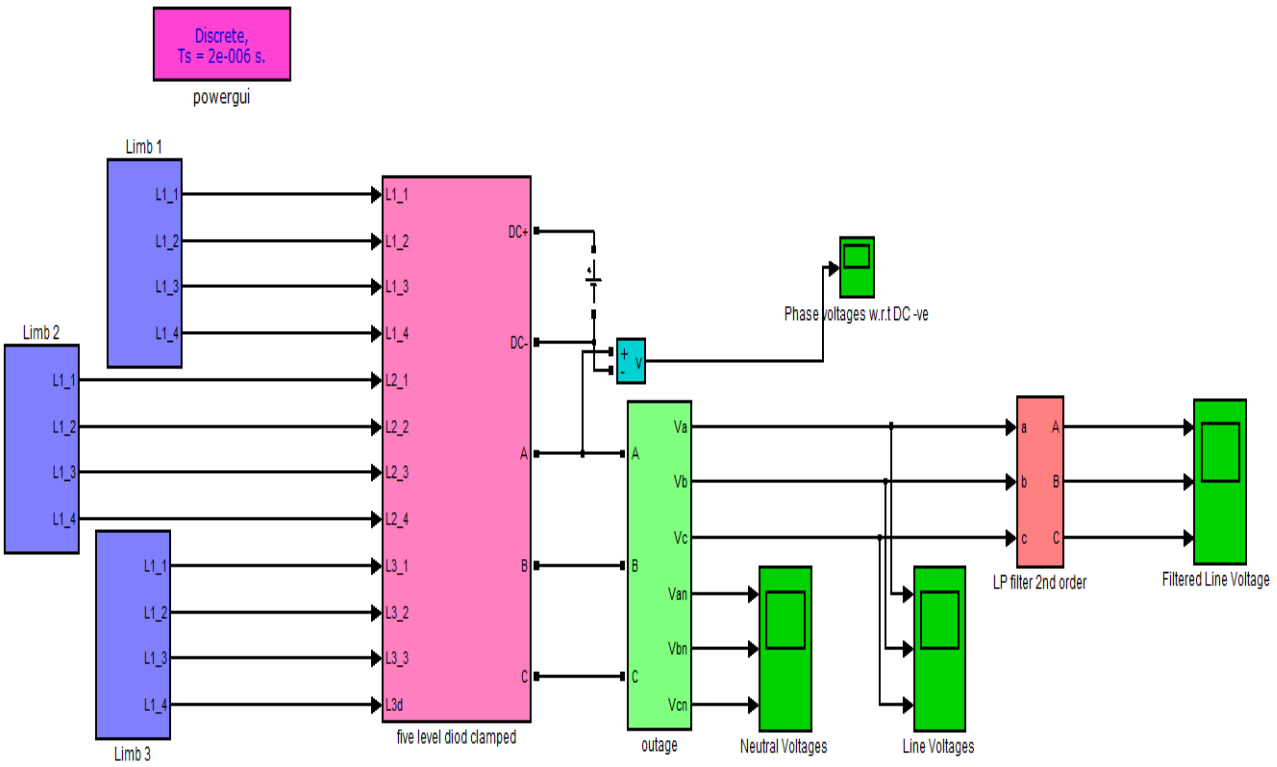

Fig. 3.1 Simulation circuit (5-level DCMI)

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Output V_{AO}	Switch State							
	Sa1	Sa2	Sa3	Sa4	Sa' 1	Sa' 2	Sa' 3	Sa' 4
$V_5=V_{dc}$	on	on	on	on	Off	off	off	off
$V_4=3V_{dc}/4$	off	on	on	on	On	off	off	off
$V_3=V_{dc}/2$	off	off	on	on	On	on	off	off
$V_2=V_{dc}/4$	off	off	off	on	On	on	on	off
$V_1=0$	off	off	off	off	On	on	on	on

Table 3: 5-Level DCMI voltage levels & their switching States

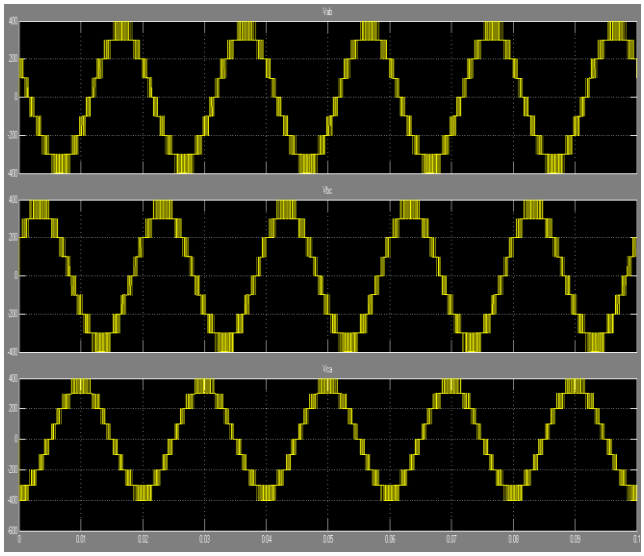

Fig.3.2 Line to line voltage waveform

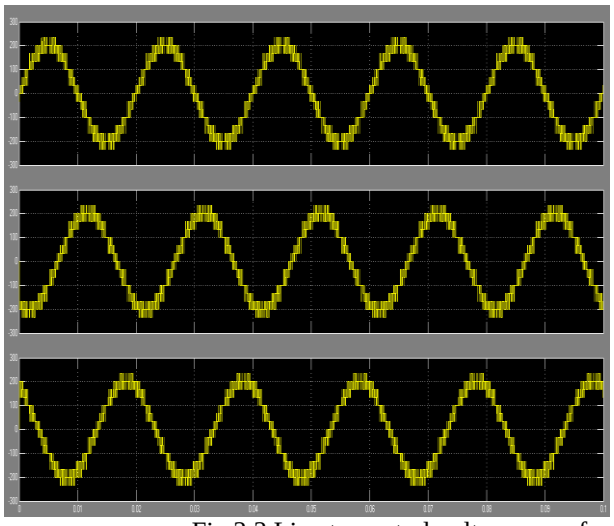

Fig.3.3 Line to neutral voltage waveform

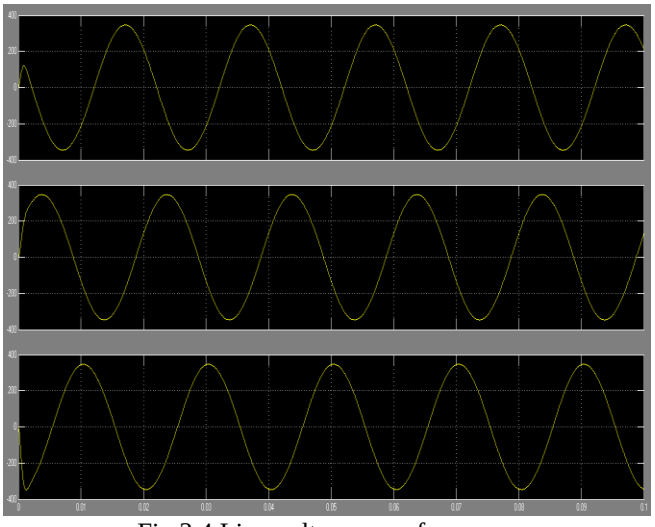

Fig.3.4 Line voltage waveform

SEVEN-LEVEL DCMI

A three-phase seven-level diode-clamped inverter is shown in fig.3.5. Each phase is constituted by 12 switches (six switches for upper leg and six switches for lower leg). Switches Sa1 through Sa6 of upper leg form complementary pair with the switches Sa1' to Sa6' lower leg of the same phase.

The complementary switch pairs for phase 'A' are (Sa1, Sa1'), (Sa2, Sa2'),(Sa3, Sa3'),(Sa4, Sa4'),(Sa5, Sa5'),(Sa6, Sa6') and similarly for B and C phases. Clamping diodes are used to carry the full load current.

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Sa_1	Sa_2	Sa_3	Sa_4	Sa_5	Sa_6	V_{AB}	V_{AO}
1	1	1	1	1	1	V_{dc}	V_{dc}
0	1	1	1	1	1	$V_{dc}/6$	$2V_{dc}/3$
0	0	1	1	1	1	$2V_{dc}/6$	$V_{dc}/3$
0	0	0	1	1	1	$3V_{dc}/6$	0
0	0	0	0	1	1	$4V_{dc}/6$	$-V_{dc}/3$
0	0	0	0	0	1	$5V_{dc}/6$	$-2V_{dc}/3$
0	0	0	0	0	0	0	$-V_{dc}$

Table 4:Pole Voltage and Line Voltage of a Seven Level Inverter

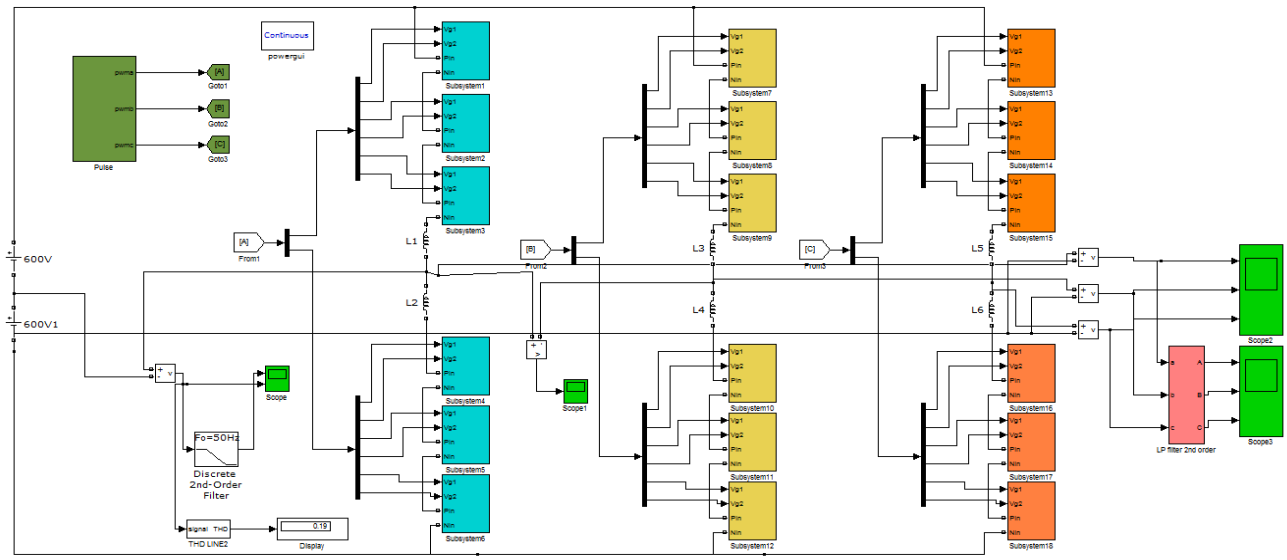

Fig. 3.5 Simulation circuit of three-phase seven-level diode-clamped inverter

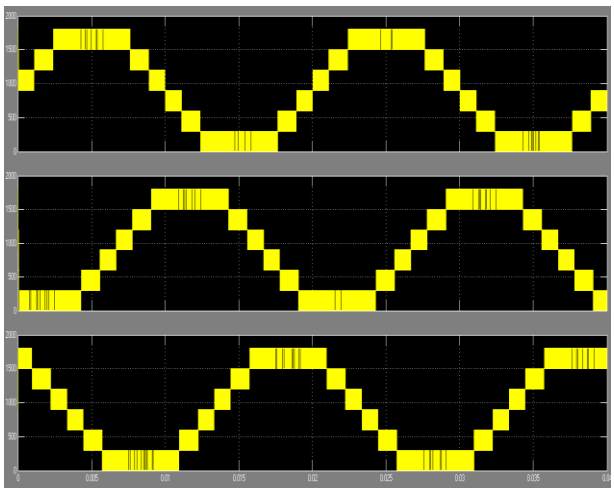

Fig 3.6 Three phase waveform of line to line voltage

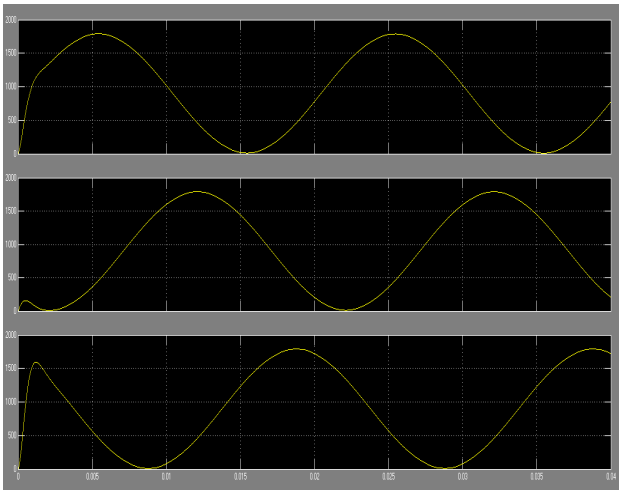

Fig 3.7 Line to Line filter voltage waveform

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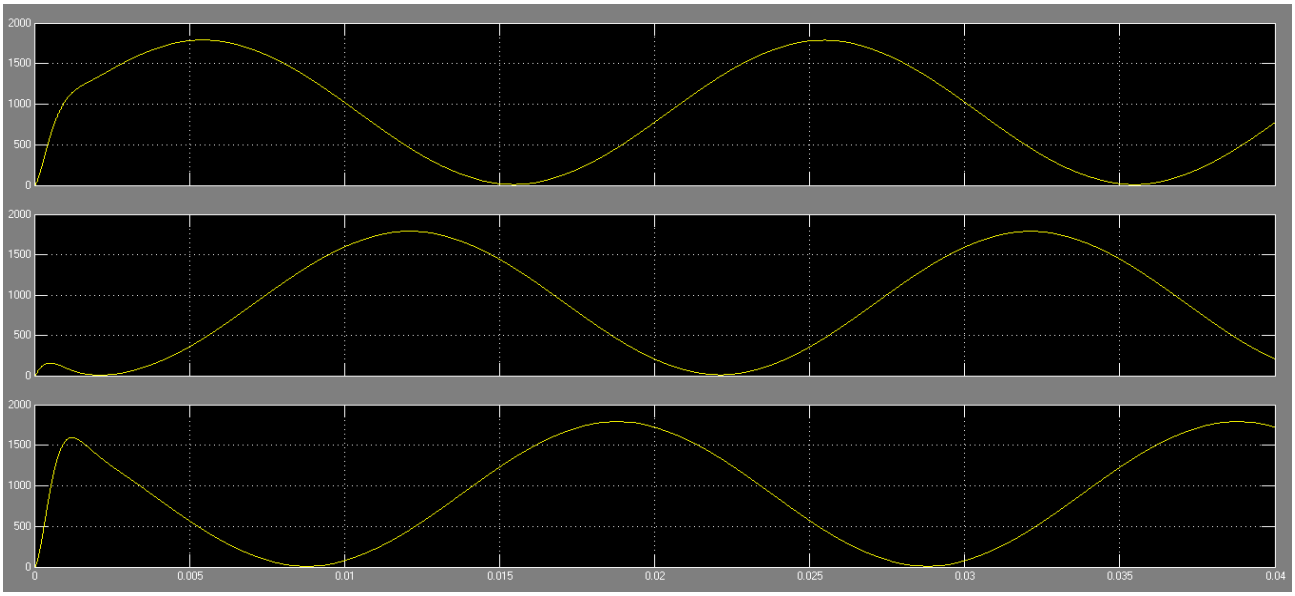

Fig 3.8 Line to Line filter voltage waveform

TABLE-III

Diode Clamped Multilevel Inverter	THD%
Five Level	0.28
Seven Level	0.19

Comparison of THD Level.

VI.CONCLUSION

In this paper, the multilevel topology is presented for industrial application. The multilevel inverters and percentage of total harmonic distortions of several levels of inverter are simulated and compared. The simulated results are 0.28 % THD and 0.19 % THD of five level and seven level inverters respectively. As the number of levels increases the harmonic distortion also decreases.

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BIOGRAPHY

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