ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

A Single Source Five Level Inverter with Reduced Number of Switches

Chippy Venugopal[1], Shinosh Mathew[2]

PG Scholar, Dept. of EEE, Amal Jyothi College of Engineering, Kanjirapally, Kerala, India [1]

Assistant Professor, Dept. of EEE, Amal Jyothi College of Engineering, Kanjirapally, Kerala, India [2]

ABSTRACT:A single phase five level inverter with a dual reference single carrier Pulse Width Modulated (PWM) control scheme is presented. The inverter is capable of producing five levels of output voltage levels (Vdc, Vdc/2, 0, −Vdc/2, −Vdc) from the dc supply voltage. For this, the proposed multilevel inverter needs a single dc voltage source with a series connection of two capacitors, a bidirectional switch formed with four diodes and a switch, and an H-bridge cell. The proposed approach helps in reducing the number of independent dc voltage sources and number of switches as compared with conventional circuits

KEYWORDS: Multilevel Inverter (MLI), Pulse Width Modulation, Total Harmonic Distortion (THD).

I.INTRODUCTION

Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage applications. Researches are going on to improve their capabilities further through optimized control techniques, and to minimize both component count and manufacturing cost. The multilevel inverter has been implemented in various applications, such as motor drives, power conditioning devices, renewable energy generation and distribution. PWM inverters can simultaneously control output voltage, frequency and it can reduce the amount of harmonics in output current which results in better THD content.

Several multilevel topologies have been developed, but as the output voltage levels increases, it also increases the number of switches, number of independent dc sources, switching stresses, losses, voltage unbalancing across capacitors etc.
Half and Full bridge inverters requires large input and output filters, lower voltage operating capability, harmonic distortion is high, high Electro Magnetic Interference (EMI) [1]. The mainly used MLI topologies are flying capacitor, diode clamped and H-bridge converter with separate DC sources. Diode clamped MLI requires large number of diodes as no: of level increases. Flying capacitor MLI uses a large no: of capacitors to hold voltages. Cascaded H bridge MLI requires least no: of components but needs separate dc voltage sources for each H bridges [2]. Among conventional multilevel inverters, cascaded H-bridge multilevel inverter (CHB) is one of the best approaches to increase the number of output voltage levels. As CHB increases H-bridge cells, it also increases the number of switches and also independent dc input voltage sources. One of the solutions to reduce the number of components in CHB is to use asymmetrical dc voltage sources. But the main disadvantage of asymmetric cascaded H-bridge inverter is the requirement of asymmetric DC sources for its operation. Using H Bridge with Multiple Transformer reduces the number of switches and provides proper isolation. It also uses a combination of asymmetrical voltage sources to synthesize multilevel output voltages. This technique employs only a single dc voltage source. But it uses two low frequency transformers and thus makes the system bulky and costly [3]. In case of CHB with single voltage source, capacitor acts as a DC power source. This method requires a complete monitoring of capacitor charging and discharging [4]. Modular multilevel converter was introduced in [5]. Although it is very easy to be extended to higher levels, it increases the number of bulky capacitors and switches as level increases. Most of the commonly used methods employ series connected capacitors, as it reduces the use of independent dc sources.

The different PWM techniques which are commonly used are Sinusoidal PWM (SPWM), Space Vector PWM (SVPWM), and Selective Harmonic Elimination PWM (SHEPWM). Out of which, SPWM is the commonly used. It is

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

of two types- Multi-carrier PWM and Multi-reference PWM. Multi-carrier PWM technique is of two types- level shifted and phase shifted. Level shifted PWM techniques involve Phase Disposition PWM (PDPWM), Phase Opposition Disposition PWM and Alternate Phase Opposition Disposition PWM. Multi-reference single carrier SPWM helps in reducing the THD content in output voltage, so it is used here over multi-carrier single reference SPWM [6].
In this paper a single sourced five level inverter with less number of components is introduced. A dual reference single carrier PWM technique is used and thus reduces the THD in output voltage. To verify the validity of the proposed approach, computer-aided simulations are performed using MATLAB/SIMULINK.

II. LITERATURE SURVEY

Multilevel converters have received increased interest recently for high-power and medium-voltage applications. They can synthesize switched waveforms with lower levels of harmonic distortion compared to a two-level converter. The multilevel concept is used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. The most attractive features of multilevel inverters are as follows [2]:

1) They can generate output voltages with extremely low distortion and lower dv/dt.
2) They draw input current with very low distortion.
3) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
4) They can operate with a lower switching frequency.

By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped); capacitor- clamped (flying capacitors); and cascaded multicell with separate dc sources. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulsewidth modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM).

Three major types of MLIs applied in industrial applications are flying capacitor, diode clamped and H-bridge converter with separate DC sources.Flying capacitor type multilevel inverters are notwidely used because of its bulk nature due to the presence of alarge number of capacitors, diode clamped multilevel invertershave the highest cost of implementation compared to flyingcapacitor and cascaded H-bridge multilevel inverters. CascadedH-bridge multilevel inverter is simpler than diode clamped andflying capacitor multilevel inverter topologies because of someadvantages such as automatic voltage sharing, smallerswitching stresses, low switching redundancy and requirementof least number of components, no high rated capacitors and diodes. Main disadvantage of cascaded H-bridge multilevel inverteris that for increasing the number of levels of output voltage,number of DC input sources is to be increased, since for theoperation of cascaded H-bridge multilevel inverters separate DC sources are required for each H-bridge and at the sametime number of switches is also increasing. For example, to obtain a five levelinverter output, number of input DC sources required is twoand the number of switches is eight, this is not soadvantageous. These drawbacks can be overcome by using asingle source multilevel inverter with reduced number ofswitches which is suitable for multi-string solar panelapplications.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

III.PROPOSED FIVE LEVEL PWM INVERTER

A. CIRCUIT CONFIGURATION

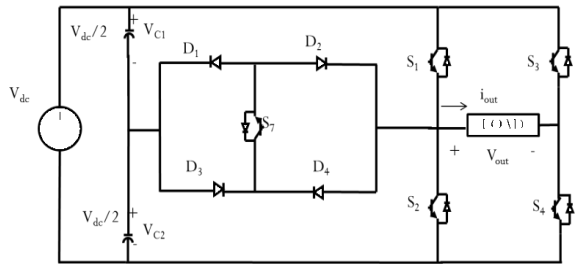

Fig. 1. Circuit configuration of the proposed 5-level PWM inverter.

The proposed five level inverter shown below has a conventional H bridge circuit, an auxiliary circuit and two capacitors connected in series. It is assumed that all the components are ideal. The voltage across each capacitor is Vdc/2. Thus the 5 levels of output voltages, Vdc, Vdc/2, 0, - Vdc/2, - Vdc are obtained. The H bridge cell provides the output voltage levels Vdc and - Vdc and other levels are obtained by the auxiliary circuit.

B. GENERATION OF OUTPUT LEVELS

The required five output voltage levels are generated as follows:

1) Level Vdc: S2 is in ON state, connects the load positive terminal to Vdc, and S5 is in ON state, connects the load negative terminal to ground. The other switches are OFF thus the applied voltage to the load terminals is Vdc. Fig. 2 shows the current paths at this stage.

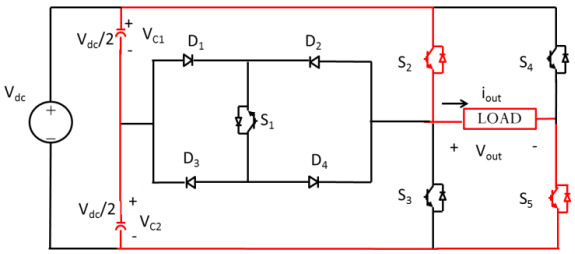

Fig.2. Generation of *Vdc* voltage level and load current path

2) Level Vdc/2: The auxiliary switch, S1 and S5 is ON and the other controlled switches are OFF; the voltage applied to the load terminals is Vdc/2. Fig. 3 shows the current paths at this stage.

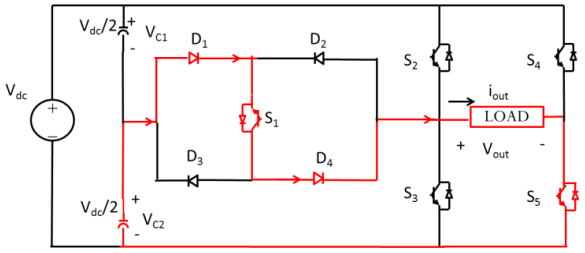

Fig.3. Generation of Vdc/2 voltage level and load current path

3) Zero output: The two main switches S3 and S5 are ON, short-circuiting the load. All other controlled switches are OFF; the voltage applied to the load terminals is zero. Fig. 4 shows the current paths at this stage.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

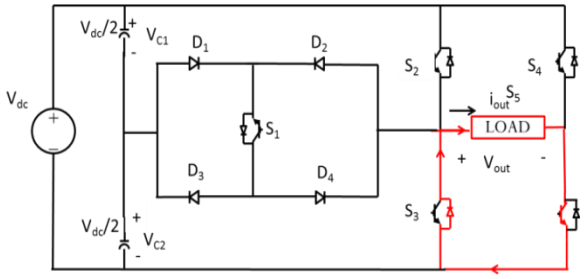

Fig.4. Generation of zero voltage level and load current path

4) Half-level negative output, Vdc/2: The auxiliary switch, S1 is ON and S4 is ON and the other controlled switches are OFF; the voltage applied to the load terminals is - Vdc/2. Fig. 5 shows the current paths at this stage.

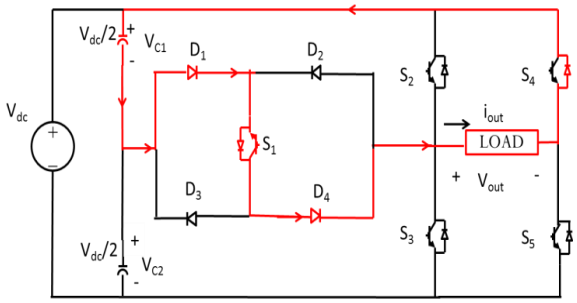

Fig.5. Generation of *-Vdc/2* voltage level and load current path

5) Maximum negative output: S4 is ON and S3 is ON and the other controlled switches are OFF; the voltage applied to the load terminals is - Vdc. Fig. 6 shows the current paths at this stage.

6)

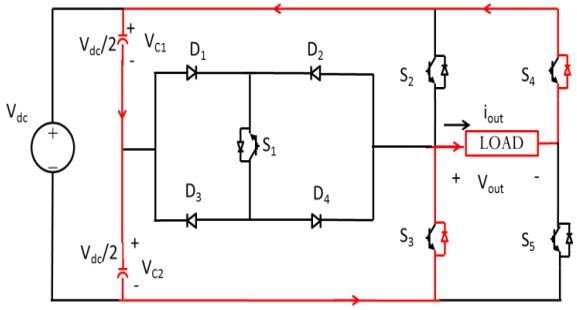

Fig.6. Generation of *-Vdc* voltage level and load current path

IV.CONTROL SCHEME

A single carrier multi reference PWM technique is used to generate the switching signals. A five level inverter requires four high frequency carrier signals and one reference signal for a multi-carrier SPWM. A multi-reference single carrier SPWM requires two reference signals and single high frequency carrier signal for obtaining a five level inverter. Here both the reference signals are compared with a carrier signal. The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

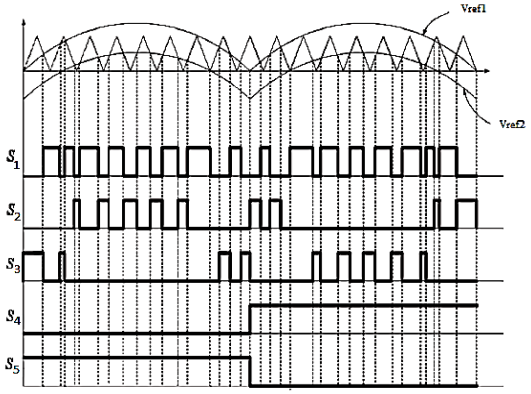

Fig.7. Switching pattern for generating 5-level PWM output voltage.

Two reference signals V_{ref1} and V_{ref2} will take turns to be compared with the carrier signal at a time. If V_{ref1} exceeds the peak amplitude of the carrier signal $V_{carrier}$, V_{ref2} will be compared with the carrier signal until it reaches zero. At this point onwards, V_{ref1} takes over the comparison process until it exceeds $V_{carrier}$. This will lead to a switching pattern as shown in Fig.3. Switches S1- S3 will be switching at the rate of the carrier signal frequency while S4 and S5 will operate at a frequency equivalent to the fundamental frequency.

V.SIMULINK MODEL AND SIMULATION RESULTS

In order to verify the proposed inverter, simulations were performed by using MATLAB/SIMULINK. Fig.8 shows the SIMULINK model of the 5 level inverter. The input voltage applied is 100V and the two capacitors are used for dividing the voltage into 50V each. Frequency of output voltage is set to 50Hz.

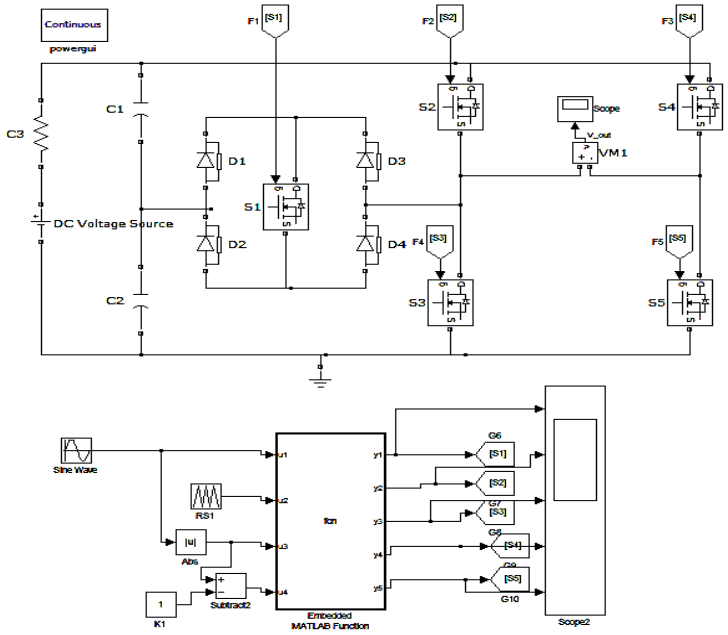

Fig.8. Simulink Model of the Proposed System

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

Fig.9. shows simulation results of the output voltage with the proposed switching scheme. The output voltage shows exact 5 levels.

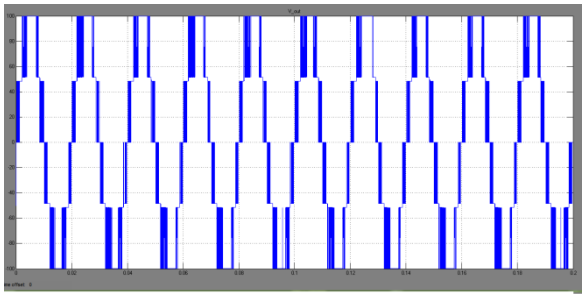

Fig.9. Output Voltage of Proposed Five Level Inverter

THD of the output voltage is measured and found as shown in theFig.10. THD is found to be less when compared with conventional topologies. Also the number of components required for getting five levels in the output voltage is less as compared with the conventional configurations.

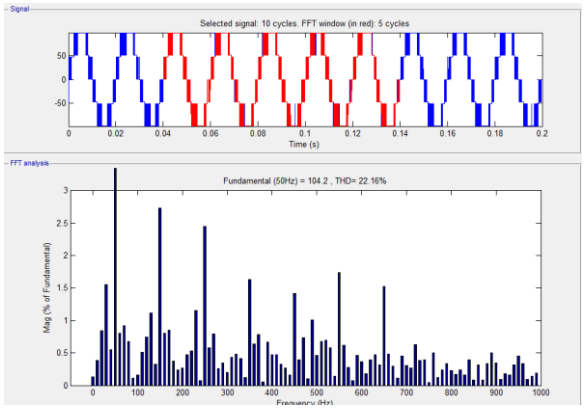

Fig.10. Output Voltage of Proposed Five Level Inverter

Thus the output of the proposed five level inverter is verified using MATLAB/ Simulink. THD of the output voltage is found to be 22.16%, which is less when compared to conventional five level inverters.This chapter deals with the Simulink models and simulation results of the proposed system. The output voltage and current waveform for the single source five level inverter obtained is shown.

VI. HARDWARE IMPLEMENTATION

Main parts of the system are as follows:

1) Power supply unit
2) PIC 16F877A Microcontroller
3) Gate Driver Circuit
4) Single Source Five Level Inverter

The power supply unit is used to generate regulated power supply. 7805 regulator IC is used to obtain +5 V output. A capacitor is used to eliminate ripples. An LED is connected to the circuit to check whether it is properly working.

PIC is a family of microcontrollers made by Microchip Technology, the name PIC initially referred to "Peripheral Interface Controller". PIC microcontrollers use Harvard architecture. Here PIC 16F877A is used as the controller and pulses to the gate of every switch is generated using this microcontroller. The gate pulses generated using the PIC Microcontroller is having only a 5V magnitude. So in order to convert it into the required voltage level a gate driver

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

circuit is required.Gate driver circuit used here uses an optocoupler MCT2E, npn transistors BC547 and BC557 and resistors. The gate driver circuit for MOSFETs in the inverter is shown below in Fig.11.

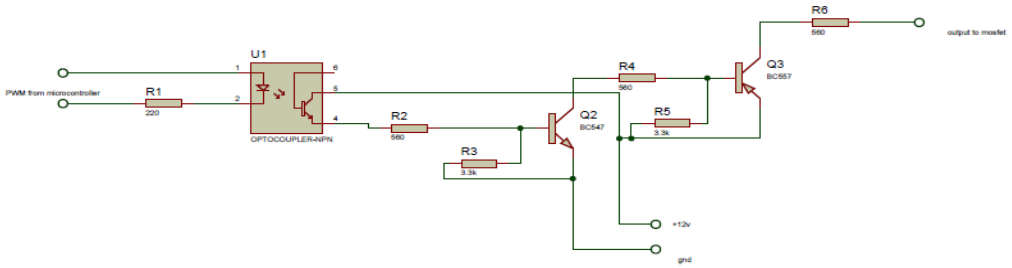

Fig.11. Circuit diagram of a single gate driver circuit

Complete circuit diagram for hardware setup is shown below in Fig.12. Fig.13 shows the output voltage waveform for single source five level inverter.

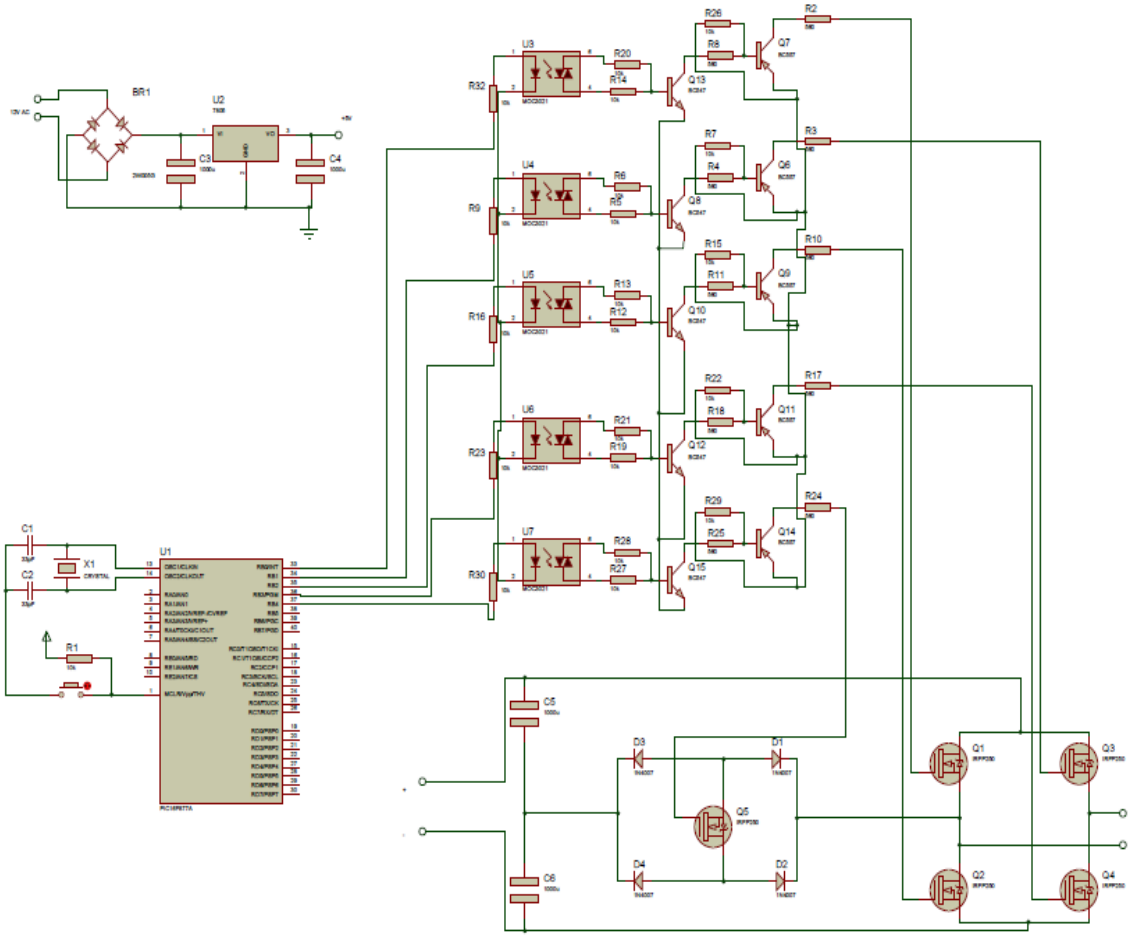

Fig.12. Complete Circuit Diagram for hardware

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

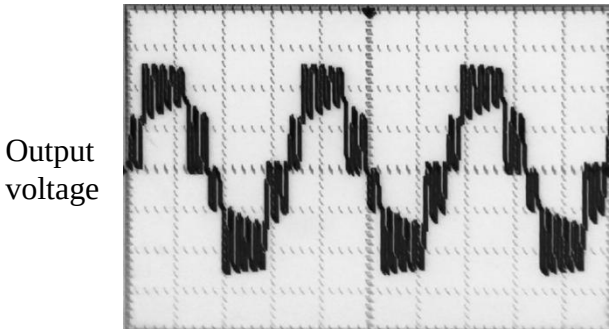

Fig.13. Output Voltage waveform obtained in Digital Signal Oscilloscope

The hardware setup for the entire system is developed. The experimental results are tested by using a digital storage oscilloscope. From the experimental results it is clear that the hardware setup is working and produces the desired output.

VI. CONCLUSION

Here a multilevel PWM inverter is proposed which can effectively increase output voltage levels with a single dc voltage source. To generate a 5-level output voltage, the proposed multilevel inverter requires a single dc voltage source with two series connected capacitors, one bidirectional switch formed with four diodes and an H-bridge cell. After analyzing theoretically, computer-aided simulations are performed to verify the validity of the proposed approach. The proposed single source inverter has advantages like single source, lesser number of switches, low switching stress. The PWM control technique used here with dual reference single carrier sinusoidal PWM helps in reducing the THD. Thus the proposed 5-level PWM inverter can be a good candidate, which can be used in place of conventional PWM inverters in the power rating of a common use.

REFERENCES

[1] Puyal. D, Barragan. L. A, Acero. J, Burdio. J. M and Millan. I, "An FPGA-based digital modulator for full or half-bridge inverter control," IEEE Transactions on Power Electronics., 21(5), 1479–1483, Sept. 2006.

[2] J. Rodríguez, Jih-Sheng Lai, and F. Z. Peng., "Multilevel Inverters: A Survey of topologies,Controls, and pplications," IEEE Transactions on Industrial Electronics., Vol. 49, No. 4, August 2002.

[3] Ekta Desai, Nilesh Shah, "Comparative Analysis of Multilevel Inverter Topologies for Photovoltaic System" Nirma University International Conference on Engineering (NUiCONE), 2013.

[4] K.N.V.Prasad, G.R.Kumar, T.V.Kiran, G.S.Narayana, "Comparison of Different Topologies of Cascaded H-Bridge Multilevel Inverter", International Conference on Computer Communication and Informatics, January 2013.

[5] Kui Wang, Yongdong Li, Zedong Zheng, Lie Xu, "Voltage Balancing and Fluctuation-Suppression Methods of Floating Capacitors in a New Modular Multilevel Converter," IEEE Transactions on Industrial Electronics, vol. 60, no. 5, pp. 1943-1954, 2013.

[6] B. P. McGrath and D.G.Holmes, "Multicarrier PWM Strategies for Multilevel Inverters," IEEE Transactions on Industrial Electronics, Vol. 49, No. 4, August 2002.

[7] Nasrudin A. Rahim, Krismadinata Chaniago and Jeyraj Selvaraj, "Single-Phase Seven-Level Grid-Connected Inverter for Photovoltaic System," IEEE Transactions on Industrial Electronics, Vol. 58, No. 6, June 2011.

[8] Youhei Hinago, Hirotaka Koizumi, "A Single-Phase Multilevel Inverter Using Switched Series/Parallel DC Voltage Sources," IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2643-2650, Aug. 2010.

[9] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Perez, "A Survey on Cascaded Multilevel Inverters", IEEE Transaction on Industrial Electronics, Vol. 1, No. 1 December 2009.

[10] K.Biju and R.Ramchand, "Modelling and Simulation of Single phase five level inverter fed from renewable energy sources",International Conference on Microelectronics, Communication and Renewable Energy,2013.

[11] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for gridconnected photovoltaic systems," IEEE Transactions on Industrial Electronics, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[12] Gerardo Ceglia, Víctor Guzmán, Carlos Sánchez, Fernando Ibáñez, Julio Walter, andMaría I. Giménez, "A New Simplified Multilevel Inverter Topology for DC–AC Conversion," IEEE Transactions on Power Electronics, Vol. 21, No. 5, September 2006.

[13] N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," IEEE Transactions Industrial Electronics, vol. 57, no. 6, pp. 2111–2123, Jun. 2010.