Integrated Power Converter for Distributed Generation

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ABSTRACT: Distributed generation systems with the using of the renewable sources increasingly, application of the distributed generation (DG) in the distribution system acquired more attention. After the power system faults, distribution system which contains many DGs would usually cut off the DGs from the distribution system at the joint where the DGs connected into the system term less. However, considering the enlarge scale and the capability of the DGs, also with the improving ratio of the DG to all generator, cut off the DGs from the distribution system directly without analysis of the splitting point detailed after the faults occurs in the power system, which cannot improve the reliability of the distribution system and made the effect of the DG at a discount. Distributed generation systems also include local energy sources, storages, and loads. Almost always, these entities have their own power converters for grid interfacing and energy processing. Having individual converters has advantages like more flexible individual control and simpler design but does not encourage functionality merging. Reduction of semiconductors to arrive at a more compact integrated design is thus not possible. Addressing this concern, a number of integrated energy generation systems that use 25% lesser semiconductors are proposed. The systems can be single or three phase depending on the types of sources, storages, and loads assembled. They can operate in the grid-tied or stand-alone mode with no compromise in performances expected, when compared with other solutions using more switches.

KEYWORDS: Distributed generation (DG), energy storages, energy systems, microgrids, pulse width-modulated converters.

I. INTRODUCTION

 Distributed generation (DG) by local green energy sources has gained worldwide attention because of the ever-growing energy demand, gradual depletion of fossil fuels, and environmental concerns linked to the burning of fossil fuels. Accompanying this interest is an equally intensive effort devoted to energy storages like batteries, ultracapacitors, and flywheels. Energy stored in these mediums can appropriately be used for smoothing variations linked to most green (usually renewable) sources, which at present are major shortcomings. Another way of smoothing the variations is to design the DG systems with different types of sources, whose generation characteristics must complement each other. There is however no guarantee that a continuous stream of energy will always be produced if the sources are mostly uncontrollable likes renewable sources. For greater controllability, energy storages appear to be unavoidable even though their capacities can be reduced if there are more source types in the systems. The installed energy storages also need not be of the same type. They should instead be designed with a variety, for example, a combination of ultracapacitors and batteries for fulfilling the power and energy density requirements of the considered system. In short, that means a typical comprehensive energy system would unlikely be a single-source system. Rather, it would include many entities needed for meeting the local generation, storage, utilization, and grid-tied requirements. Almost always, these entities would have their own power converters for processing energy to a form suitable for storage or consumption. This is no doubt the most flexible arrangement, which certainly is an advantage. Other advantages can also be thought of, but for certain, including too many individual converters to a system might at times introduce too much costly redundancy. This might be the case for renewable systems, whose energy generations are usually intermittent. Power converters connected to them might therefore operate below their rated capacities for a sizable period of time. It might hence be of interest to

perform some integration rather than use multiple individual converters as per existing practice. For that, a number of integrated energy systems using 25% lesser semiconductors are proposed here for DG [1]. Operating principles and advantages of the systems proposed are first clarified before considering their likely performance tradeoffs. These tradeoffs cannot be avoided by most (if not all) reduced semiconductor topologies but can surely be minimized for the systems proposed. Relevant explanation can be found in a later section, together with experimental results for proving the practicalities of the systems proposed.

II. ENERGY GENERATION SYSTEMS WITH NON INTEGRATED POWER CONVERTERS

Fig.1.1 (a) shows the typical block representation of a common solar energy generation system drawn here for example. Each source or storage included is accompanied by its own dc–dc boost or charging converter tied to a common dc link. The harnessed energy is then forwarded to a dc–ac inverter for conditioning before channeling it to the grid. The inverter can either be single or three phase, even though the latter is explicitly drawn in the diagram. It is also not necessary for the dc–ac inverter to tie to the grid if the energy generated is meant for immediate load consumption in an islanded local microgrid. The dc–ac inverter in an islanded microgrid can also be replaced by a dc–dc converter if the loads are dc by nature. DC network is certainly a possibility, but based on present advancement, ac output would probably continue to dominate for many more
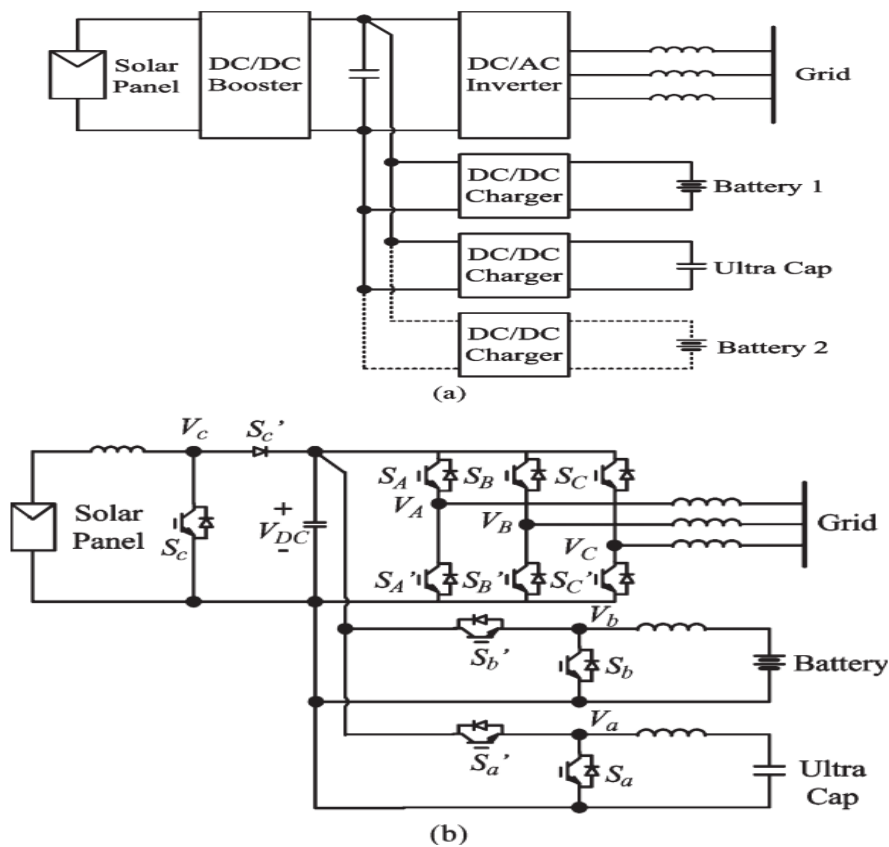

Fig.1.1. Example (a) block diagram and (b) circuit layout of nonintegrated energy system.

To reveal more details of Fig.1.1 (a), its individual blocks are filled with some simple representative circuits. The resulting circuit shown in Fig.1.1 (b) uses 12 semiconductor devices in total. Eleven of the devices are controllable switches with the remaining one being an uncontrollable diode. The diode S'_c can be replaced by a controllable switch if

the indicated solar panel in Fig.1.1 (b) is replaced by another type of source that can absorb backward flow of energy. Regardless of that, the system shown in Fig.1.1 (b) clearly lacks integration. Its formation is simply by connecting individual well-known converters to a common dc link. The system is thus fully decoupled with each converter having virtually no influence on the others. Surely, this is an advantage, but because of the intermittent nature of the solar source (in fact, most renewable sources) and battery charging process, most of the converters would likely not operate continuously at their rated capacities[2]. The resulting system built with multiple individual converters is hence neither cost effective nor compact. The suggestion is then to introduce some amount of integration to the system to cut down on its number of semiconductors. The integrated system must produce comparable input and output performances as the fully decoupled system. Like all reduced semiconductor topologies though, some tradeoffs like higher voltage stresses and control limitations would likely surface.but can surely be minimized if designed appropriately. Approaches to realize the minimization for the proposed single- and three-phase energy systems are now described as follows.
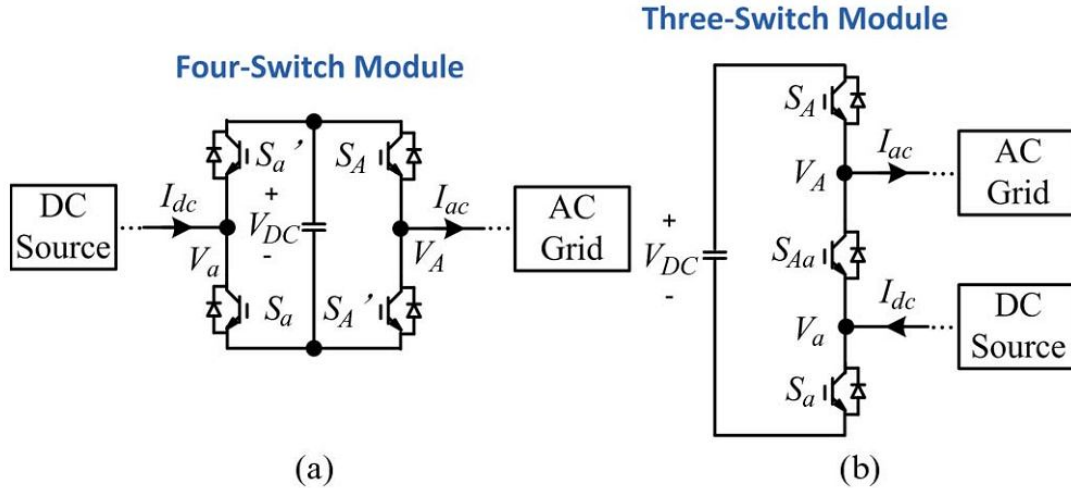

Fig.1.2. Illustration of (a) nonintegrated four-switch and (b) integrated three switch topologies.

TABLE I
SWITCHINGSTATES ANDOUTPUTVOLTAGES OF FIG.1.2 (a)

S_A	S_A'	S_a'	S_a	V_A	V_a
ON	OFF	ON	OFF	V_{DC}	V_{DC}
ON	OFF	OFF	ON	V_{DC}	0
OFF	ON	OFF	ON	0	0
OFF	ON	ON	OFF	0	V_{DC}

TABLE II
SWITCHINGSTATES ANDOUTPUTVOLTAGES OF FIG.1.2 (b)

S_A	S_{Aa}	S_a	V_A	V_a
ON	ON	OFF	V_{DC}	V_{DC}
ON	OFF	ON	V_{DC}	0
OFF	ON	ON	0	0

III. INTEGRATED ENERGY GENERATION SYSTEMS

A. Method of Integration

The integration principles are better explained by referring first to the nonintegrated energy system shown in Fig.1.1 (b). For easier viewing, two of its phase legs with switches $\{S_A, S'_A, S_a, S'_a\}$ are drawn separately, as shown in Fig.1.2 (a). For each of the illustrated phase legs, its two switches must be switched in complement, meaning that, when one switch is on, the other must be off. Terminal voltage of the considered phase leg can then produce two discrete values identified as Vdc and 0 V. The same applies to the other phase leg shown in Fig.1.2 (a). Terminal voltages of the two phase legs can then be any of the four sets of values indicated in Table I. Instead of two independent phase legs, the switches can be rearranged as shown in Fig.1.2 (b) while still providing two terminal voltages. Instead of four switches, only three switches labeled as $\{S_A, S_{Aa}, S_a\}$ are used. That represents a saving of 25%, which can be sizable if more switches are considered. Among the three switches, two of them will be turned on to tie the terminal voltages to either the same or different dc rails at any instant. The three possibilities are summarized in Table II, which, when compared with Table I, tells a constraint faced by the three-switch topology. To be more precise, the terminal voltages of the three-switch topology cannot produce the fourth combination of $V_A = 0V$ and $V_a = V_{dc}$, which certainly is a tradeoff incurred by saving one switch. The overall system design should therefore be planned such that influences from this tradeoff on the terminal voltages
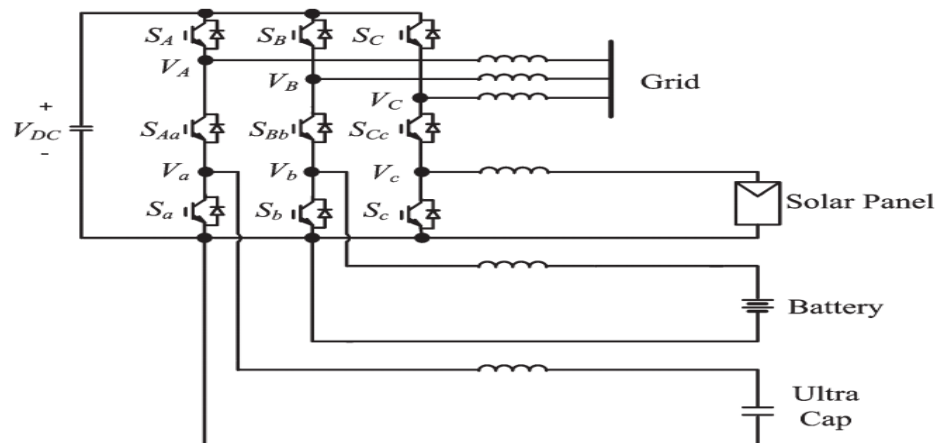

Fig.1.3 Integrated three-phase energy system with multiple sources and storages.

are kept to a minimum. Discussion on this issue can be found in the next section. Applying the same integration to the remaining two pairs of phase legs with switches $\{S_B, S'_B, S'_b, S_b\}$ and $\{S_C, S'_C, S'_c, S_c\}$ then results in the integrated energy system shown in Fig.1.3. The system in Fig.3.3 uses nine switches as compared to 12 for the nonintegrated system shown in Fig.1.1 (b). The same six terminal voltages are retained with the upper three produced by the dc–ac inverter formed by the upper three switches $\{S_A, S_{Aa}, S_a\}$ and middle three switches $\{S_B, S_{Bb}, S_b\}$. On the other hand, the lower three voltages are produced by three dc–dc converters formed by the middle three switches $\{S_B, S_{Bb}, S_b\}$ and lower three switches $\{S_C, S_{Cc}, S_c\}$. The middle three switches are obviously shared by the inverter and converters, which will surely introduce some constraints as already identified (fourth combination of $V_A = 0V$ and $V_a = V_{dc}$ cannot be produced). Before progressing forward, it is appropriate to share here that the same nine-switch topology has earlier been used as an ac–ac converter for dual motor drives, rectifier-inverter systems, and uninterruptible power supplies. In those attempts, the six converter terminals are organized as either two sets of three-phase ac outputs or one set of three-phase ac input and one set of three-phase ac output [3]. They have so far been proven fine, but with serious limitations imposed. The limitations can be summarized as either a very limited phase shift between the two sets of ac terminals or a doubling of dc-link voltage caused by strict amplitude sharing . These constraints would make the 25% saving in semiconductors not so attractive. Methods for minimizing them are therefore of interest and are discussed here in the context of energy systems. Concentrating on energy systems also has the merit of merging ac and dc circuits using the nine-switch topology, which so far has not been tried by other researchers.

B. Modulation Principles

Referring again to those two simplified illustrations shown in Fig.1.2, making them produce the same terminal voltages
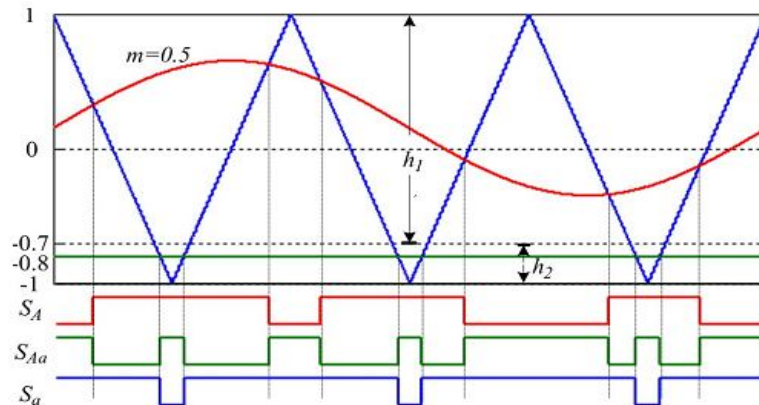

Fig.1.4. Carrier band division and gating signal generation per phase leg.

would demand that they share the same modulation theories. Some constraints would however be accompanying the three switch topology shown in Fig.1.2 (b) since it uses lesser switches. A convenient way of explaining the three-switch modulation is hence to focus on the more established independent phase legs shown in Fig.1.2 (a) first, before shifting the knowledge with constraints added to Fig.1.2 (b). With the circuit shown in Fig.1.2 (a), the phase leg tied to the dc source is, in theory, controlled by a dc reference and a triangular or saw-tooth carrier. The second phase leg tied to a phase of the three-phase ac grid is similarly controlled by a sinusoidal reference and a triangular carrier (saw-tooth carrier not considered here since it has no spectral benefit). Strictly, carriers of the two phase legs need not be the same, but in practice, using one carrier has the benefit of involving only one timer. It is hence advisable to use a common carrier and two independent references for the circuit shown in Fig.1.2 (a). The same independence cannot be introduced to the integrated topology shown in Fig.1.2 (b), whose sinusoidal reference for the upper terminal must always be placed above its linear reference for the lower terminal. Such placement helps to avoid the fourth restricted state of $V_A = 0V$ and $V_a = V_{dc}$. An example illustrating the three-switch modulation is shown in Fig.1.4, where a single carrier band is clearly divided into h_1 and h_2. The upper sub band h1is assigned to the upper terminal and hence confines the sinusoidal reference. Similarly, the lower sub band h_2 is assigned to the lower terminal and hence encompasses the linear reference. Comparing the references with the single common carrier based on the following rules then leads to those gating signals for S_A and S_a shown at the bottom of Fig.1.4

$$S_A = \begin{cases} 1, & \text{reference} \geq \text{carrier} \\ 0, & \text{reference} < \text{carrier} \end{cases}$$

$$S_a = \begin{cases} 0, & \text{reference} \geq \text{carrier} \\ 1, & \text{reference} < \text{carrier.} \end{cases} \quad (1.1)$$

To ensure that only two switches are on and hence produce any of the three combinations shown in Table II, the gating signal for the middle switch SAa must be derived from the earlier two based on the following:

$$S_{Aa} = S_A \oplus S_a - (!S_A) \oplus (!S_a) \quad (1.2)$$
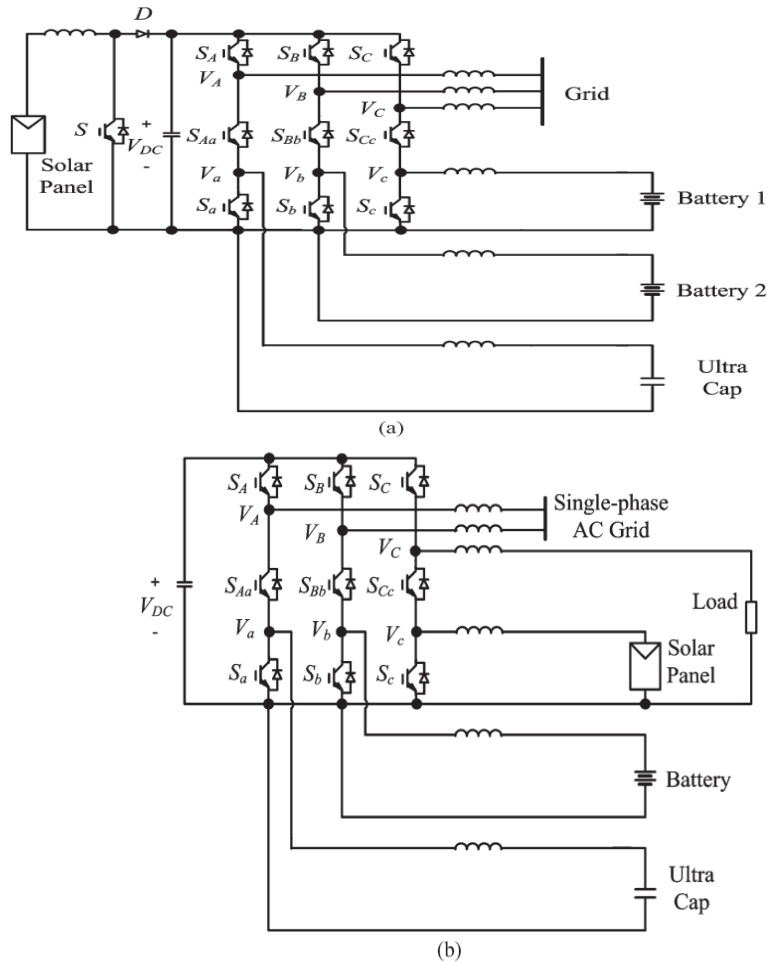
Fig.1.5. Other integrated configurations for (a) three- and (b) single-phase grid-tied energy conversions.

Where $\oplus$ is the logical XOR operator and $!S_A$ and $!S_a$ are the complements of S_A and S_a with dead time added. Operating on $!S_A$ and S_a is recommended since it automatically creates the dead time needed by S_{Aa} to avoid shorting the three switches simultaneously . The full set of gating signals obtained (e.g., bottom of Fig.1.4) is thus always in agreement with the allowed states summarized in Table II. Another concern noted with the modulation process is the dc offset added to the sinusoidal reference for centering it within h_1.Like triplen, this offset is added to all phases of a three phase system and will therefore be cancelled in the line-to-line voltages.

C. Parameters and Constraints

As mentioned earlier, the lower subband$h2$ in Fig.1.4 is assigned to the lower terminal of the three-switch topology shown in Fig.1.2 (b). Given that it is tied to a dc source, the usual parameter of interest would be the duty ratio d or fractional on time of the lower switch Sa. The range of variation of d and its accompanied gain G_{dc} (= $1/(1-d)$)can accordingly be determined as

$$(1 - 0.5h_2) \leq d \leq 1 \qquad 2/h_2 \leq G_{\mathrm{dc}} < \infty. \qquad (1.3)$$

For interfacing the dc source to the ac grid, G_{dc} must usually be high so as to minimize the number of dc sources or storages connected in series. With fewer entities in series, problems like shading and unbalanced charging are less prominent, inferring that mechanisms for preventing them might not be necessary. The overall system is hence simplified, which certainly is a strong reason for keeping$h2$small and G_{dc} high. Referring now to the upper terminal of

the three-switch topology shown in Fig.1.2 (b), since it is tied to an ac source, its parameter of interest would be the modulation index M. Referring to Fig.1.4, M represents the amplitude of the sinusoidal reference, which, in theory, is also equal to the resulting buck gain G_{ac}. Its value can vary within the range spelled in (1.4), where the factor of 1.15 is added for representing triplen insertion.

$$0 \leq M \leq 1.15 \times h_1/2. \tag{1.4}$$

The value of M is also known to vary inversely with the dc-link voltage Vdc ($M \propto 1/V_{dc}$)in the case of a fixed ac grid voltage. Lowering Vdc therefore requires M and, hence, h1to be high. That means $h_2 = 2 - h_1$in Fig.1.4 must be low, which, for the proposed energy system, is fine since a high dc gain G_{dc} is needed, as explained earlier. The proposed energy system is therefore a more suitable system for applying the three-switch topology shown in Fig.1.2 (b) rather than those ac–ac converters. In those references, V_{dc} is doubled because M is set to a maximum of only 0.5.

D. Other Integrated Configurations

Instead of the system shown in Fig.1.3, the three-switch topology shown in Fig.1.2 (b) can be used to form other energy systems. Two proposed examples are shown in Fig.1.5 (a) and (b), where, again, three three-switch phase legs are shown. In general, the number of three-switch phase legs connected in parallel can be any positive integer
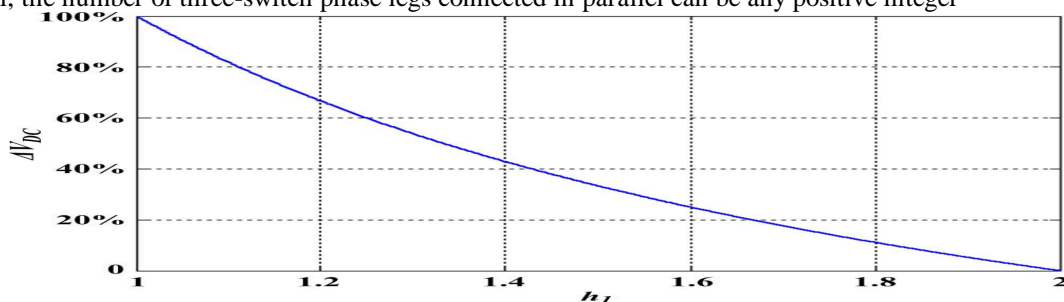

Fig.1.6. Illustration of dc-link voltage increase for three-switch topology.

number. It depends on the number of sources, storages, and loads connected together. Where needed, traditional two-switch phase legs can also be added in parallel to the three-switch phase legs. This extension is relatively straightforward and will hence not be explicitly shown in this paper. Rather, the intention for including Fig.1.5 (a) is to show the additional possibility of connecting a solar panel (indicated only as an example) to the dc link through its dc–dc converter. Unlike Fig.1.3, no source is now connected to the lower three dc terminals, which are instead tied to three storages (two batteries and an ultracapacitor). The system however retains its three-phase ac grid interfacing like in Fig.1.3. For illustrating single-phase grid interfacing, Fig.1.5 (b) is referred to instead, where two of its upper terminals are used for single-phase grid interfacing. The same dc offset as in Fig.1.4 must still be added to the two 180° phase-shifted sinusoidal references for the two upper terminals, which, when subtracted, will not appear in the ac voltage (V_A-V_B). Since the third upper terminal is now not used for grid interfacing, it can either be removed together with switch SC or tied to a dc load, as shown in Fig.1.5 (b). Other connections to the lower three dc terminals in Fig.1.5 (b) remain unchanged as in Fig.1.3.

IV. THREE-SWITCH VERSUS FOUR-SWITCH TOPOLOGY

A. Dc-link voltage

As described earlier, the four-switch topology shown in Fig.1.2 (a) is divided into two independent phase legs with no restriction on their modulation parameters. Choosing the ac terminal voltage VA as the base (= 1p.u.), the minimum dc link voltage Vdc is then given by 1.74 p.u. if VA is assumed to be a phase of a three-phase ac grid. This value is obtained by substituting the maximum modulation index of M=1.15 to the standard definition of $M=V_A/(V_{dc}/2)$. On the other hand, if a single-phase ac system is considered, the minimum Vdc would change to 2 p.u. since the maximum M is now one. Converting from three- to single-phase system is thus a simple multiplication by 1.15, which is also applicable to the three switch topology shown in Fig.1.2 (b). Unlike the four-switch topology, the maximum modulation index of the three-switch topology in a three-phase system is not M=1.15but is rather given by the expression in (1.4). The minimum

dc-link voltage V_{dc} of the three-switch topology is thus computed as $(3.48/h_1)$ p.u. for the three-phase systems shown in Figs.1.3 and 1.5 (a). [As mentioned earlier, a multiplication factor of 1.15 needs to be included for the single-phase system shown in Fig.1.5 (b).] In percentage term, it represents an increase given by

$$\Delta V_{\mathrm{dc}} = \frac{\left(\frac{3.48}{h_1}\right) - 1.74}{1.74} \times 100\%$$
$$= \left(\frac{2}{h_1} - 1\right) \times 100\%, \qquad 1 \leq h_1 \leq 2.$$

(1.5)

TABLE III
Currents through Switches at different Output Voltages for Four-Switch Topology

S_A	$S_A{}'$	$S_a{}'$	S_a	V_A	V_a
I_{ac}	0	$-I_{dc}$	0	V_{DC}	V_{DC}
I_{ac}	0	0	I_{dc}	V_{DC}	0
0	$-I_{ac}$	0	I_{dc}	0	0
0	$-I_{ac}$	$-I_{dc}$	0	0	V_{DC}

Variation of (1.5) is shown in Fig.1.6, from which it is read that the increase is 100% or doubled when $h_1=1$ or M= 0.5. This doubling of dc-link voltage is experienced by those ac–ac converters , which conceptually can be reduced here by increasingh1. For example, if h1 is raised to 1.6 and 1.8, the increase ΔV_{dc} would be 25% and 11%, respectively. It is hence important to keep one sub band much wider than the other (h_1 h_2 shown in Fig.1.4), which, fortunately, is a requirement enforced by the proposed energy systems. This identification has so far not been discussed in the open literature. When dividing the carrier band, it is also of concern to mention here that the upper subbandh1must include all upper references and the lower sub band h_2 must include all lower references. That indirectly means that the highest modulating references in both sub bands will decide on the appropriate level to divide in the full carrier band. These references correspond to the highest upper and lower terminal voltages that the inverter can manage.

B. **Switch Currents and Overall System Losses**

Instantaneous current stresses experienced by the switches can be found by considering the individual terminal currents and converter states summarized in Tables I and II for the four-switch and three-switch topologies. For clarity, positive reference currents for the terminals are defined here as those of I_{ac} and Idc shown in Fig.1.2 (a) and (b). Positive current through a switch is also defined as current flowing through its transistor, which then means that negative current flows through its antiparallel diode. With these definitions, the four-switch topology shown in Fig.1.2 (a) can easily be analyzed by considering which switches from its two phase legs are turned on. The turned-on switches will carry the respective terminal currents, which then lead to those entries shown in Table III for each pair of corresponding terminal voltages [4]. The table shows that each switch of the nonintegrated four-switch topology carries a terminal current, which is not true for the integrated three-switch topology. For example, to produce $V_A=V_a=V_{dc}$, the first row of Table II indicates that the upper two switches S_A and S_{Aa} of the threes witch topology must be turned on, which then lead to currents $-(I_{dc}-I_{ac})$ and $-Idc$ flowing through them. The current flowing through SA is obviously decided by two terminal currents and not one. The same determination can be applied to the other two states listed in Table II with their resulting current expressions summarized in Table IV. Table IV is, in principle, applicable to the three systems shown in Fig.1.3 and Fig.1.5 (a) and (b) since they use the same three-switch topology and the same three operating states.

TABLE I V

Currents through switches at different output voltages for three-switch topology

S_A	S_{Aa}	S_a	V_A	V_a
$-(I_{dc}-I_{ac})$	$-I_{dc}$	0	V_{dc}	V_{dc}
I_{ac}	0	I_{dc}	V_{dc}	0
0	$-I_{ac}$	$I_{dc}-I_{ac}$	0	0

The currents obtained in Tables III (first three rows only) and IV can then be compared for each pair of terminal voltages produced. The conclusions drawn are summarized hereinafter.

1) By eliminating one switch, the middle switch SAa of the three-switch topology carries the same current as either S'$_A$ or S'$_a$ of the four-switch topology, depending on the state presently being assumed.

2) The current through S_A of the three-switch topology has an interval over which its current is $-(I_{dc}-I_{ac})$. Otherwise, it is closely similar to the current flowing through S_A of the four-switch topology.

3) The current through Sa of the three-switch topology is similar to that flowing through the same switch of the four-switch topology, except for an interval over which the current is $(I_{dc}-I_{ac})$. It should be noted here that the absolute amplitude of the current $(I_{dc}-I_{ac})$ depends on the amount of boosting introduced and the individual current polarities (e.g., charging or discharging, terminals connected to sources, storages, or loads). Instantaneous current stresses might therefore be raised, but that does not imply the same for the overall system losses. On average, if a good mix of different entities is tied to the integrated system, its losses should be either comparable or slightly raised as compared to its nonintegrated counterpart. The slightly higher losses are mainly caused by the slightly higher dc-link voltage needed by the integrated system, as understood from Fig.1.4.

To demonstrate, the overall losses of the nonintegrated and integrated energy systems shown in Figs.1.1 (b) and 1.3 have been computed based on the simulation approach. Switches used for the simulation are 600-V/50-A insulated gate bipolar transistors (IGBTs), whose parameters can be found. For both systems, energy flow has been tuned to flow from the solar source to the ac grid and storages. Results obtained are tabulated in Table V for small lh2≤0.4, which is in accordance to the earlier suggested band sizing requirement. The results show that, for smaller h_2, losses of the nonintegrated energy system increase because of the lower dc terminal voltages and hence higher dc terminal currents if the system power is kept constant. The integrated system, on the other hand, has its losses reduced because of the lower dc-link voltage associated with a smaller h_2. This trend is applicable to both three-phase systems shown in Figs.1.3 and 1.5(a), except for higher loss values anticipated with Fig.1.5(a) because of its additional switch S, diode D, and other passive components. The evaluation is next performed with the three-phase grid in Fig.1.1 (b) replaced by a single-phase grid and a resistive load like those shown in Fig.1.5 (b) for the single-phase integrated system. Results obtained for both systems can be found in Table VI, which, upon compared, show lower losses for the integrated

TABLE V

Losses of energy systems with three-phase grid

h_2	Non-Integrated System		Integrated System	
	DC-Link Voltage (p.u.)	Losses (% Rating)	DC-Link Voltage (p.u.)	Losses (% Rating)
0.2	1.74	1.65	1.93	1.41
0.3	1.74	1.53	2.05	1.65
0.4	1.74	1.41	2.17	1.91

TABLE VI
Losses of energy systems with single-phase grid

h_2	Non-Integrated System		Integrated System	
	DC-Link Voltage *(p.u.)*	Losses (% Rating)	DC-Link Voltage *(p.u.)*	Losses (% Rating)
0.2	2.0	1.55	2.22	1.11
0.3	2.0	1.43	2.36	1.22
0.4	2.0	1.41	2.50	1.41

system. The reason might probably be linked to the third upper terminal supplying a positive current to the dc load. The earlier notated upper current I_{ac} is thus always positive, which, when subtracted from Idc, will always lead to a smaller $(I_{dc}-I_{ac})$ for the third three-switch phase leg. Since its currents are reduced, its losses will reduce accordingly too.

V.   CONTROL PRINCIPLES

In this section, only the control schemes for the integrated energy system shown in Fig.1.3 are explained in detail. This does not compromise generality since the other two discussed systems in Fig.1.5 (a) and (b) and the nonintegrated system shown in Fig.1.1 (b) share the same control principles. The same control schemes were, in fact, used for single- and three phase experimental testing, whose results are shown in a later section. It is hence appropriate to consider only Fig.1.3 with its upper dc–ac inverter control discussed now with reference to the upper half of Fig.1.7. In that representation, the dc link voltage Vdc is first measured, before being regulated by a classical proportional (P)-integral (I) (PI) controller to follow a defined command V*$_{dc}$. Parameters of this PI controller are designed based on, where the inner current loop, being much faster, is replaced by a time lap and a low-pass-filter block for representing computational delay and capacitor charging dynamics. The P and I gains are then chosen as K =0.1 and K$_{i1}$=10 to give enough phase margin for maintaining the overall system stability. The PI output, being the active current amplitude needed for keeping Vdc constant, is then multiplied with a unit sine synchronized with the ac grid voltage V grid by a standard phase locked loop. The resulting ac signal I*$_{ac}$ represents the in-phase active current reference fed to the inner current loop. The inner current controller can no longer be a PI controller, whose steady-state error is not zero because of its finite gain at the ac frequency of interest. A P–resonant (PR) controller is used instead, whose transfer expression is written as

$$G_{\mathrm{PR}}(s) = K_{p2} + \frac{2K_{i2}\omega_c s}{s^2 + 2\omega_c s + \omega_0^2}$$
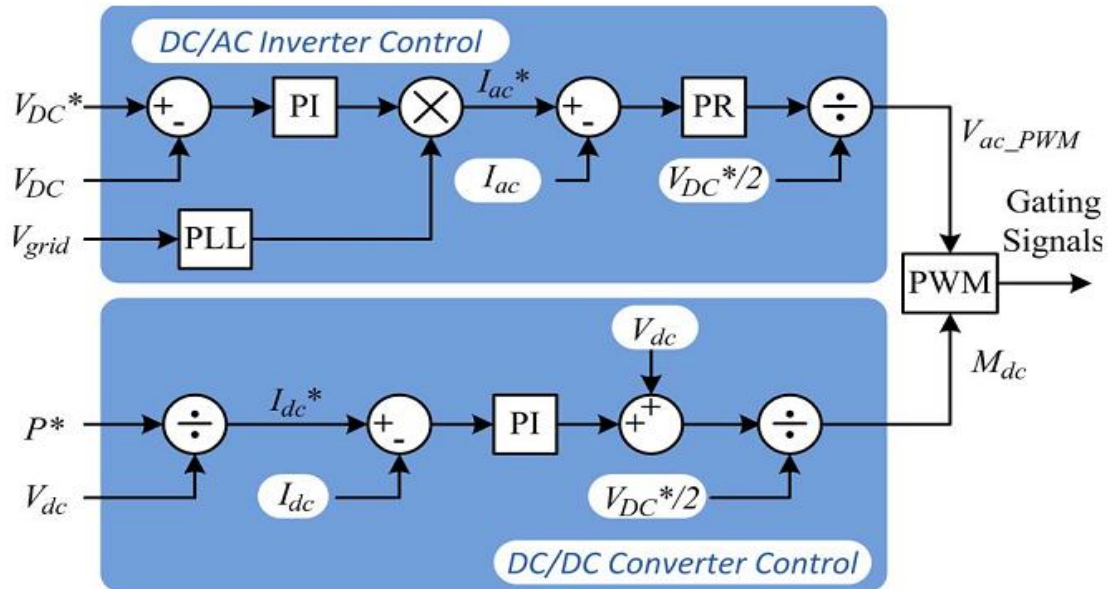
(1.6)

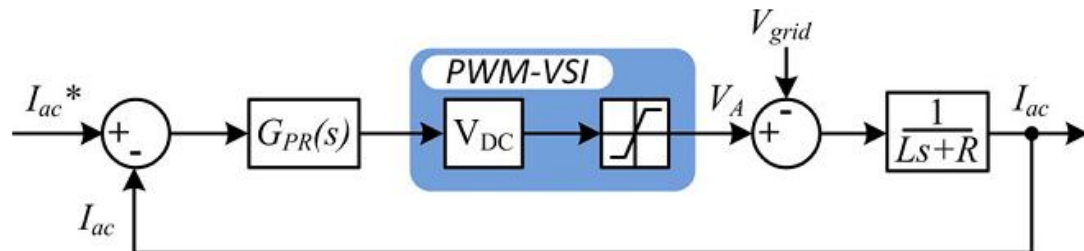Fig.1.7. Per-phase illustration of the overall control schemes.

Fig.1.8. Per-phase ac inner current loop.

Where K_{p2} and K_{i2} are the controller gains and ω_c and ω_o are the angular cutoff and fundamental frequencies, respectively. Bode diagrams of (1.6) will, in theory, have a high resonant peak at the 50-Hz frequency of interest. This peak will gradually tend toward infinity as $\omega c{\to}0$. The final tracking performance of the inner current loop can be verified by referring to its control block diagram drawn separately in Fig.1.8. Filter impedance (R+sL) and grid voltage V grid have now been included in the figure for arriving at its closed-loop transfer function written in (1.7). The derived transfer function clearly has two terms for informing that, if the controller gains are chosen high enough, I_{ac} will follow its reference I^*_{ac} exactly with little influence from V grid

$$I_{\mathrm{ac}} = \frac{G_{\mathrm{PR}}(s)V_{\mathrm{dc}}}{G_{\mathrm{PR}}(s)V_{\mathrm{dc}}+sL+R}I^*_{\mathrm{ac}} - \frac{1}{G_{\mathrm{PR}}(s)V_{\mathrm{dc}}+sL+R}V_{\mathrm{grid}}. \tag{1.7}$$

The controller gains, on the other hand, cannot be too high if the system is to be kept stable[5]. To balance the tradeoff, Bode diagrams of the open-loop transfer function of Fig. 1.8 are plotted in Fig.1. 9. In addition to those obtained with the PR controller, relevant plots obtained with a P controller are also included in Fig.1. 9 for the design. The design procedure read from then suggests choosing a P gain *Kp*2 for the P controller so that the system is stable with good transient response. For that, *Kp*2 = 0.1 is chosen, which gives more than 90◦ of phase
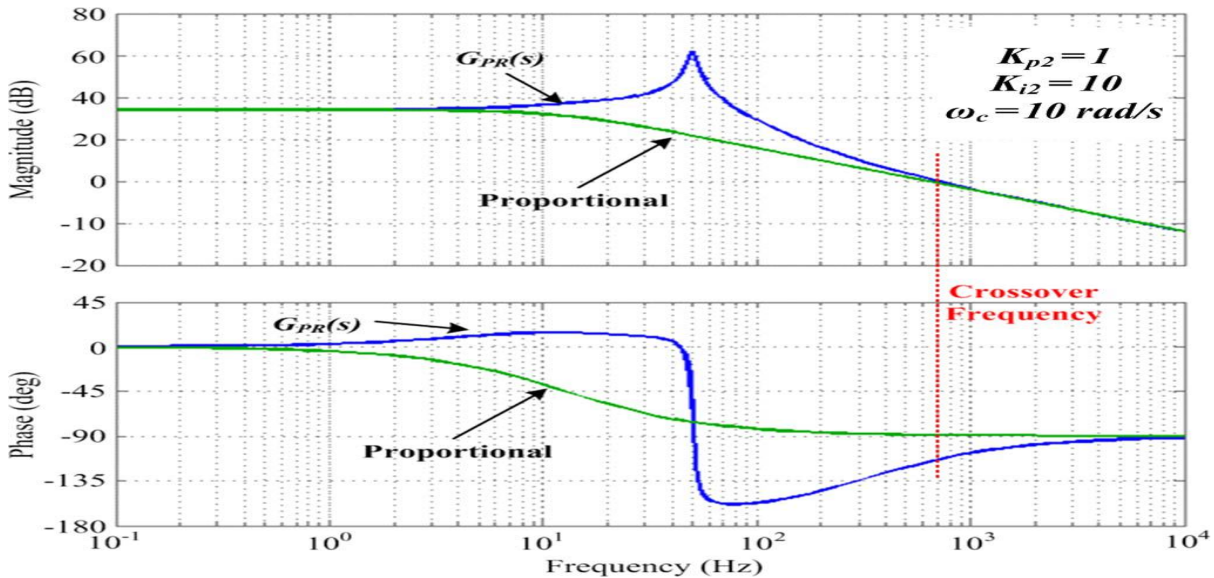
Fig.1.9. Bode plots of feedforward path of Fig.1.8.

margin at the system crossover frequency (instant at which magnitude response drops to 0 dB). The system is thus stable. The second step is to design the resonant gain so that acceptably small steady-state errors are produced, together with a satisfactory phase margin. The chosen resonant gain here is $Ki2 = 10$, which will alter only the magnitude response around 50 Hz and not at the crossover frequency. The final phase margin is thus still more than 60◦, which, needless to say, represents a stable system. Cutoff frequency ωc can next be chosen, whose purpose is mainly to lessen selectiveness by Fig.1. 9. Bode plots of feed forward path of Fig.1. 8. widening the bandwidth around the resonant peak. This can be helpful if the 50-Hz resonance frequency varies slightly but should not be excessive since the resonant peak amplitude drops significantly as ωc increases. The resulting signal from the properly designed PR controller then forms the required ac modulating reference (upper sinusoidal reference in Fig.1. 4) needed for switching pulse generation. For that, a timer counting from zero to one and then back is used for realizing a positively displaced triangular carrier, unlike that shown in Fig.1. 4. The ac modulating reference should therefore be changed according to (1.8), whose effect is still to place the reference centrally within the upper subband $h1$

$$V\_ac\_PWM = 0.5Vac\_PWMh1 + 1 − 0.5h1. \qquad \text{………} \qquad (1.8)$$

Attention should next be focused on the control scheme shown at the bottom of Fig.1. 7 for the dc–dc converters. In that scheme, a power reference (or voltage reference in some cases) is first created by an algorithm linked to the source or storage. For the case of a solar module, the power reference is usually decided by an appropriate maximum-power-point-tracking algorithm . The determined power reference can then be divided by the measured input voltage to create a current reference $I*dc$ for tracking by the dc boost current Idc. Tracking is enforced here by a simple PI controller, whose high dc gain helps to force zero dc steady-state error. Tuning of this PI controller is presently well established and can, in fact, be done in Matlab after setting the desired closed-loop bandwidth to be a fifth of the switching frequency or lower. The final parameters obtained are summarized here as $Kp3 = 0.301$ and $Ki3 = 2131$. The output from the PI controller is then added to the feed forward source voltage Vdc, before being normalized by half the dc-link voltage $V *dc/2$ to form the linear dc modulating reference Mdc. This modulating reference, according to Fig.1.4, is placed within the lower subband $h2$. Since the carrier is realized with a timer counting between zero and one as mentioned
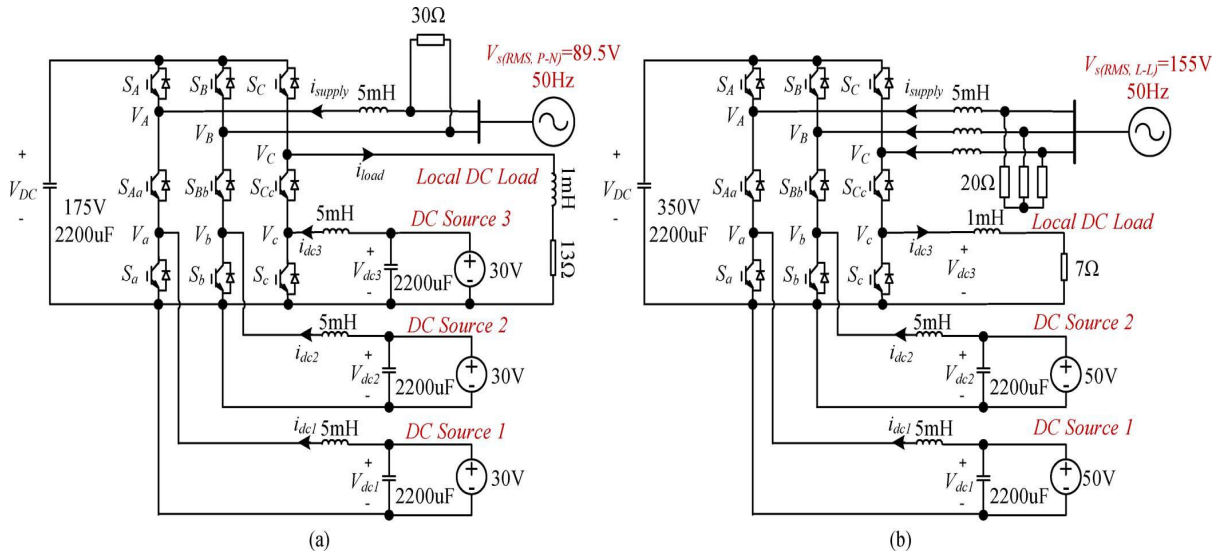
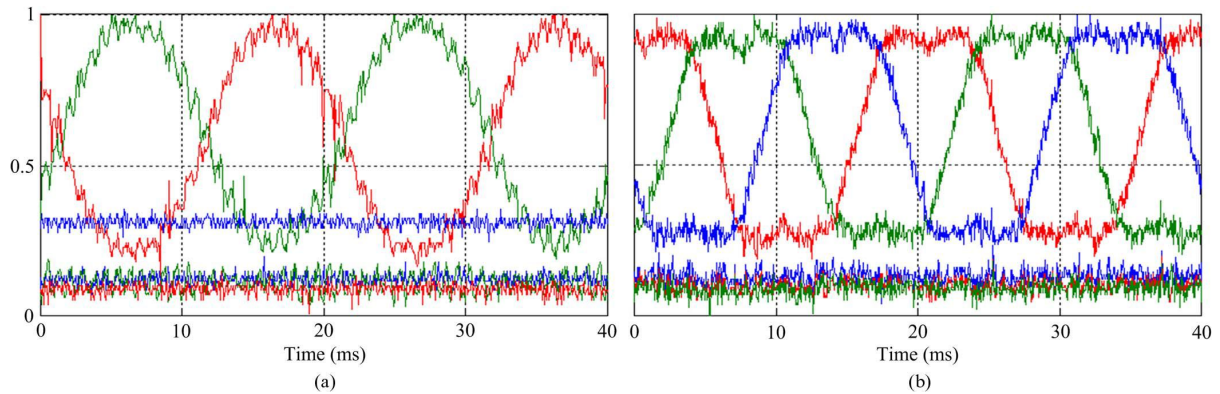Fig.1. 10. Experimental setups and parameters used for (a) single- and (b) three-phase energy systems.

Fig.1. 11. Modulating references for single-phase system in Fig. 10(a) and three-phase system in Fig. 10(b) before transient. (a) Single phase. (b) Three phase.

earlier, no dc offset needs to be added to Mdc, unlike the ac reference Vac_PWM. In general, the presented control schemes function well with the same steady-state responses produced by the nonintegrated and integrated energy systems, if controlled by the same control schemes. Their transient responses are however different caused by coupling introduced by the integrated energy system. To illustrate, a transient step decrease in dc source current

reference I^*dc is assumed as an example. To make the actual dc source current Idc track rapidly, the on time of the lowest switch (e.g., Sa in Fig.1. 3) should be shortened, which, according to (1.1) and Fig.1. 4, requires the dc modulating reference Mdc to increase. The amount by which Mdc can increase is however limited to $h2$ for the integrated energy system. Its current response is therefore slower than the nonintegrated system whose modulating reference is not confined to $h2$. Slower response is however not experienced during transient step increase in current, which, based on the reverse reasoning, requires the on time of the lowest switch to be lengthened [6]. This requires lowering Mdc, which, according to Fig. 1.4, is not restricted by the integrated system. The above-explained slower current decrease of the integrated system is undeniably a disadvantage. However, when compared with the usually slow maximum power point tracking, storage charging, and discharging, its impact might not be significant. The proposed energy system is therefore still competitive as compared to its nonintegrated counterpart.

VI. EXPERIMENTAL RESULTS

For verification of practicality, scaled-down prototypes shown in Fig.1.10(a) and (b) were assembled in the laboratory using the parameters indicated in the figures (values chosen from those available in the laboratory and, hence, not optimized). Fig.1.10(a) was clearly a single-phase grid-tied system with two of its upper terminals connected to one phase of a 155-V (line-to-line rms) 50-Hz three-phase ac grid and a local single-phase ac load of 30 Ω. The third upper terminal was tied to a local dc load of 13 Ω, while the lower three terminals were connected to three separate dc sources of 30 V each. Two 180° phase-shifted sinusoidal and four linear references were thus needed, as shown in Fig. 1.11(a). In the figure, two upper sinusoidal references and a single linear load reference

at $M_{dc} = 0.33$ were shown occupying the upper subband with a width of $h_1/2 = 0.8$. Also shown in the figure were three lower linear references clustering around $M_{dc} = 0.15$ for the dc sources. They occupy the lower narrower subband with a width of $h_2/2 = 0.2$.
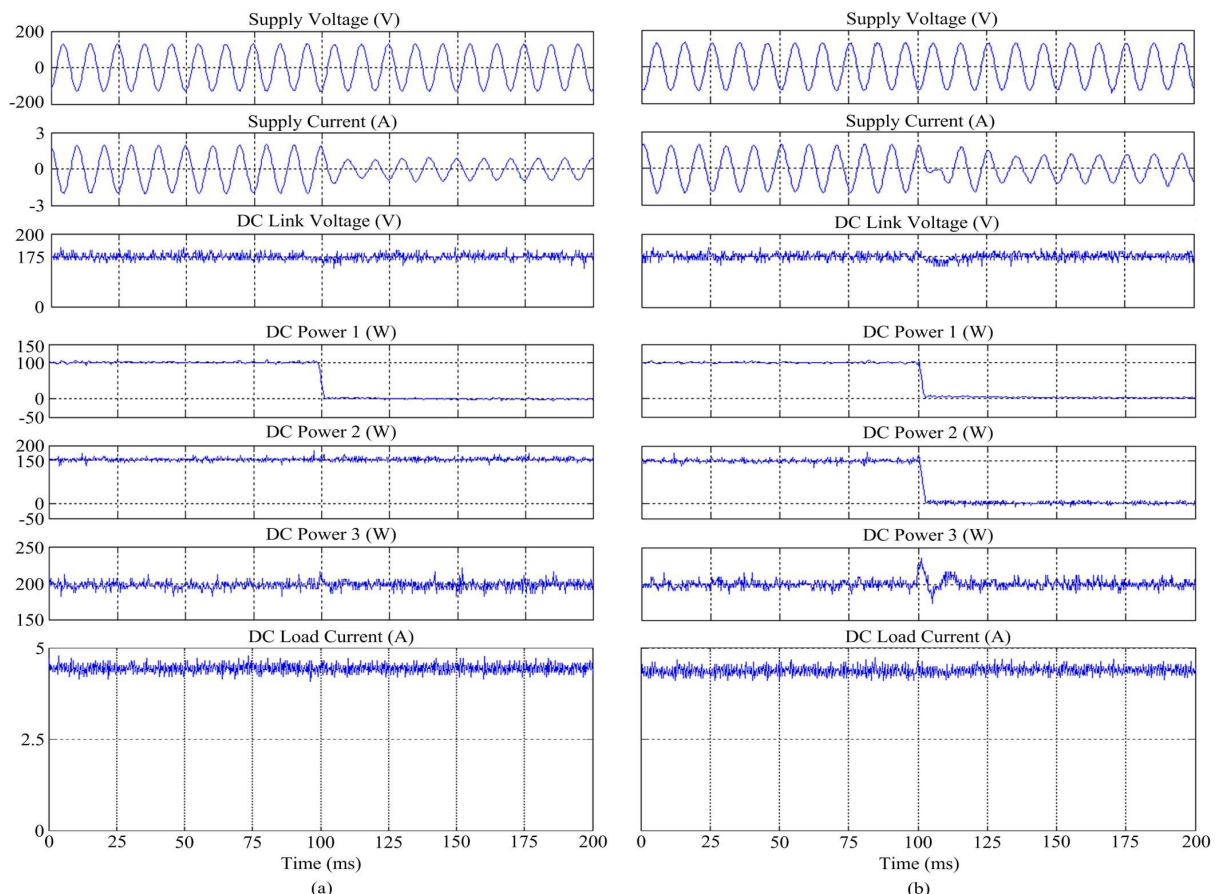

Fig.1.12. Experimental waveforms of single-phase system in Fig.1.10(a). (a) Transient 1. (b) Transient 2.

Corresponding waveforms of the single-phase power stage were then measured and plotted in Fig.1. 12 for two intentionally created transient events triggered at $t = 100$ ms in each plot. For the event shown in Fig. 1.12(a), all three dc sources were initially generating positive powers with their respective values read from the fourth to sixth traces as 100, 150, and 200 W before $t = 100$ ms. The generated powers were for local dc load consumption and injection to the ac grid. The former was reflected by the positive dc load current in the last trace, whilethe latter was reflected by the 180° phase-shifted ac voltage and current in the first two traces before $t = 100$ ms. At $t = 100$ ms, dc source 1 was interrupted

with the local dc load demand kept unchanged. Power output from dc source 1 therefore dropped to zero in the fourth trace, while the dc load current in the last trace remained constant. The amount of surplus energy injected to the grid was thus reduced, causing the ac supply current in the second plot of Fig.1.12(a) to drop. The same initial conditions in Fig.1.12(a) were repeated in Fig.1. 12(b), whose transient event at $t = 100$ ms was triggered by turning off dc sources 1 and 2 with the dc load demand kept unchanged. Power values in the fourth and fifth traces of Fig.1.12(b) therefore dropped to zero with the load current in the last trace kept constant. The remaining dc source 3 was not able to power the load fully, hence causing the ac grid current in the second trace to reverse. The ac grid current was now in phase with the ac grid voltage, representing energy drawn from the grid. Testing was next performed on the three-phase system shown in Fig.1.10(b) with its upper three terminals tied to the three phase ac grid and a local ac load of 20 Ω per phase. The lower three terminals were connected to two 50-V dc sources and a 7-Ω dc load, respectively. The references needed were therefore three upper sinusoidal references with triplen offset added and three lower linear references, occupying subbands h_1 and h_2 in Fig.1.11(b). The common dc-link voltage produced was 350 V, as seen from the third trace in Fig.1.13. This value could be reduced further by narrowing h_2 or widening h_1, as shown in Fig.1.6. Two transient events were also emulated here with the first shown in Fig.1.13(a). Throughout the illustrated duration, both dc sources were producing positive powers,
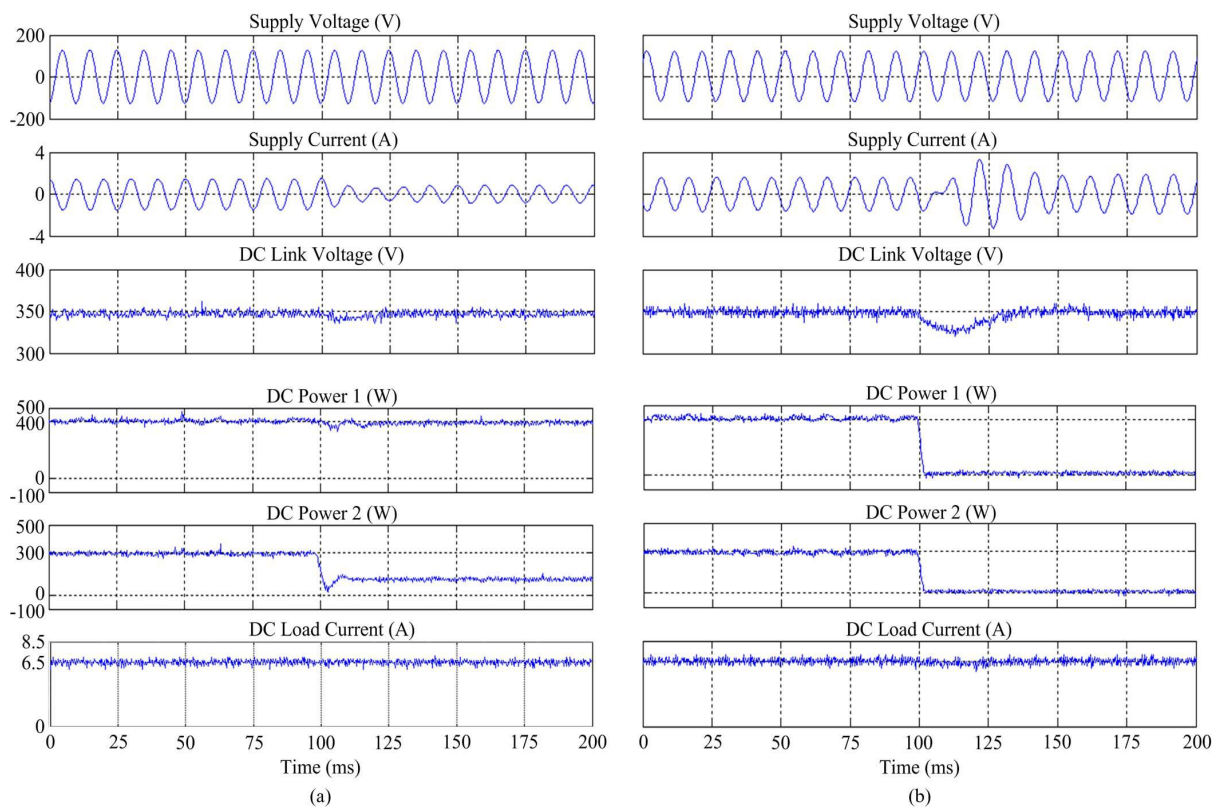

Fig.1.13. Experimental waveforms of three-phase system in Fig. 10(b). (a) Transient 1. (b) Transient 2.

as read from the fourth and fifth traces in the figure. Part of the generated powers was for local dc load consumption reflected by the last trace in Fig. 1.13(a). The rest was for ac grid injection reflected by the 180° phase-shifted ac voltage and current in the first two traces. Power from dc source 2 was subsequently lowered at $t = 100$ ms with the local dc load kept constant. Lesser power was hence injected to the grid, causing the ac current in the second trace to drop in magnitude after $t = 100$ ms. A second transient event was repeated in Fig. 1.13(b) with the same initial system conditions and constant dc load assumed. The transient was triggered by turning off both dc sources at $t = 100$ ms, causing the fourth and fifth traces to collapse to zero. The grid eventually had to reverse its energy flow to supply the local dc load. This was reflected by the ac grid current reversal in the second trace, to be now in phase with the grid voltage in the first trace.

These results clearly prove the effectiveness of the proposed integrated energy systems, which, in principle, can also be produced by the nonintegrated energy systems like the example shown in Fig. 1.1 (b). The integrated systems however have the following anticipated features, which have now been proven experimentally.

1) The same integrated configuration can be used for single and three-phase energy systems.

2) Doubling of dc-link voltage is not necessary, unlike those of ac–ac converters.

3) No significant deterioration of transient responses when applied to energy systems.

4) Energy flows through all terminals are not impeded by the converter merging, hence giving rise to no damaging surge or dip in voltage across the dc link. The dc-link voltage, in fact, remains nearly constant throughout the experiments.

5) Same implementation complexity with only one timer/ carrier and some dc offsets needed. DC offsets are usually added together with the triplens. Virtually the same performance is achieved with 25% lesser semiconductor.

VII. CONCLUSION

This project has proposed a number of integrated energy systems based on a compact converter topology. Through proper design, the proposed systems are shown to output equally good terminal waveform quality while yet gaining advantages like reduced switch count and compactness. Surely, some tradeoffs cannot be avoided but can be minimized through proper modulation planning and, hence, do not constitute a major problem. Experimental testing has already confirmed their conceptual validity and practicality, regardless of whether implemented in single- or three-phase form.

REFERENCES

[1]   Poh Chiang Loh, Lei Zhang, and Feng Gao, "Compact   Integrated Energy Systems   for   Distributed Generation," ," *IEEE Trans. Ind. Electron.,* vol. 60, no. 4, pp. 1137–1145, Apr. 2013.

[2]   S. Vazquez, S. M. Lukic, E. Galvan, L. G. Franquelo, and J. M. Carrasco, "Energy storage systems for transport and grid applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 3881– 3895, Dec. 2010.

[3]   J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. P. Guisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power electronic systems for the grid integration of renewable energy sources : A survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016,Jun. 2006.

[4]   D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice.* Piscataway, NJ: Wiley, 2003.

[5]   Ned mohan, torem underland and william P. Robbins, *Power Electronics Converters, Applications and Design,* Third Edition,2000.

[6]   J. P. Barton and D. G. Infield, "Energy storage and its use with intermittent renewable energy," *IEEE Trans. Energy Convers.,* vol. 19, no. 2, pp. 441–448, Jun. 2004.