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A New Cascaded 2-Level Inverter based STATCOM for High Power Applications

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ABSTRACT: This paper presents a simple STATCOM scheme using a cascaded two-level inverter-based multilevel inverter. The proposed topologies have two VSI based two-level inverters are connected in cascade through open-end windings of a three-phase transformer and filter elements. Converter fed dc-link voltages is regulates at different levels to obtain four-level operation. The proposed STATCOM multilevel inverter has operates under MATLAB/SIMULINK environment and the results are verified in balanced and unbalanced conditions. Further, stability behavior of the topology is investigated. The dynamic model is developed and transfer functions are derives under different conditions. The system behaviors are analyzing under various operating conditions.

KEYWORDS: DC-link voltage balance, multilevel inverter, power quality (PQ), static compensator (STATCOM).

I. INTRODUCTION

In recent years, the custom power technology, the low- voltage counterpart of the more widely known flexible ac transmission system (FACTS) technology, aimed at high-voltage power transmission applications, has emerged as a credible solution to solve many of the problems relating to continuity of supply at the end-user level. Both the FACTS and custom power concepts are directly credited to EPRI [1], [2]. At present, a wide range of very flexible controllers, which capitalize on newly available power electronics components, are emerging for custom power applications. Among these, STATCOM is popularly accepted as a reliable reactive power controller replacing conventional var compensators, such as the thyristor-switched capacitor (TSC) and thyristor-controlled reactor (TCR). This device provides reactive power compensation, active power oscillation damping, flicker attenuation, voltage regulation, etc. [3][4]and [5].

The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes [6][7].

1. Voltage regulation and compensation of reactive power

2. Correction of power factor

3. Elimination of current harmonics

Here, such device is employed to provide continuous voltage regulation using an indirectly controlled converter. The single line diagram is shown in fig :1

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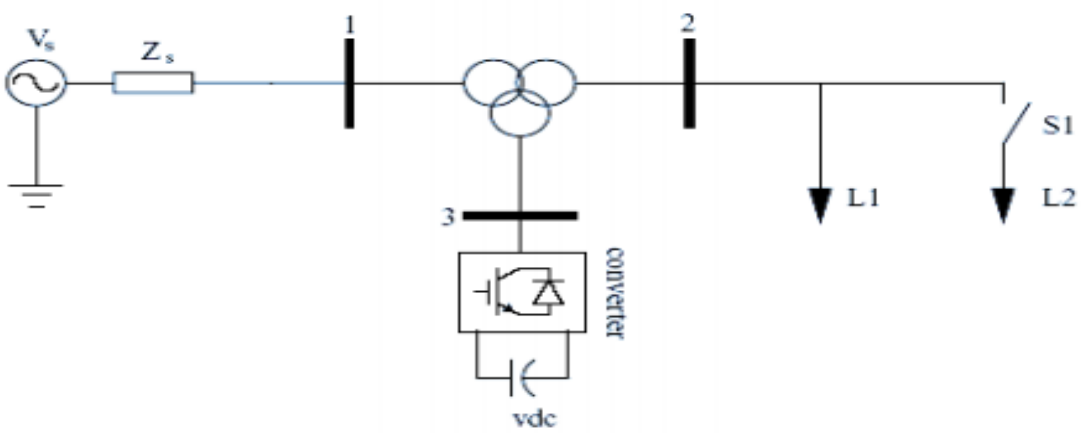

Fig:1 single line diagram of the test STATCOM.

Generally, in high-power applications, Var compensation is achieved using multilevel inverters [8]. These inverters consist of a large number of dc sources which are usually realized by capacitors. Hence, the converters draw a small amount of active power to maintain dc voltage of capacitors and to compensate the losses in the converter. However, due to mismatch in conduction and switching losses of the switching devices, the capacitors voltages are unbalanced. Balancing these voltages is a major research challenge in multilevel inverters. Various control schemes using different topologies are reported in [9]–[10].

Static Var compensation by cascading conventional multi-level/two level inverters is an attractive solution for high-power applications. The topology consists of standard multilevel/two- level inverters connected in cascade through open-end windings of a three-phase transformer. Such topologies are popular in high-power drives [11]. One of the advantages of this topology is that by maintaining asymmetric voltages at the dc links of the inverters, the number of levels in the output voltage waveform can be increased. This improves PQ [12]. Therefore, overall control is simple compared to conventional multilevel inverters. Various var compensation schemes based on this topology are reported in[13]–[14]. In[12], a three-level inverter and two level inverter are connected on either side of the transformer low-voltage winding. The dc-link voltages are maintained by separate converters. In [15], three-level operation is obtained by using standard two-level inverters.

The dc-link voltage balance between the inverters is affected by the reactive power supplied to the grid. In this paper, a static var compensation scheme is proposed for a cascaded two-level inverter-based multilevel inverter. The topology uses standard two-level inverters to achieve multilevel operation. The dc-link voltages of the inverters are regulated at asymmetrical levels to obtain four-level operation. To verify the efficacy of the proposed control strategy, the simulation study is carried out for balanced and unbalanced supply-voltage conditions.

The dc-link voltages of two inverters collapse for certain operating conditions when there is a sudden change in reference current. In order to investigate the behaviour of the converter, the complete dynamic model of the system is developed from the equivalent circuit. The model is linearized and transfer functions are derived from proposed system.

II. CASCADED INVERTER-BASED MULTILEVEL STATCOM

Fig. 2 shows the circuit topology of the cascaded two-level inverter-based multilevel STATCOM using standard two-level inverters. The inverters are connected on the low-voltage (LV) side of the transformer and the high-voltage (HV) side is connected to the grid.

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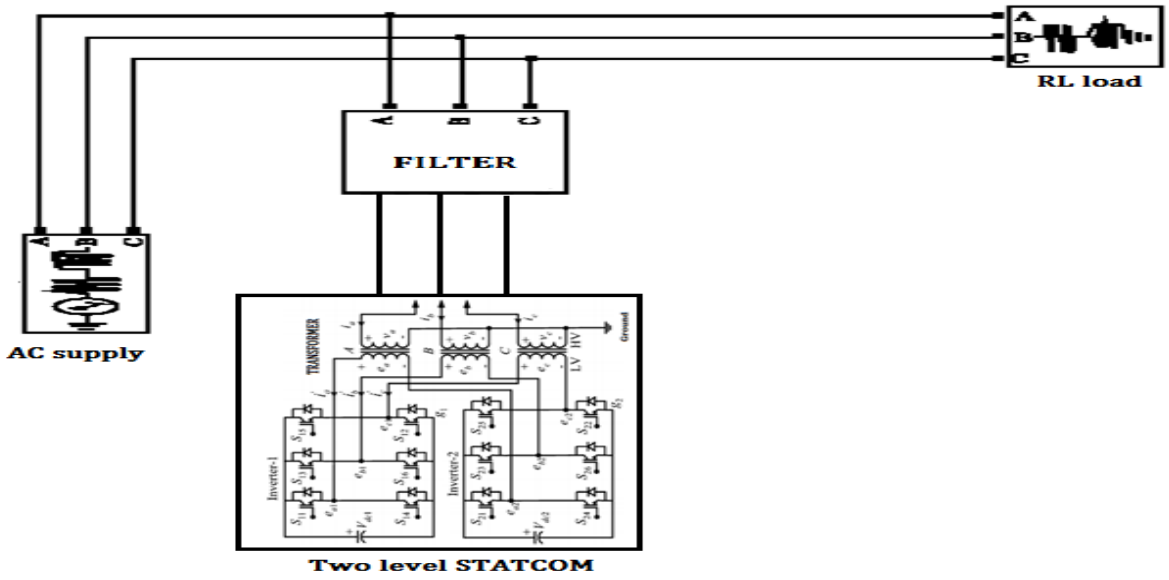

Fig2: Three phase source to load with cascaded multilevel inverter

The dc-link voltages of the inverters are maintained constant and modulation indices are controlled to achieve the required objective.

A: LOAD VOLTAGE CONTROL AND VSC MODULATION

Fig:3 diagram shows the control block for STATCOM in [10], [11], that the closed-loop control is achieved using voltage and current feedback loops. In this paper, a simple output voltage feedback control is used for the control of the load bus voltage. In this scheme, the actual load voltage is fed back and compared with the reference voltage.

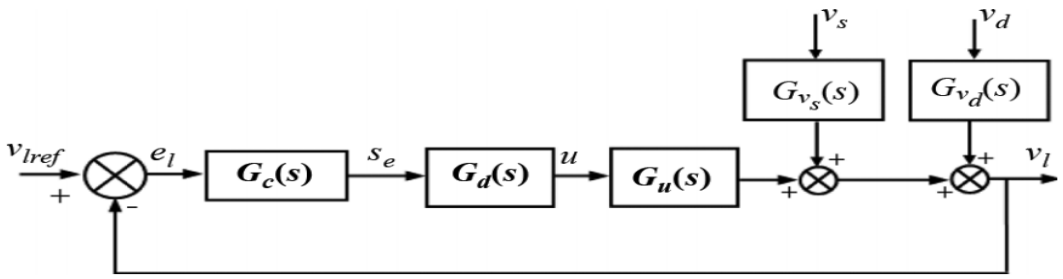

Fig:3 controller circuit

The error so obtained is passed through the proportional plus low-pass-filtered derivative controller to produce a switching function. The s-domain representation of the controller transfer function between the output switching function and the input error function is defined as

$$G_c(s) = \frac{s_{e(s)}}{e_{l(s)}} = k_1 + \frac{K_2 s}{\alpha K_2 s + 1} \quad (1)$$

$$G_d(s) = \frac{k_d}{1 + T_{dS}} \quad (2)$$

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where the error function is defined as . The constants and are the proportional and derivative gains, respectively. The derivative action is associated with the first-order low-pass filter to limit the application of the high-frequency noise and disturbances. The low-pass filtering action depends upon the filter coefficients.

The switching function so obtained is modulated following the phase-shifted multicarrier PWM for the cascaded multilevel converter as given in [17]. The equivalent modulation method used with the two-level converter can be implemented as [11]. The effect of the high-frequency switching due to modulation is modelled as a first-order lag. Therefore, in steady state, the modulation process is defined by a transfer function that consists of a fixed gain and a $1 + T_{dS}$ delay function .

B. DC-Link Balance Controller

The active power transfer between the source and inverter depends on and is usually small in the inverters supplying var to the grid [1]. Therefore, the Q -axis reference voltage component of inverter-2is derived to control the dc-link voltage of inverter-2 as,

The -axis reference voltage component of inverter-1 is obtained as

$$e_1 = \sqrt{e_d^2 + e_q^2} \qquad (3)$$

It results in four-level operation in the output voltage and improves the harmonic spectrum. The reference voltages generated for inverter-2 are in phase opposition to that of inverter-1. From the reference voltages, gate signals are generated using the sinusoidal pulse-width modulation (PWM) technique [15]. Since the two inverters' reference voltages are in phase opposition, the predominant harmonic appears at double the switching frequency.

C. Unbalanced Conditions

As a result, negative-sequence voltage appears in the supply voltage. This causes a double supply frequency component in the dc-link voltage of the inverter. This double frequency component injects the third harmonic component in the ac side [17]. Moreover, due to negative-sequence voltage, large negative-sequence current flows through the inverter which may cause the STATCOM to trip [16][18]. Therefore, during unbalance, the inverter voltages are controlled in such a way that either negative-sequence current flowing into the inverter is eliminated or reduces the unbalance in the grid voltage. In the latter case, STATCOM needs to supply large currents since the interfacing impedance is small. This may lead to trip- ping of the converter.

III. SIMULATION RESULTS

Table:1 Simulation parameter

Parameters	Value (units)
Rated Power	4MVA
Transformer voltages	11kV, 6.6kV
Fundamental Frequency	50Hz
Carrier frequency	2.4kHz
Sampling frequency	15kHz
Inductance (per phase)	18%
Dc link capacitance	75mF
Transformer resistance	3%

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The proposed STATCOM based two level inverter system is studied using MATLAB/ SIMULINK. The overall system configuration and controller are shown in fig 4(a), (b) & (c) for balanced and unbalanced condition. The simulation study is carried out using. The system parameters are given in Table I. In fault condition, a single-phase-to-ground fault is created at time=1.2s to 1.5s, on the phase of the HV side of the 33/11-kV transformer. The fault is cleared after0.3s. Fig. 5(a) (b) and (c) are shows Balanced Single line to ground fault (voltage & current), d-q the-axes components of negative-sequence current and PCC Voltage of the converter. These currents are regulated at zero during the fault condition. Fig. 6(a) (b) and (c) are shows unbalanced Single line to ground fault (voltage & current), d-q the-axes components of negative-sequence current and PCC Voltage of the converter.

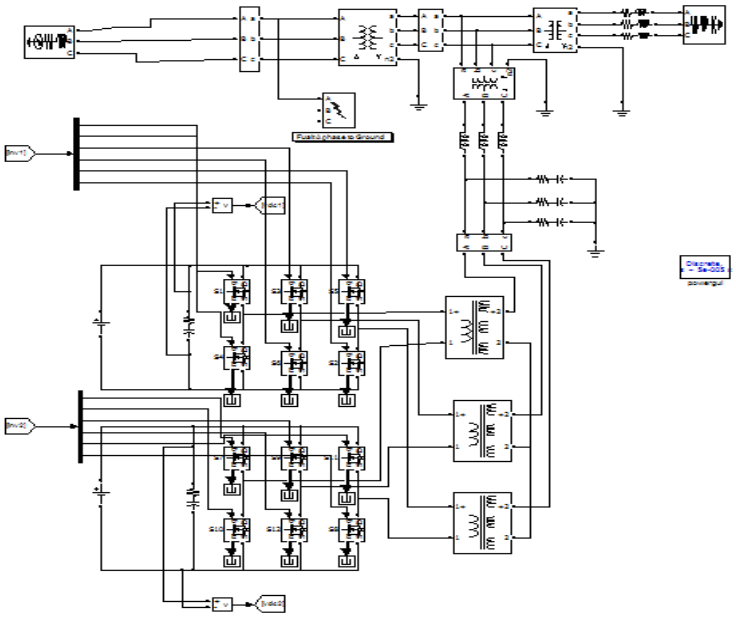
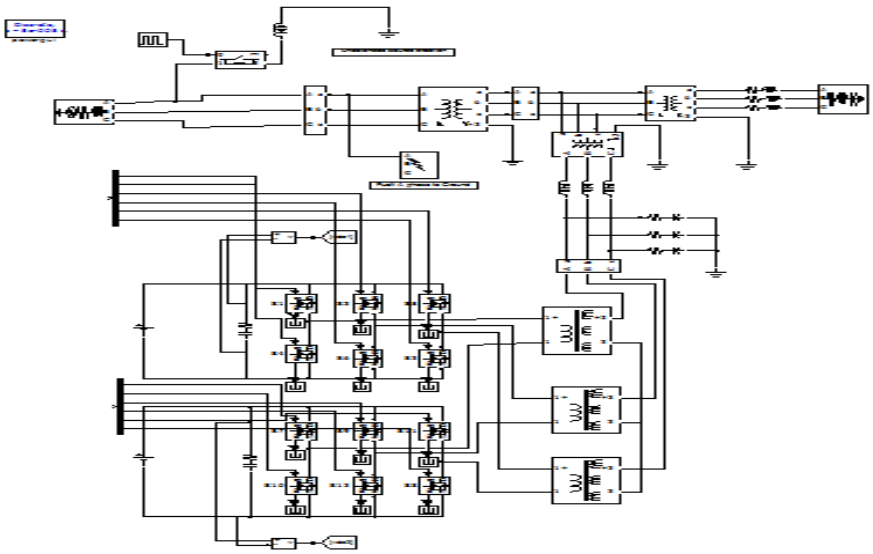


Fig4(a):Circuit diagram for balanced condition



Fig(b):Circuit diagram for unbalanced condition

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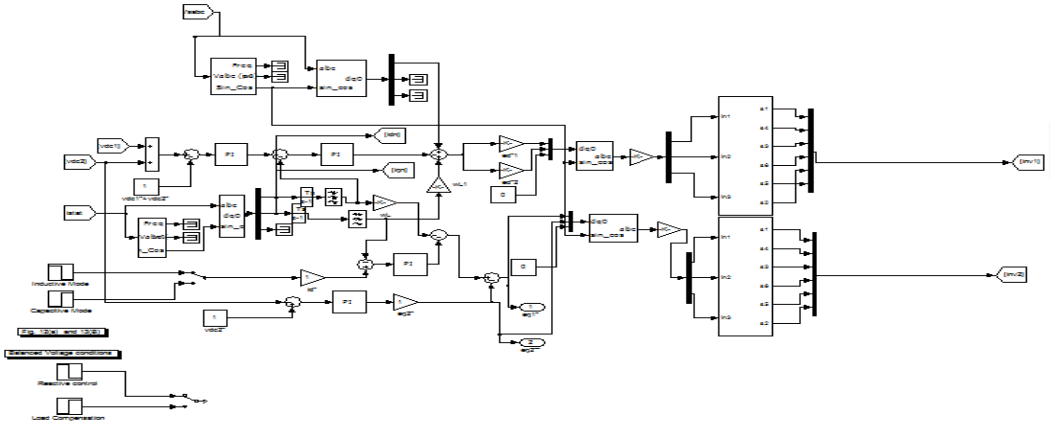

Fig 4(c): Controller circuit diagram

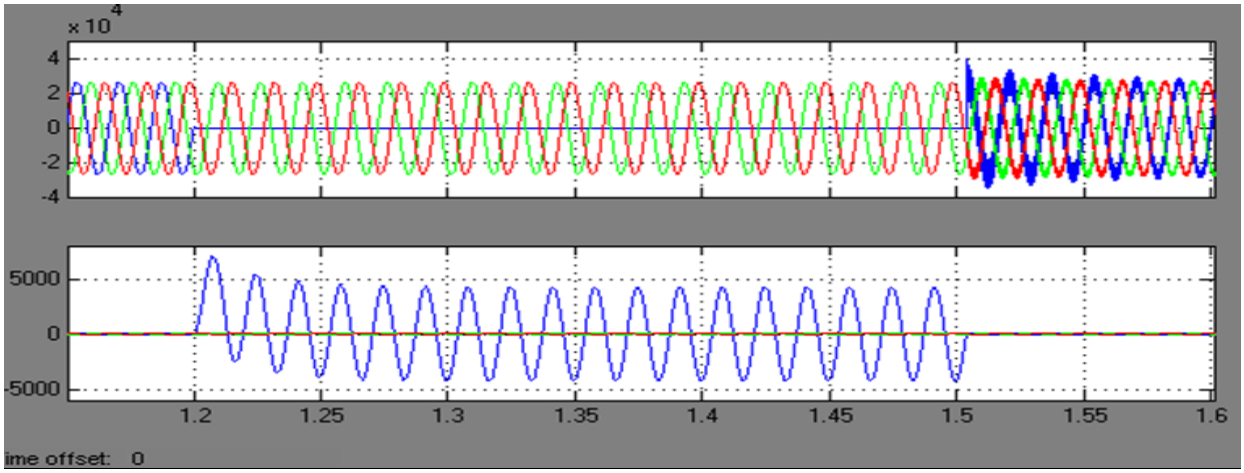

Fig 5(a): Balanced Single line to ground fault(voltage & current)

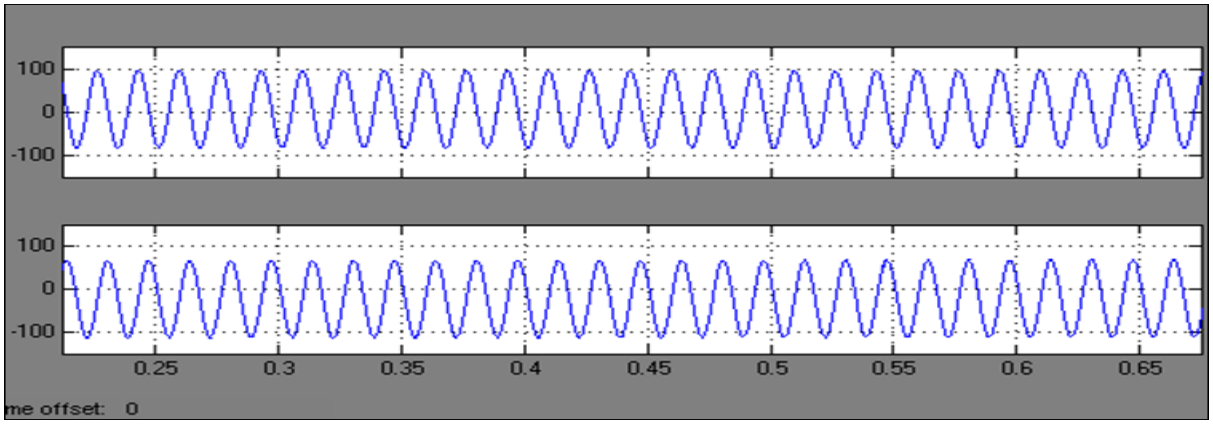

Fig 5(b): Balanced D and Q axis current

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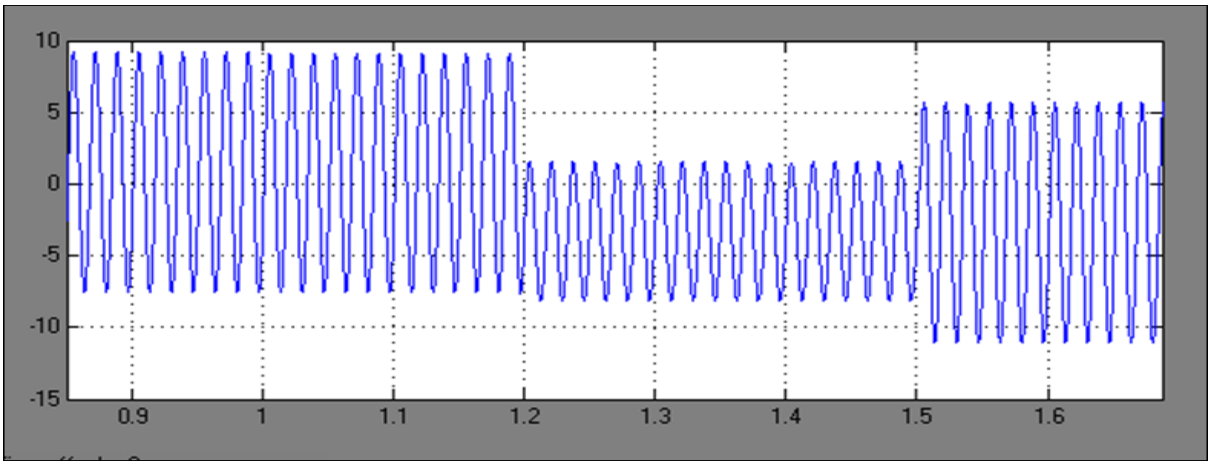

Fig 5(c) :Balanced PCC Voltage

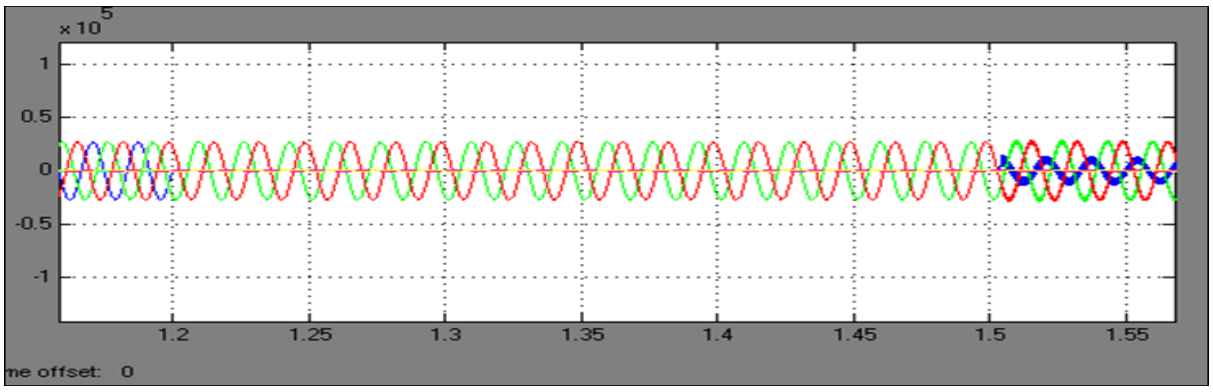

Fig 6(a) :Balanced Single line to ground fault(voltage)

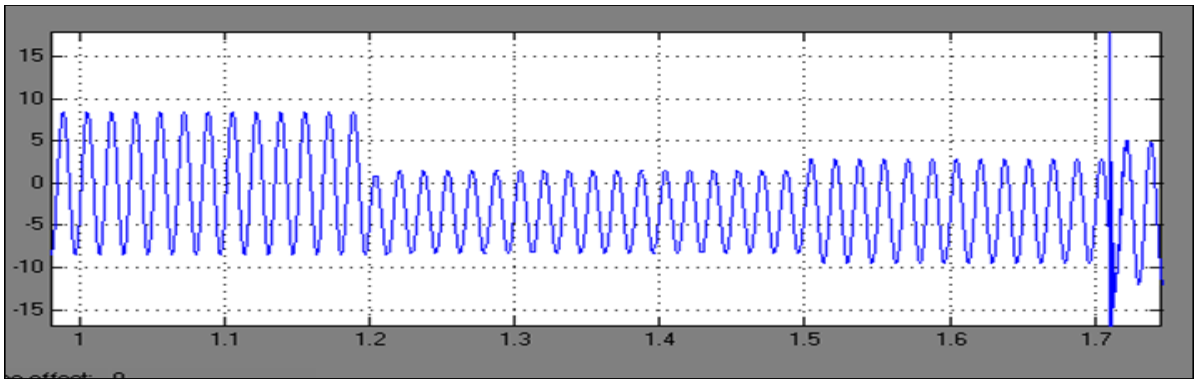

Fig 6(b): BalancedPCC Voltage

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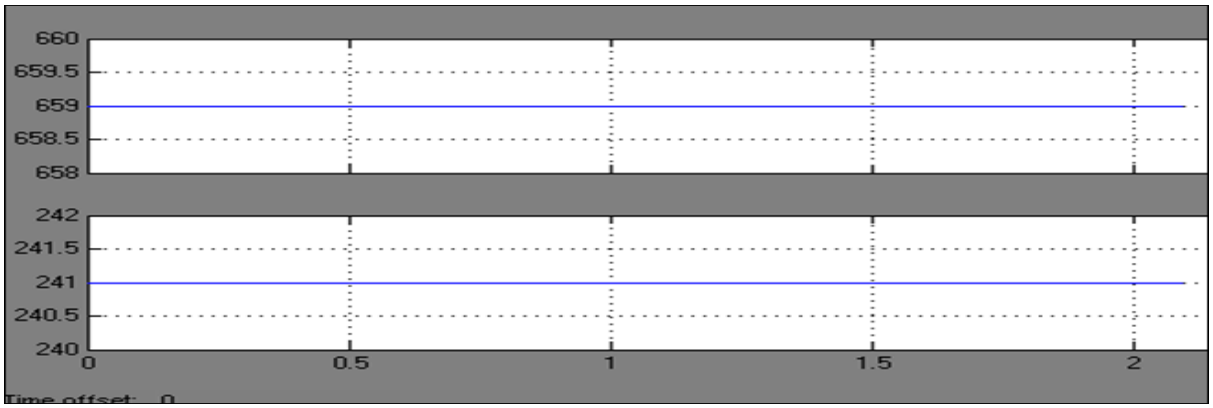

Fig 6(c):unbalanced Dc link voltage (Dc1 and DC 2)

V. CONCLUSION

A simple STATCOM scheme using a cascaded two-level inverter-based multilevel inverter is presented in this paper . The proposed topologies have two VSI based two-level inverters are connected in cascade through open-end windings of a three-phase transformer and filter elements. Converter fed dc-link voltages is regulated at different levels to obtain four-level operation. The proposed STATCOM multilevel inverter has operated under MATLAB/SIMULINK environment and the results are verified in balanced and unbalanced conditions. Further, stability behavior of the topology is investigated. The dynamic model is developed and transfer functions are derived. The system behavior is analyzed for various operating conditions**.**

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