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A Study of FIFO Buffer Adoption Scheme for High Speed Data Links

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ABSTRACT: The FIFO buffer used in high speed data links plays an important role in data transfer and depending upon the application the size of FIFO is variable in nature which known as buffer adoption. There are different buffer adoption schemes for FIFO buffer, some of which are based on goodput, throughput, speed, network natures etc. This paper presents the study of those current various FIFO buffer adoption schemes which employs in current best effort data networks. Also the some proposed works are hereby studied and the conclusion have made by this study. This study work have done in three phase. Firstly the different types of FIFO architecture have studied and present the basic architecture of it. Second the problem identification has been done by literature review of different network architecture proposed. Finally the few best FIFO buffer adoption techniques are studied followed by literature review as extension of it. The RADA scheme is concluded the best buffer adoption scheme among all the papers studied during study.

KEYWORDS: FIFO, FIFO memory depth, Quality of service, RAM, ATM.

I. INTRODUCTION

The name FIFO stands for first in first out and means that the data written into the buffer first comes out of it first. There are other kinds of buffers like the LIFO (last in first out), often called a stack memory, and the shared memory. A FIFO is a special type of buffer. The choice of buffer architecture depends on the application to be solved. FIFOs can be implemented with software or hardware. The choice between software and a hardware solution depends on the application and the features desired. When requirements change, a software FIFO easily can be adapted to them by modifying its program, while a hardware FIFO may demand a new board layout. Software is more flexible than hardware. The advantage of the hardware FIFOs shows in their speed. The FIFO buffer adoption schemes have different dependency parameters like memory depth, speed, throughput, goodput etc. The researches in this field propose some algorithmic solutions and few hardware implementations. The FIFO which is constant in memory length is unable to receive all the data packets during the network congestion of network failure. This problem comprises the different buffer adoption scheme including the large memory buffer, variable memory buffer, packet selection algorithms etc. Thus the new schemes for buffer management have been introduced to satisfy the link requirements of networks. This paper presents a study on the different FIFO buffer adoption schemes which are proposed by the current researchers. And also provide the new area where the work should be done to provide high speed data transfers. circular FIFO buffer architecture is as shown in fig. 1. In which the different sections are shown as read/write pointer control, flag/status control, RAM address with read/write control of data and RAM (memory). The read and write pointers of FIFO are basically circular pointers which overflows and become initial. The RAM memory depth defines the capacity of the FIFO and the status/flag signals indicates the status of the FIFO and RAM memory as EMPTY, FULL, NOPUSH, NOPOP etc. The choice for no. of flag signals are depends upon the user applications. There are different types of FIFO buffer available such as asynchronous read/write, synchronous read/write, simultaneous read/write and non-simultaneous read/write. These are also used as the applications requirement. These above FIFOs are based on the clock signals for read and write operations because some devices use different clock frequencies for read and write operations. Some applications required one operation at a time means if reading of data is going on then writing is in hold and vice versa. This paper shows some buffer management approaches which utilizes the buffer spaces and suggests the modification in FIFO architecture on the basis of application and speed. In this paper the study of various proposed works have been done. The requirement of FIFO buffer management or adoption scheme is due to increase

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the goodput, throughput and speed. Size of the FIFO will always introduce the delay, so it is necessary to manage the resources available with take care of area, speed and other parameters. The basically FIFO buffer can supports the ATM (asynchronous transfer mode) because the handshake signals.

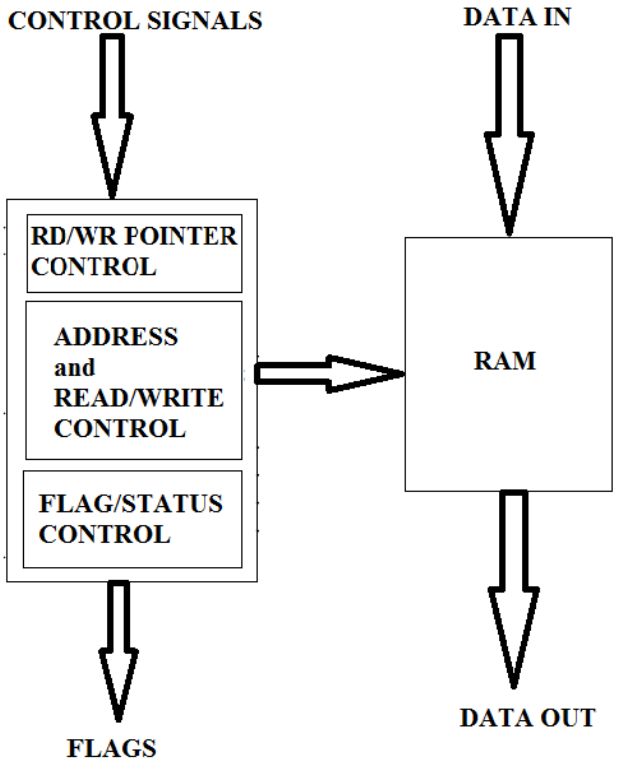

Fig. 1 FIFO buffer architecture.

II. LITERATURE REVIEW

In this section various works with considering the different applications have been studied and represented here. This review sections selected the different new architectures and algorithms for high speed data links. By this the problems related to buffer adoption and delay bounds with data rate have been extracted. Admission Control for Statistical QoS proposed by Shroff et al. [16] in which a buffer-less multiplexer introduces and they conclude economics of scale in the number of multiplexed flows was a crucial component in achieving a high degree of accuracy. They also experimentally observed loss curves (loss probability vs. buffer size). Mehaoual et al. [1], in which a framework for the transport of real-time multimedia trace generated by MPEG-2 applications over ATM networks using an enhanced UBR best effort service (UBR+). Based on encoding MPEG.. They concentrated over minimizing loss of critical video data with bounded end-to-end delay for arriving cells and second, reducing the bad throughput crossing the network during congestion. Dynamic Extended Priority Assignment Scheme (DexPAS), an intelligent packet video drop policy named Nelissen et al [13], in which they suggested different types of switch implementations such as scheduler-based implementations provide a much better performance than the simple switch implementation. Girod et al.[3], in which they concentrated on a several recent advances for channel-adaptive video streaming. their techniques have the common objective of providing efficient, robust, scalable and low-latency streaming video. They conclude three things first, by allowing the client to control the rate at which it consumes data, adaptive media play-out can be used to reduce receiver buffering and therefore average latency, and provide limited rate scalability and secondly, rate-distortion optimized packet scheduling, a transport technique, provides a flexible framework to determine the best packet to send given the channel behaviours, the packets' deadlines, their transmission histories, the distortion reduction associated with sending each packet, and the inter-packet dependencies, thirdly, at the source encoder channel-adaptive packet dependency control can greatly improve the error-resilience of streaming video and reduce latency. [4] Chou et al.

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(2004), in which they introduce an incremental redundancy error-correction scheme that combats the effects of both packet loss and bit errors in an end-to-end fashion, without support from the underlying network or from an intermediate base station ordered to meet an average transmission- rate constraint while minimizing the average end-to-end distortion. Stockhammer et al. [16], in which they worked on the separation between a delay jitter buffer and a decoder buffer is in general suboptimal for VBR video transmitted over VBR channels. They introduced a minimum initial delay and the minimum required buffer for a given video stream and a deterministic VBR channel. Katti et al. [14], in which they suggested COPE, a new architecture for wireless mesh networks. In which the addition to forwarding packets, routers mix (i.e., code) packets from different sources to increase the information content of each transmission are concluded. They show that intelligently mixing packets increases network throughput. Their design is rooted in the theory of network coding. They conclude that COPE can be used in multi-hop wireless networks that satisfy the Memory, Omni-directional antenna and Power requirements. Liu et al. [12], in which they suggested a performance analysis for the PCA protocol, considering the bursty nature of multimedia traffic. The mean frame service time and the mean waiting time of frames belonging to different traffic classes are obtained by them. Their model was applied to delay-sensitive traffic for QoS provisioning. They have focused on the interrelation between the AIFS mechanism specified in PCA and the burstiness/correlation properties in the multimedia traffic. Shi et al. [11] in which they suggested a MAC layer congestion control method to deal with wireless packet loss due to errors (as opposed to congestion). Their mechanism was implemented at the end wireless nodes based on the IEEE 802.11 DCF mechanism but without any modification to the TCP layer. Then they allow their congestion control mechanism to adjust its MAC congestion window based on the contention degree and the packet loss rate at the MAC layer. By improving the channel utilization and increasing congestion window for weak nodes, their mechanism improved the throughput performance and fairness performance significantly. Baiji et al. [2], in which they concluded the energy-efficiency and packet-loss trade-off at physical and medium access control layers. They show how energy-efficiency vs. packet-loss Pareto Frontier can be determined. They set E2 vs. packet-loss MOO problem at PHY and MAC layers and find PF - the set of all points with a property that there are no other points improving any objective without degrading another on. "Adaptive Network Coding for Broadband Wireless Access Networks" [8], in which the authors proposed FASNC scheme and it was evaluated by conducting a series of simulations using the QualNet simulator with a WiMAX module. In their work performance was evaluated in terms of the good-put, decoding delay and buffer requirements, and was compared with that of HARQ-CC (with chase combining), the optimal NCL scheme, and three N-in-1 ReTX schemes. The performance of the FASNC scheme with feedback periods of first, second, and fourth frames given transmitter buffer sizes ranging from 25 to 300 MPDUs. They also concluded the FASNC scheme switches adaptively between M-SNC and MGC on a frame-by-frame basis in order to effectively utilize the available TxOps.

III. VARIOUS BUFFER ADOPTION SCHEMES

Here are some current buffer adoption schemes which are proposed recently by the researchers.

"Buffer management algorithms and performance bounds" [6], suggested the design Criteria By a close examination of the adversaries described in the proofs of Lemmas 1 and 2, one can see that the adversary manages to force any algorithm to drop frames without resorting to forcing the algorithm to do any type of preemption. They also conclude that, the traffic produced by the adversary actually puts the emphasis on the algorithm's ability to discern which packets to accept to the buffer, and which to drop upon arrival. By further examining the adversaries of Lemmas 1 and 2, one can notice that the traffic generated by the adversary forces any algorithm to focus on specific streams/frames, and dropping frames that would eventually turn out to be easier to manage. They conclude that since arrivals are online, the algorithm has no way of discerning these frames at the point it is forced to make a decision. They combining these observations and give the following design criteria for competitive algorithms for the problem:-

1. No-regret policy. Once a frame has a packet admitted to the buffer, make every attempt possible to deliver the complete frame.
2. Ensure progress. Ensure the delivery of a complete frame as early as possible. To implement the first criterion, they will use a dynamic ranking scheme for the traffic. The second criterion takes form in the usage of preemption rules. The balancing between the two criteria is done by a definition of the delicate interplay between the ranking scheme and the preemption rules. They proposed a WEIGHTPRIORITY Algorithm, which follows the design criteria of above two policies.

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"Receiving Buffer Adaptation for High-Speed Data Transfer" [8], in which the authors suggested RADA, a dynamic receiving buffer adaptation scheme for high-speed data transfer. RADA employs an exponential moving average aided scheme to quantify the data arrival rate and consumption rate in the buffer. Based on these two rates, they develop a linear aggressive increase conservative decrease scheme to adjust the buffer size dynamically. In their work also a weighted mean function is employed to make the adjustment adaptive to the available memory in the receiver. They provide theoretical analysis to demonstrate the rationale and parameter bounds of RADA. RADA decides to increase/decrease the buffer when the data arrival rate is constantly faster/slower than the data consumption rate. The adaptation of them was extent in each buffer increase/decrease operation is based on an LAICD scheme, and was also automatically adjusted according to the receiver's memory utilization using a WMF. They suggested three scenarios as following:-

1. Single Transfer Scenario - If the transfer data of no more than 1,000 MB at a certain moment, the optimal buffer size cannot be larger than 500 MB.
2. Loaded Receiver Scenario - when the transfer size reaches 5,000 MB. It requires more time and the 2,000-MB buffer.
3. Multiple Transfers Scenario - RADA with the static buffer scheme when there are multiple simultaneous transfers to the receiver.

"Smoothing Variable-Bit-Rate Video in an Internetwork" [17], in which the authors show how the burstiness of compressed video complicates the provisioning of network resources for emerging multimedia services. They also conclude for stored video applications, the server can smooth the variable-bit-rate stream by transmitting frames into the client playback buffer in advance of each burst. They also worked on the frame lengths and client buffer size, such bandwidth-smoothing techniques can minimize the peak and variability of the rate requirements while avoiding underflow and overflow of the playback buffer. They develop efficient techniques for minimizing the network bandwidth requirements by characterizing how the peak transmission rate varies as a function of the playback delay and the buffer allocation at the two nodes. Drawing on these results they present an efficient algorithm for minimizing both the playback delay and the buffer allocation, subject to a constraint on the peak transmission rate. They also describe how to compute an optimal transmission schedule for a sequence of nodes by solving a collection of independent single-link problems, and show that the optimal resource allocation places all buffers at the ingress and egress nodes. They experiments with motion-JPEG and MPEG traces show the interplay between buffer space, playback delay, and bandwidth requirements for a collection of full-length video traces.

"Buffer management for shared-memory ATM switches" [5], in which the authors stated that in the shared-memory switch architecture, output links share a single large memory. And also in logical FIFO queues were assigned to each link. They also suggested some buffer allocation policies, buffer sharing with Maximum Queue Lengths, SMA (sharing with a minimum allocation) and SMQMA (sharing with a maximum queue and minimum allocation). The above all sharing policies and also some dynamic policies as adaptive control and dynamic threshold related to buffer management scheme were introduced by them.

IV. CONCLUSIONS

The first phase of study, which deals FIFO in short with introduction conclude that the FIFO selection is based on application. Also in this paper we have studied the different current FIFO buffer adoption techniques. In which the RADA [8], scheme is best because it has high goodput and throughput as compared to the WEIGHPRIORITY algorithm [6] where the throughput is high but goodput is low. The RADA scheme does not have the packet selection algorithm compared to [6], which makes it better than others for high memory capacity during network congestion of failure.. The buffer allocation policies [5], is utilize the common buffer memory space during ATM operations which leads to packet overflow during network congestion. [17] is based upon the buffer allocation minimization but the consideration of congestion in network is zero. These most of schemes are based on the algorithms and software level in which particular operating system is responsible for memory allocations. The hardware implementation of FIFO buffer is mostly neglected which leads to low speed.

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V. FUTURE WORKS

The key point in this paper is the modern high speed data requirements using internet links. The all high speed data links are evaluate on the basis of good-put and through-put of packets. The hardware implementation of large memory capacity FIFO buffer is the area on which the future works have to done.

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