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Leakage Power Reduction Using Sleepy Stack Power Gating Technique

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ABSTRACT: The project presents the power gating techniques used for leakage power reduction.The rapid progress in semiconductor technology have led the feature sizes of transistor to be shrunk there by evolution of Deep Sub-Micron (DSM) technology; there by the extremely complex functionality is enabled to be integrated on a single chip. In the growing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements. Leakage power consumption is one of the major technical problem in DSM in CMOS circuit design. A comprehensive study and analysis of various leakage power minimization techniques have been presented in this paper a novel Leakage reduction technique is developed in Tanner EDA tool.

KEYWORDS : Sleep Transistor,Stack Approach,Sleepy Keeper,Leakage Feedback

I. INTRODUCTION

Leakage power consumption of current CMOS technology is already a great challenge. ITRS projects that leakage power consumption may come to dominate total chip power consumption as the technology feature size shrinks. We propose a novel leakage reduction technique, named "sleepy stack," which can be applied to general logic design. Our sleepy stack approach retains exact logic state – making it better than traditional sleep and zigzag techniques – while saving leakage power consumption. Unlike the stack approach (which saves state), the sleepy stack approach can work well with dual-*Vth* technologies, reducing leakage by several orders of magnitude over the stack approach in single-*Vth* technology. Unfortunately, the sleepy stack approach does have a area penalty (roughly 50∼120%) as compared to stack technology; nonetheless, the sleepy stack approach occupies a nice where state-saving and extra low leakage is desired at a (potentially small) cost in terms of increased delay and area.In today's technology, the main contributer to static power consumption of a CMOS circuit is subthreshold leakage, i.e., source to drain current when gate voltage is smaller than the transistor threshold voltage. In this paper, we focus exclusively on reducing subthreshold leakage power. As introduced in Section 1, previously proposed work can be divided into techniques that either (i) preserve state or (ii) destroy state. State-destructive techniques (ii) cut off transistor (pull-up or pull-down or both) networks from supply voltage or ground using sleep transistors. These types of techniques are also called gated-*VDD* (note that a gated clock is generally used for dynamic power reduction).

Motoh et al. propose a technique called multi-thresholdvoltage CMOS (MTCMOS), which adds high *Vth* sleep transistors between pullup networks and *VDD* and between pull-down networks and ground while logic 150 J.C. Park, V.J. Mooney, and P. Pfeiffenberger circuits use low *Vth* to maintain logic performance .The sleep transistor is turned off when the logic circuits are not in use. Powell et al. propose a gated-*VDD* cache technique called DRI cache, which dynamically changes cache size with gated-*VDD* transistors of dual or single *Vth*. Since the gated-*VDD* technique cuts off logic blocks from *VDD* and *Gnd*, time and energy for waking up are significant. The zigzag technique proposes the reduction of wake-up overhead by choosing a particular circuit state (e.g., corresponding to a "reset") and then, for the exact circuit state chosen, cutting off the pull-down network for each gate whose output is high while conversely cutting off the pull-up network for each gate whose output is low.Although the zigzag technique can retain a particular state chosen prior to chip fabrication, any other arbitrary state during regular operation is lost in power-down mode.

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Another technique to reduce leakage power is transistor stacking that exploits the stack effect, i.e., it turns out that two stacked and turned off transistors reduce subthreshold leakage current substantially due mainly to a reverse bias between the gate and source.

II. RELATED WORK

A. Data-Driven Clock Gating

Clock enabling signals are very well understood at the system level and thus can effectively be defined and capture the periods where functional blocks and modules do not need to be clocked. Those are later being automatically synthesized into clock enabling signals at the gate level. In many cases, clock enabling signals are manually added for every FF as a part of a design methodology.

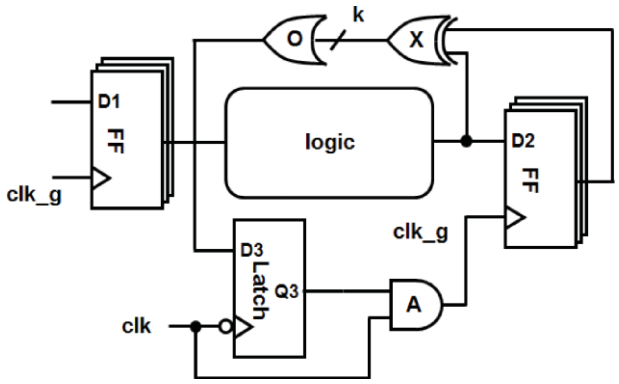

Fig.1.Practical data-driven clock gating

A FF finds out that its clock can be disabled in the next cycle by XORing its output with the present data input that will appear at its output in the next cycle. The outputs of *k* XOR gates are ORed to generate a joint gating signal for *k* FFs, which is then latched to avoid glitches. The combination of a latch with AND gate is commonly used by commercial tools and is called integrated clock gate (ICG). Such datadriven gating is used for a digital filter in an ultralow-power design. A single ICG is amortized over *k* FFs.

Knowing the optimal group size *k*, the next step is to partition the FFs of a system into *k*-size sets such that the power savings will be maximized. Grouping FFs for joint clock gating as a part of the physical layout synthesis. Such tools are focusing on skew, power, and area minimization, but they are not aware of the toggling correlations of the underlying FFs, which this paper is focusing on.

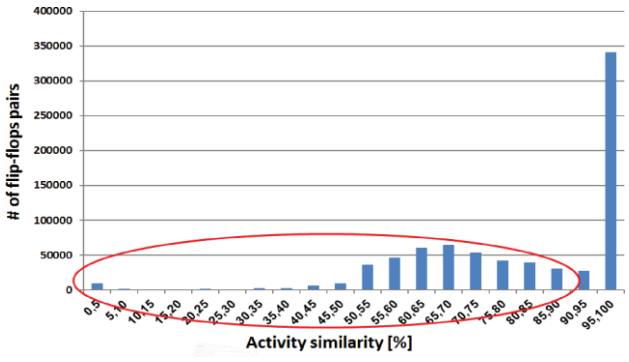

Fig.2.Activity similarity of FFs in a DSP core

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FFs are paired only if they share same pre-enabled clock signal. Undesirable pairs are Encircled. Notice that different pre-enabled clock signals may have a different duration *m* of enabled window.As expected, the activity similarity is very high, mostly due to the very low FFs' toggling during their enabled clock window.Still, highly active and uncorrelated FF pairs exist and are encircled. A good FFs grouping algorithm should avoid putting the FFs of an encircled pair into the same group.

Data-driven clock gating is shown to achieve savings of more than 10% of the total dynamic power consumed by the clock tree. Data driven clock gating for digita filters achieves 20% power savings.The gating logic is tailored to the structure of the filter, whereas the approach discussed in this paper is more general and applies to large scale and a wide range of designs.

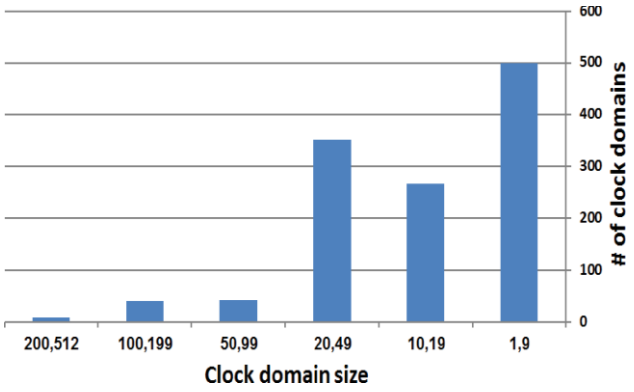

Fig.3.Distribution of the number of FFs sharing a common pre-enabled clock signal of a DSP core

III. PROPOSED MODEL

A.Power Gating Technique

New low power solutions for Very Large Scale Integration (VLSI) are proposed. Especially, we focus on leakage power reduction. Although neglected at 0.18u technology and above, leakage power is nearly equal to dynamic power consumption in nanoscale technology, e.g., 0.07u. We present a novel circuit structure, we call it sleepy stack, which is a combination of two well-known low-leakage techniques: the forced stack and sleeptransistortechniques.

B.Sleep approach

Sleep approach is used for reduction of gate oxide and sub threshold leakage current in DSM technology.Sleep approach is used to rail off the circuit from Vdd to ground, so we insert a PMOS transistor above pull up network and Vdd and NMOS transistor below pull down Network and GND.During standby mode a sleep transistor turns off turn off and rail from Vdd and reduces the leakage current.During active mode we ON the sleep transistor and direct connection of circuit with Vdd, so increase the performance of the circuit and Reduces the leakage power efficiently.Unlike the forced stack technique, the sleepy stack technique can utilize high-Vth transistors without incurring a large delay increase.

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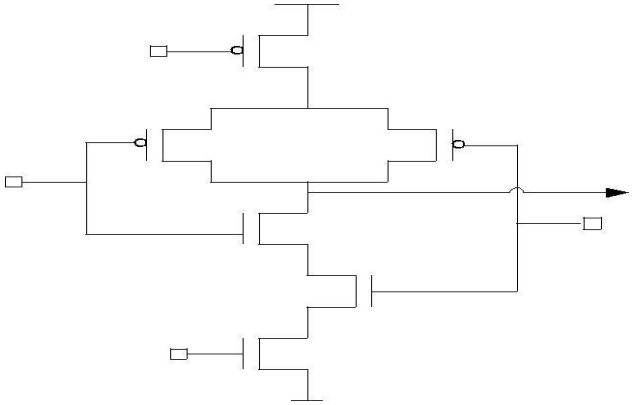

Fig.4. Sleep Approach NAND Gate

C.Stack Approach

Force stack is another approach for further leakage reduction, in this approach we provide the stacking of the transistor, we divide pull up and pull down network into two half size. The dividing of the transistor will not affect the W/L ratio of the circuit, The W/L ratio of the circuit is maintained after dividing of the circuit. For better Leakage saving we divide pull up PMOS network which provide the stacking of the transistor, same process of dividing is also done in pulldown network serially.

Also, unlike the sleep transistor technique, the sleepy stack technique can retain exact logic state while achieving similar leakage power savings. In short, our sleepy stack structure achieves ultra-low leakage power consumption while retaining logic state. We apply the sleepy stack technique to both generic logic circuits as well as SRAM. At 0.07u technology, the sleepy stack logic circuits achieves up to 200X leakage reduction compared the forced stack technique with small (under 7%) delay variations and 51~118% area overheads. The sleepy stack SRAM cell with 1.5xVth achieves 5X leakage reduction with 32% delay increase or 2.49X leakage reduction without delay increase compared to the high-Vth SRAM cell. As such, the sleepy stack technique can be applicable to a design that requires ultra-low leakage power with quick response time while paying area and delay cost.

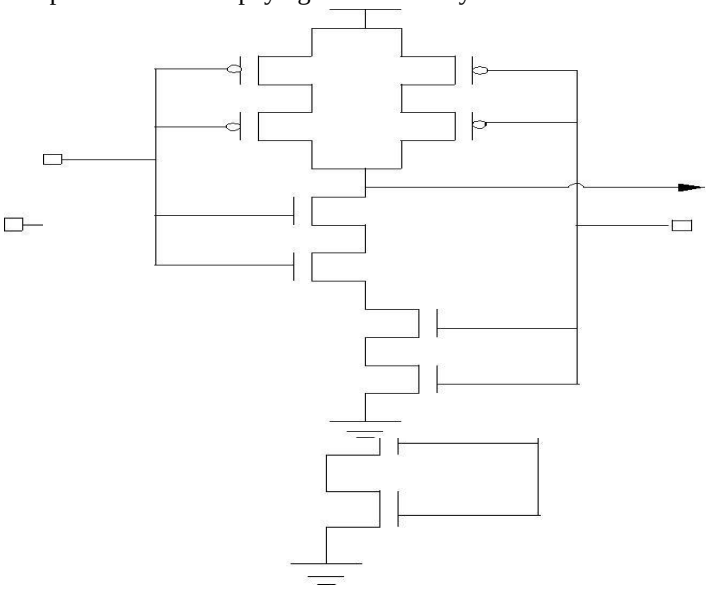

Fig.5.Stack Approach based 2 input NAND gate

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We achieve 20.43% processor dynamic energy savings with 4.14% execution cycle increase using 2-stage low-Vdd LPPC. Furthermore, we apply LPPC to the sleepy stack SRAM. The sleepy stack pipelined SRAM achieves 17X leakage power reduction while increasing execution time by 4% on average. Although this combined technique increases active power consumption by 33%, this technique is well suited for the system that spends most of its time in sleep mode. Static power consumption is a major concern in nanometer technologies. Along with technology scaling down and higher operating speeds of CMOS VLSI circuits, the leakage power is getting enhanced. As process geometries are becoming smaller, device density increases and threshold voltage as well as oxide thickness decrease to keep pace with performance.

D.Leakage Feedback Approach

Another Leakage reduction technique is leakage feedback approach; In this approach we use two parallel PMOS transistor above pull up network and Vdd . To provide the inverting output of the circuit we connect inverter at the output, an inverter provides the proper logic feedback to both pull down NMOS(S') and pull up PMOS(S) sleep transistor. This two transistor enhance the circuit performance and maintain the proper logic of the circuit during standby mode. In standby mode one of the transistor of parallel sleep transistor turn off both NMOS and PMOS, the output of the circuit is pass through inverter which keep ON one of the sleep transistor which is connected parallel by providing the proper feedback approach. Hence circuit is active in standby mode, we mitigate the various leakage current which flow during standby mode and increase the performance of the circuit.

E.Sleepy Keeper Approach

Above all this approach the most efficient approach for leakage power reduction is the sleepy keeper approach. In this approach combination of PMOS and NMOS transistor which is connected paralleled inserted between pull up network and Vdd and pull down and GND, NMOS transistor of pull up sleep transistor connected PMOS pull down sleep transistor. As NMOS sleep transistor which rail off the path from Vdd to GND is connected to GND and PMOS transistor which is connected to Vdd, NMOS transistor is not turn ON that's why it will not efficiently pass Vdd, this problem can be overcome by maintaining output value "1" in sleep mode by connecting NMOS to Vdd. PMOS transistor which is connected to the pull up NMOS transistor and GND which is parallel to NMOS sleep transistor, to maintain output value equal to "0" in sleep mode.This approach reduces the leakage power efficiently and maintains the proper logic of the circuit with lesser area.

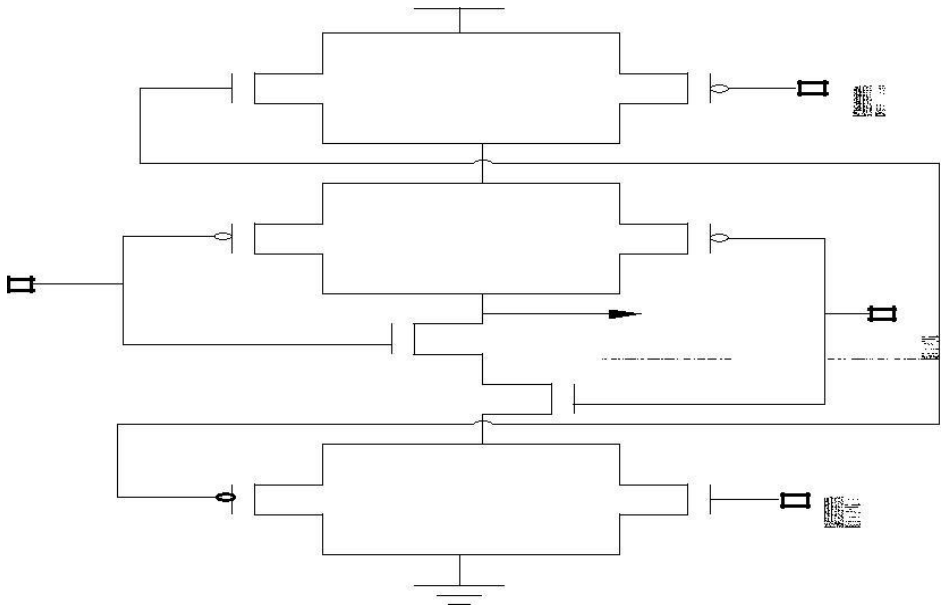

Fig.6. Sleepy keeper Approach based 2 input NAND gate

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IV. SIMULATION RESULTS

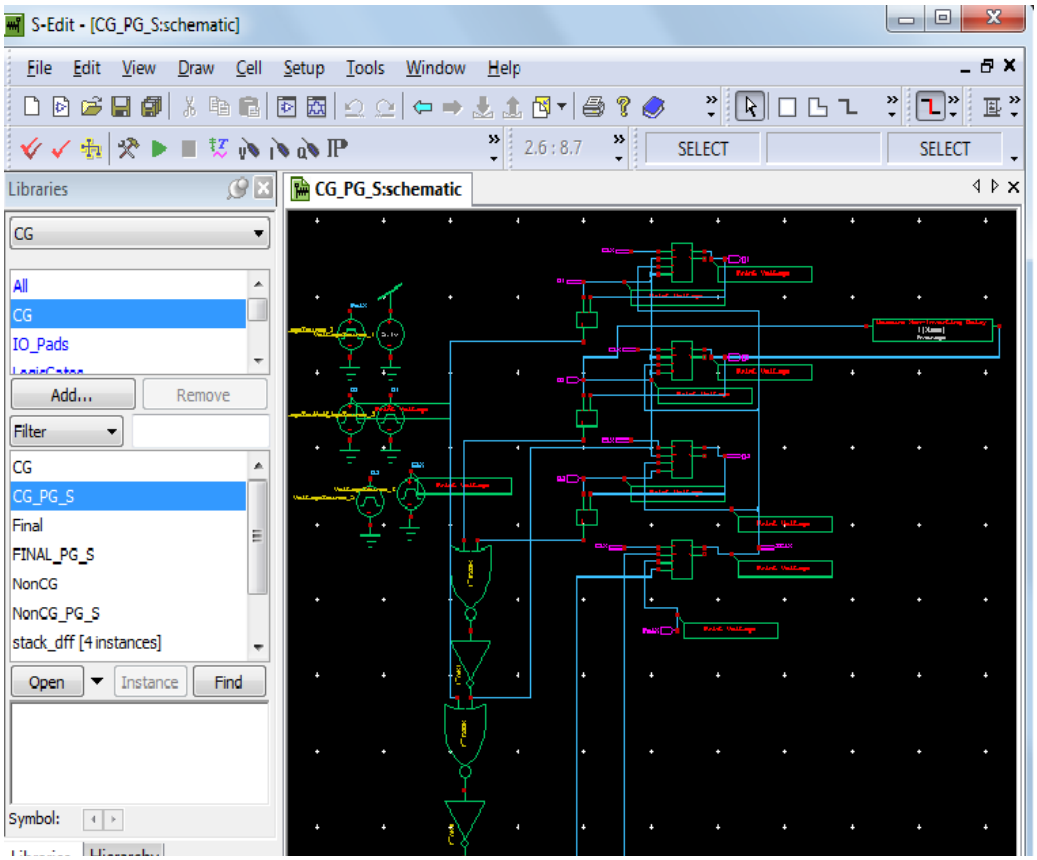

Fig.7.Power Gating Circuit

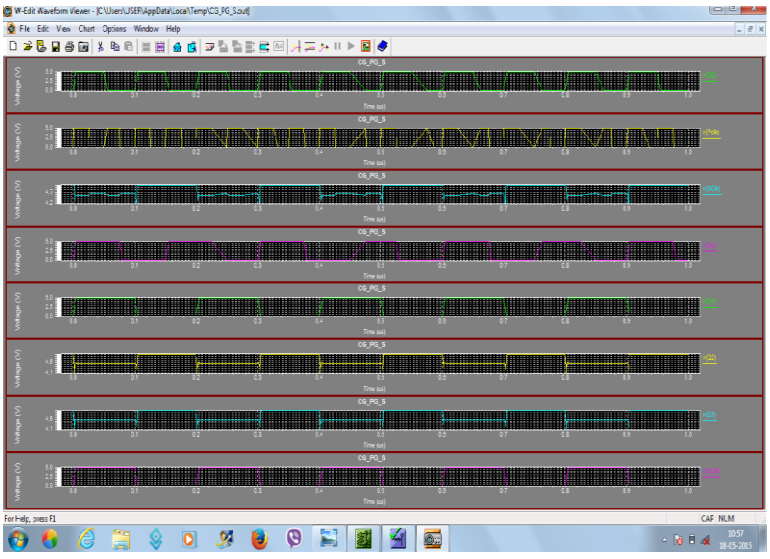

Fig.8.Waveform of Power Gating Circuit

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IV. CONCLUSION

In nanometer scale CMOS technology, subthreshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques base upon technology and design criteria. Our novel sleepy stack, which combines the sleep and the stack approaches, is proposed as a new choice for logic designers. Furthermore, the sleepy stack is applicable to single and multiple threshold voltages. In conclusion, the sleepy stack combine some of the advantages of sleep transistors most notably the effective use of dual-*Vth* technology with some of the advantages of the stack approach most notably the ability to save state. As such, the sleepy stack approach represents a new weapon in the VLSI designer's repertoire.

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