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Closed Loop Control of Transformer-Less Adaptable Voltage Quadrupler DC Boost Converter

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ABSTRACT: The work focused on the development of a transformer-less adjustable voltage quadrupler dc boost converter with PI controller to enhance high-voltage transfer gain and reduced semiconductor voltage stress is proposed. The proposed topology utilizes input-parallel output-series configuration for providing a much higher voltage gain without adopting an extreme large duty cycle. The projected converter cannot only achieve high step-up voltage gain with reduced number of component. It also reduces the voltage stress of both active switches and diodes. This will allow to choose lower voltage rating of MOSFETs and diodes to reduce both switching and conduction losses. Closed loop PI controller is used to achieve the desired output voltage. The operation principle and steady analysis as well as a comparison with other recent existing high step-up topologies are presented. Experimental and simulation and results are presented to demonstrate the effectiveness of the proposed converter.

KEYWORDS: Voltage Quadrupler, DC Boost Converter, Closed Loop, PI Controller..

I.INTRODUCTION

For Global energy shortage a renewable energy sources such as solar cells and fuel cells are increasingly widely used. However, owing to the inherent low voltage characteristic of these sources, a high step-up dc converter is essential as a pre stage of the corresponding power conditioner. The conventional boost and buck–boost converters, due to the degradation in the overall efficiency as the duty ratio approaches unity [1]. Moreover, the extreme duty ratio not only induces very large voltage spikes and increases conduction losses but also induces severe diode reverse-recovery problem [2], [3]. A simple isolated structure with a high step-up voltage gain is dc-dc fly back converter, because of the leakage inductance of the transformer converter will suffer a high voltage stress. Some energy-regeneration techniques have been proposed to clamp the voltage stress on the active switch and to recycle the leakage inductance [5,6,7].

To achieve a high step-up gain by increasing the turns ratio of the transformers some isolated voltage type converters are existing such as the phase shifted full bridge converters. Unfortunately, the large amount of input current ripple will reduce the maximum output power and cut down the usage life of input electrolytic capacitor. more input electrolytic capacitors are required to suppress the large input current ripple. In additional to that, the circuit efficiency is degraded because of high output diode voltage stress than the output voltage in the high-output-voltage applications. Other isolated current-type converters are existing such as the active-clamp dual-boost converters and the active-clamp full-bridge boost converters [8], [9], can realize high efficiency and high step-up conversion. Because of many extra power components causes to increase the cost. In order to reduce system cost and to improve system efficiency a non-isolated dc/dc converter is a suitable solution [10][11]. The switched capacitor-based converters proposed [12].
To improve the conversion efficiency and achieve large voltage conversion ratio. Numeral aspects are arises because of the usage of conventional switched capacitor are suffering high transient current and large conditional losses. Some converter topologies were presented based on a switched capacitor cell concept in which a soft switched scheme was used to reduce the switching loss & electromagnetic interference [35],[36].

Some interleaved high step-up converters with coupled inductors are introduced to derive more compact circuit structure [22]. To achieve higher voltage conversion ratio and further reduce voltage stress on the switch and diode, the

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high step-up ratio converter [25] and the ultrahigh step-up converter [26] have been proposed. These converters can provide large step-up voltage conversion ratios. Unfortunately, the voltage stress of diodes in those converters remains rather high.

In this paper, a transformer-less adaptable voltage quadrupler topology is proposed. It integrates two-phase interleaved boost converter to realize a high voltage gain and maintain the advantage of an automatic current sharing capability simultaneously. Furthermore, the voltage stress of active switches and diodes in the proposed converter can be greatly reduced to enhance overall conversion efficiency. First, the circuit topology and operation principle are given in Section II. Then, the corresponding steady-state analysis is made in Section III to provide some basic converter characteristics. A prototype is then constructed and some simulation and experimental results are then presented in Section IV for demonstrating the merits and validity of the proposed converter. Finally, some conclusions are offered in the last section.

A. Existing System

The conventional boost and buck-boost converters, due to the degradation in the overall efficiency as the duty ratio approaches unity. Besides, the extreme duty ratio not only induces very large spikes and increases conduction losses but also induces severe diode reverse – recovery problem. Active switch of high step-up voltage gain will suffer a high voltage stress due to leakage inductance of the transformer. Output diode voltage stress is much higher than the output voltage, which will degrade the circuit efficiency in the high output voltage applications. Cost is increased because extra power components and isolated sensors or feedback controllers are required. .

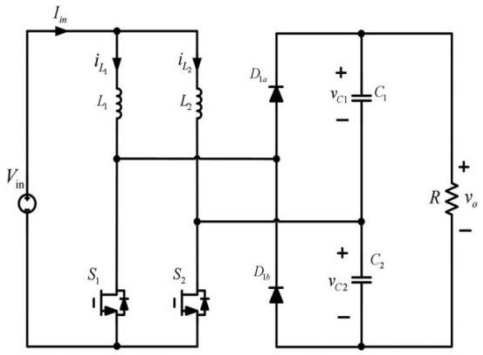

Fig.1. Configuration of Existing System.

SHORTCOMING OF EXISTING SYSTEM

- Active switch suffer high voltage stress due to leakage induction of Transformer.
- To achieve High step up gain by increasing the turns ratio of Transformer.
- Very large voltage spikes increases the conduction losses but also induces severe diode reverse recovery problem.
- Input current ripple is relatively high.
- Higher input current ripple will reduce the maximum output power and shorten the usage life of input electrolytic capacitor.
- Higher output voltage stress will degrade the circuit efficiency.
- Cost is high due to extra power components.

B. Proposed System

- With Global energy shortage and strong environmental movements, renewable or clean energy sources such as solar cells and fuel cells are increasingly valued worldwide.
- However due to the inherent low voltage characteristic of these sources, A Transformer – less DC Boost converter with low switch voltage stress to enhance efficiency has been proposed.

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- The proposed topology utilizes input-parallel output-series configuration for providing a much higher voltage gain without adopting an extreme large duty cycle.
- The proposed converter cannot only achieve high step up voltage gain with reduced component count but also reduce the voltage stress of both active switches and diodes.
- This will allow to choose lower voltage rating MOSFETs and Diodes to reduce both switching and conduction losses.

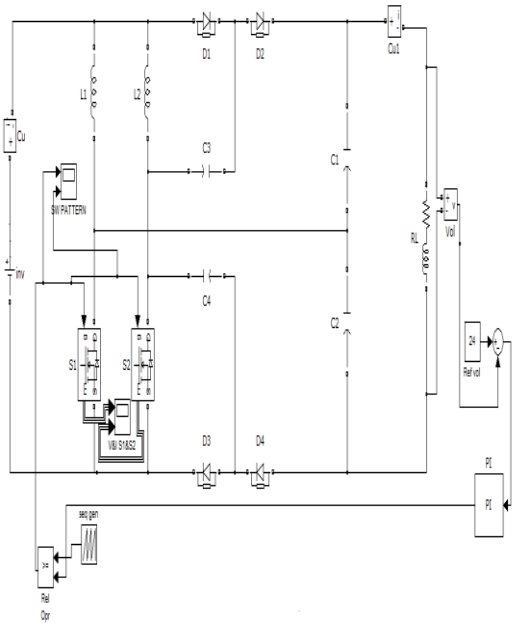

Fig.2. Circuit diagram of Proposed system.

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

For convenient reference, the two-phase interleaved boost converter with parallel-input series-output connection is first shown in Fig. 1(a). The proposed converter topology is basically derived from a two-phase interleaved boost converter and is shown in Fig. 1(b). Comparing Fig. 1(a) with Fig. 1(b), one can see that two more capacitors and two more diodes are added so that during the energy transfer period partial inductor stored energy is stored in one capacitor and partial inductor stored energy together with the other capacitor store energy is transferred to the output to achieve much higher voltage gain. However, the proposed voltage gain is twice that of the interleaved two-phase boost converter. Also, the voltage stress of both active switches and diodes are much lower than the latter. Furthermore, as will be obvious latter, the proposed converter possesses automatic uniform current sharing capability without adding extra circuitry or complex control methods. The detailed operating principle can be illustrated as follows.

The proposed converter topology, like any existing high step-up dc converter, possesses the drawback of existence of pulsating output period. Furthermore, as the main objective is to obtain high voltage gain and such characteristic can only be achieved when the duty cycle is greater than 0.5 and in continuous conduction mode (CCM); hence, the steady-state analysis is made only for this case. However, with duty cycle lower than 0.5 or in DCM, as there is no enough energy transfer from the inductors to the blocking capacitors, output capacitors, and load side, and consequently it is not possible to get the high voltage gain as that for duty ratio greater than 0.5. In addition, only with duty cycle larger than 0.5, due to the charge balance of the blocking capacitor, the converter can feature the automatic current sharing characteristic that can obviate any extra current-sharing control circuit. On the other hand, when duty cycle is smaller than 0.5, the converter does not possess the automatic current sharing capability any more,and the current-sharing control between each phases should be taken into a account in this condition.

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In order to simplify the circuit analysis of the proposed converter, some assumes are made as follows:

1) All components are ideal components
2) The capacitors are sufficiently large, such that the voltages across them can be considered as constant approximately.
3) The system is under steady state and is operating in CCM and with duty ratio being greater than 0.5 for high step-up

Basically, the operating principle of the proposed converter can be classified into four operation modes. The interleaved gating signals with a 180° phase shift as well as some key operating waveforms are shown in Fig. 2

A. Mode 1 ($t0 \le t<t1$):

For mode 1, switches S1 and S2 are turned ON, D1a,D1b,D2a,D2b are all OFF. The corresponding equivalent circuit is shown in Fig. 3(a). From Fig. 3(a), it is seen that both iL1 and iL2 are increasing to store energy in L1 and L2, respectively. The voltages across diodes D1a and D2a are clamped to capacitor voltage VCA and VCB, respectively, and the voltages across the diodes D1b and D2b are clamped to VC 2 minus VCB and VC 1 minus VCA, respectively. Also, the load power is supplied from capacitors C1 and C2. The corresponding state equations are given as follows:

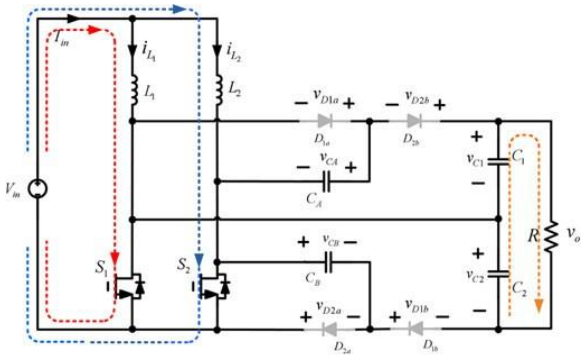

Fig.3. Mode I & III Operation.

$$C_A \frac{dv_{C_A}}{dt} = 0$$

$$C_B \frac{dv_{C_B}}{dt} = 0$$

$$C_1 \frac{dv_{C_1}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R}$$

$$C_2 \frac{dv_{C_2}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R}$$

B. Mode 2 ($t_1 \le t < t_2$) :

For this operation mode, switch S_1 remains conducting and S_2 is turned OFF. Diodes D_{2a} and D_{2b} become conducting. The corresponding equivalent circuit. It is seen from that part of stored Energy in inductor L_2 as well as the stored energy of C_A is now released to output capacitor C_1 and load. Meanwhile, part of stored energy in inductor L_2 is stored in C_B. In this mode, capacitor voltage V_{C1} is equal to V_{CB} plus V_{CA}. Thus, i_{L1} still increases continuously and i_{L2} decreases linearly. The corresponding state equations are given as follows:

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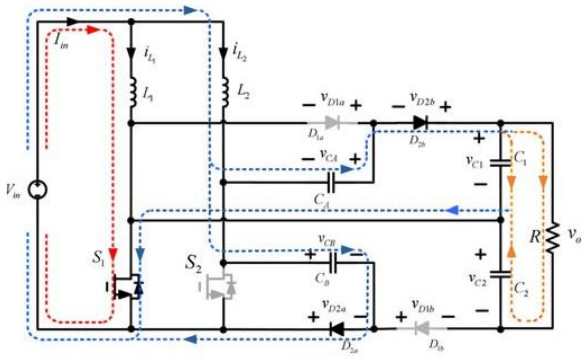

Fig.4. Mode II Operation.

$$L_2 \frac{di_{L2}}{dt} = V_{\text{in}} + v_{C_A} - v_{C_1} = V_{\text{in}} - v_{C_B}$$

$$C_A \frac{dv_{C_A}}{dt} = i_{C_B} - i_{L_2}$$

$$C_B \frac{dv_{C_B}}{dt} = i_{C_A} + i_{L_2}$$

$$C_1 \frac{dv_{C_1}}{dt} = -i_{C_A} - \frac{(v_{C_1} + v_{C_2})}{R}$$

$$C_2 \frac{dv_{C_2}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R}.$$

C. Mode 3 ($t_2 \leq t < t_3$):

For this operation mode, as can be observed, both S_1 and S_2 are turned ON. The corresponding equivalent circuit turns out to be the same.

D.Mode 4 ($t_3 \leq t < t_4$) :

For this operation mode, switch S_2 remains conducting and S_1 is turned OFF. Diodes D_{1a} and D_{1b} become conducting. The corresponding equivalent circuit. It is seen from that the part of stored energy in inductor L_1 as well as the stored energy of C_B is now released to output capacitor C_2 and load. Meanwhile, part of stored energy in inductor L_1 is stored in C_A. In this mode, the output capacitor voltage V_{C2} is equal to V_{CB} plus V_{CA}. Thus, i_{L2} still increases continuously and i_{L1} decreases linearly. The corresponding state equations are given as follows:

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(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2015

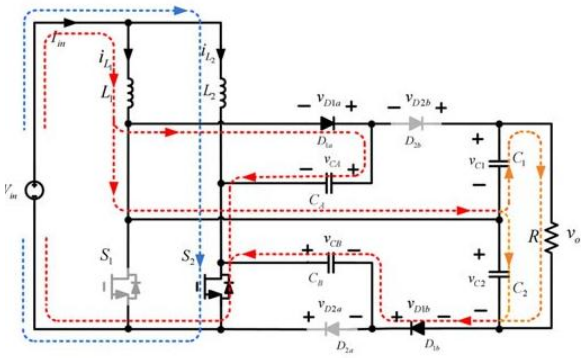

Fig.5. Mode IV Operation.

$$L_1 \frac{di_{L1}}{dt} = V_{in} - v_{C_2} + v_{C_B} = V_{in} - v_{C_A}$$

$$C_A \frac{dv_{C_A}}{dt} = i_{C_B} + i_{L_1}$$

$$C_B \frac{dv_{C_B}}{dt} = i_{C_A} - i_{L_1}$$

$$C_1 \frac{dv_{C_1}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R}$$

$$C_2 \frac{dv_{C_2}}{dt} = -i_{C_B} - \frac{(v_{C_1} + v_{C_2})}{R}$$

III. PERFORMANCE COMPARISON

From the above illustration of the proposed converter, one can see that the operations of two-phase are both symmetric and rather easy to implement. Also, from key operating waveforms of the proposed converter. One can see the low voltage stress of two active switches and four diodes as well as the uniform current sharing.

For demonstrating the performance of the proposed converter, the proposed converter is compared with some recent high step up converters. Summarize the voltage gain and normalized voltage stress of active as well as passive switches for reference.

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International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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Vol. 4, Issue 3, March 2015

Table.1 Comparison of the Steady State Characteristics

Gain/stress	Voltage Doubler [24]	High step-up ratio converter [25]	Ultra high step-up converter [26]	Proposed converter
Voltage gain	$\frac{2}{(1-D)}$	$\frac{3-D}{(1-D)}$	$\frac{3+D}{(1-D)}$	$\frac{4}{(1-D)}$
Voltage stress of switches	$\frac{1}{2}$	$\frac{1}{(3-D)}$	$\frac{2}{(3+D)}$	$\frac{1}{4}$
Voltage stress of diodes	1	$\frac{2}{(3-D)}$	$\frac{2}{(3+D)}$	$\frac{1}{2}$
numbers of MOSFETs	2	2	1	2
numbers of inductors	2	2	2	2
numbers of diodes	2	3	5	4
numbers of capacitors	2	3	4	4

For comparison, the voltage stress is normalized by the output voltage V_O , the voltage gains, the normalized switch stresses and the normalized output diode stresses of the conventional voltage-doubler, high step-up ratio converter , and the ultrahigh step-up converter are also shown in the same figure to provide better view. It is seen from that the proposed converter can achieve higher voltage gain than that of the other three boost converters. Therefore, the proposed converter is rather suitable for use in applications requiring high step-up voltage gain. From, one can see that the proposed converter can achieve the lowest voltage stress for the active switches. Also, from, it is seen that the proposed converter can achieve the lowest voltage stress for the diodes. As a result, one can expect that with proper design, the proposed converter can adopt switch components with lower voltage ratings to achieve higher efficiency.

IV. STEADY-STATE ANALYSIS

In order to simplify the circuit performance analysis of the proposed converter in CCM, the same assumptions made in the previous section will be adopted.

A. VOLTAGE GAIN

The volt–second relationship of inductor L_1 (or L_2), one can obtain the following relations:

$$V_{in}D + (V_{in} - V_{CA})(1 - D) = 0$$

$$V_{in}D + (V_{in} - V_{CB})(1 - D) = 0$$

$$V_{C1} = V_{CA} + V_{CB} = \frac{2}{1 - D}V$$

$$V_{C2} = V_{CA} + V_{CB} = \frac{2}{1 - D}V_{in}$$

It follows from (21) and (22) that the output voltage can be obtained as follows:

$$Vo = VC1 + VC2 = Vin(1 - D)$$

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(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2015

Thus, the voltage conversion ratio *M* of the proposed converter can be obtained as follows:

$$M = \frac{V_o}{V_{\text{in}}} = \frac{4}{1-D}$$

B. VOLTAGE STRESSES ON SEMICONDUCTOR COMPONENTS

To simplify the voltage stress analyses of the components of the proposed converter, the voltage ripples on the capacitors are ignored. From Fig. 3(b) and (c), one can see that the voltage stresses on active power switches S_1 and S_2 can be obtained directly as shown in the following equation:

$$V_{S1,\max} = V_{S2,\max} = \frac{1}{1-D} V_{\text{in}}$$

Substituting, the voltage stresses on the active power switches can be expressed as

$$V_{S1,\max} = V_{S2,\max} = \frac{V_O}{4}$$

From, one can see that the voltage stress of active switches of the proposed converter is equal to one fourth of the output voltage. Hence, the proposed converter enables one to adopt lower voltage rating devices to further reduce both switching and conduction losses. As can be observed from the equivalent circuits, the open circuit voltage stress of diodes D_{1a}, *D2a, D1b*, and D_{2b} can be obtained.

$$V_{D1a,\max} = V_{D1b,\max} = V_{D2b,\max} = \frac{V_O}{2}, V_{D2a,\max} = \frac{V_O}{4}.$$

In fact, one can see from (27) that the maximum resulting voltage stress of diodes is equal to $V_O / 2$. Hence, the proposed converter enables one to adopt lower voltage rating diodes to further reduce conduction losses.

C. DRIVING SCHEME

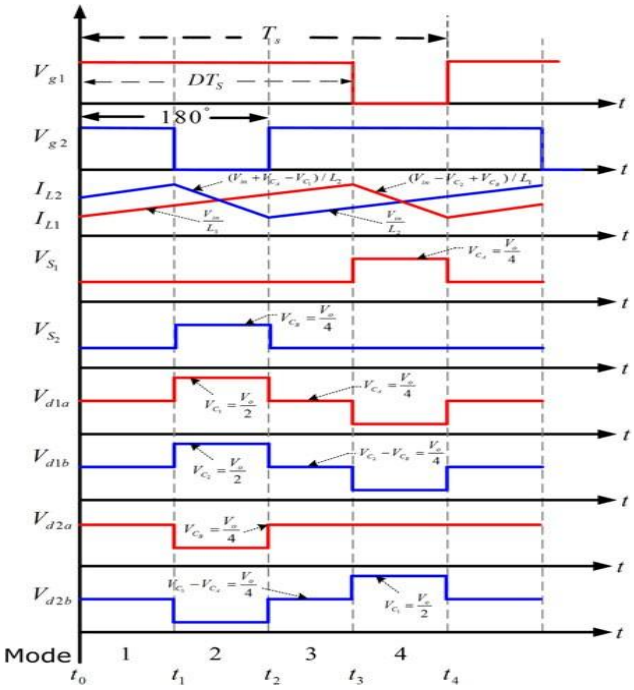

Fig .6. Driving Signal Key Waveforms

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International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2015

V.SIMULSTION RESULT

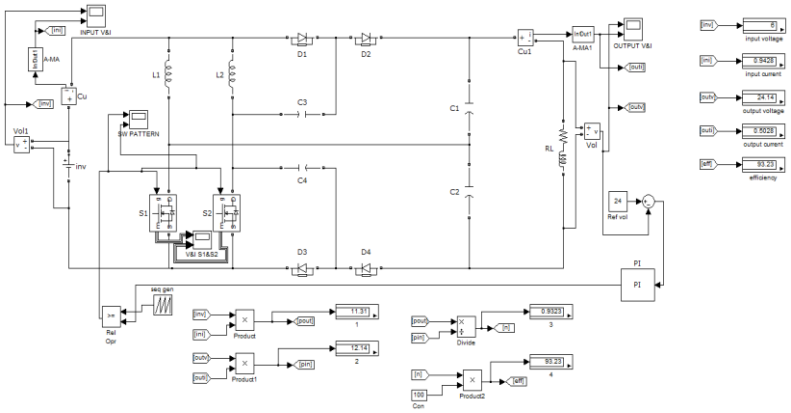

Fig.7. Simulation Circuit diagram.

A. INPUT PULSES OF VOLTAGE QUADRUPLER DC BOOST CONVERTER

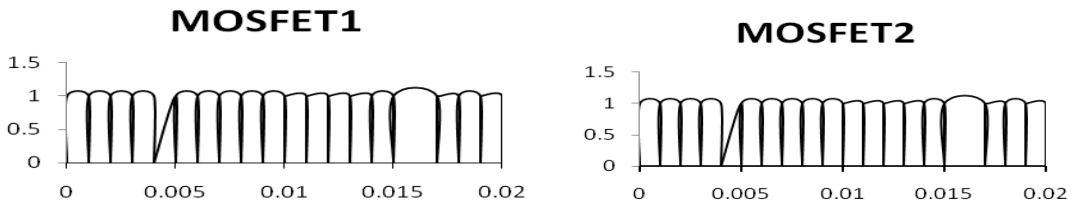

Fig.8. PWM For Mosfet1&2

B. INPUT VOLTAGE OF VOLTAGE QUADRUPLER DC BOOST CONVERTER

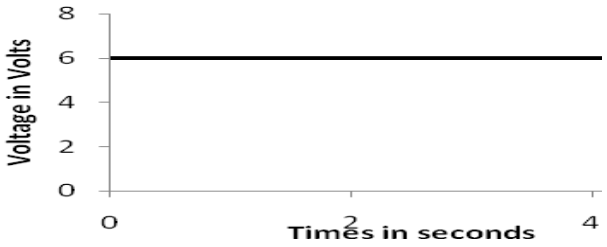

Fig. 9.Input Voltage

C. INPUT CURRENT OF VOLTAGE QUADRUPLER DC BOOST CONVERTER

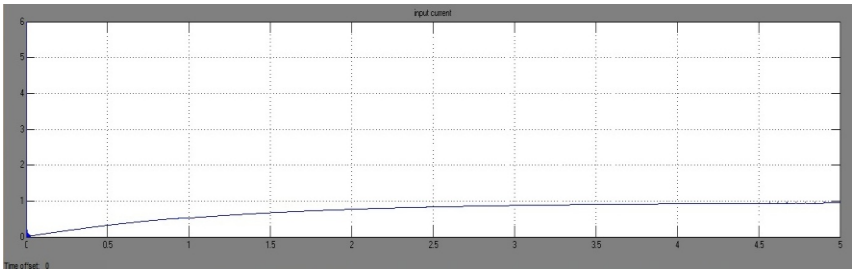

Fig.10. Input Current

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(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2015

D. OUTPUT VOLTAGE OF VOLTAGE QUADRUPLER DC BOOST CONVERTER

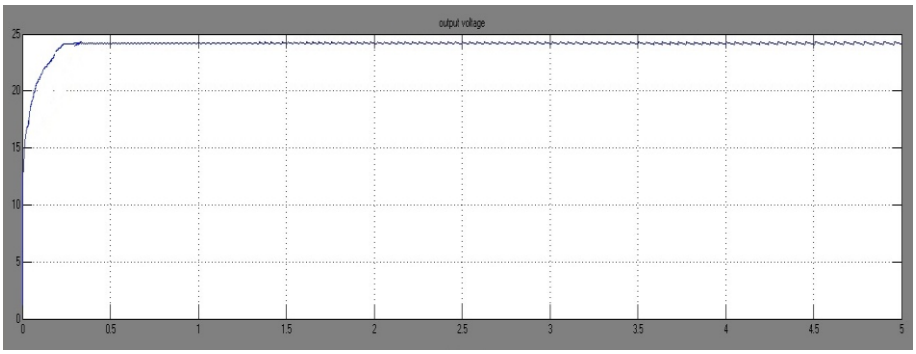

Fig. 11. Output Voltage

E. OUTPUT CURRENT OF VOLTAGE QUADRUPLER DC BOOST CONVERTER

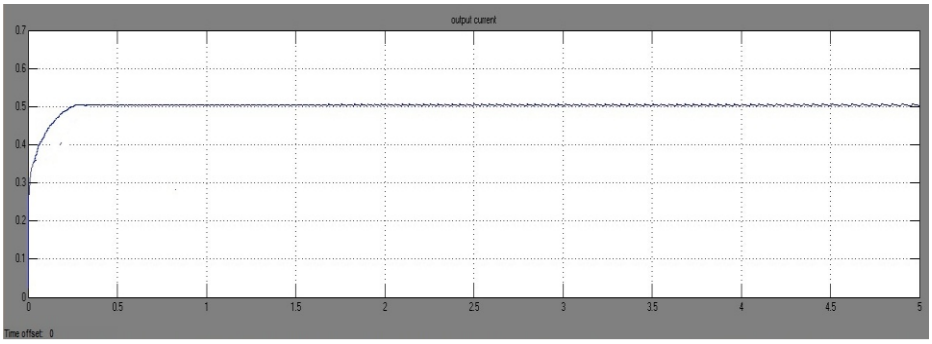

Fig.12. Output Current

VI. EXPERIMENTAL RESULT

A Transformer-less Adaptable Voltage Quadrupler DC Boost converter with PI Controller prototype is built to verify the circuit operation. The circuit parameters are:

- Input voltage: 12 DC
- Output voltage: 196 DC
- Switching frequency, 100 kHz.

Voltage Gain :

Vin= 6V

$$Vo = Vc1 + Vc2 = \frac{4}{1-??} * \text{Vin} = \frac{4}{1-0.75} * 6 = 96$$

$$Vc1 = Vca + Vcb = \frac{2}{1-??} * \text{Vin} = \frac{2}{1-0.75} * 6 = 48$$

$$Vc2 = Vca + Vcb = \frac{2}{1-??} * \text{Vin} = \frac{2}{1-0.75} * 6 = 48$$

$$Vo = 96$$

VII. CONCLUSION

A Transformer-less DC Boost converter with PI Controller to enhance efficiency with high voltage transfer gain and reduced semiconductor voltage stress is proposed. The proposed topology utilizes input-parallel output-series

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configuration and is derived from a two-phase interleaved boost converter for providing a much higher voltage gain without adopting an extreme large duty cycle. The proposed converter cannot only achieve high step-up voltage gain but also reduce the voltage stress of both active switches and diodes. This will allow one to choose lower voltage rating MOSFETs and diodes to reduce both switching and conduction losses. In addition, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the two interleaved phases for voltage boosting mode without adding any well as a comparison with other recent existing high step-up topologies are presented. Finally, a 100-W rating prototype with 12-V input and 96-V output is constructed for verifying the validity of the proposed converter. It is seen that the resulting experimental results indeed agree very close and show great agreement with the simulation results. Therefore, the proposed converter is very suitable for applications requiring high step-up voltage gain.

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