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Designing Hardware Architecture for Polynomial Matrix Multiplications

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ABSTRACT: Hardware architecture for polynomial matrix multiplication of polynomial matrices or polynomial vectors is designed using the Xilinx system generator tool. Hardware implementation of the algorithm is carried out by using highly pipelined, partly systolic field-programmable gate array architecture. The algorithm uses an extension of the fast convolution technique to multiple-input multiple-output systems. System generator enables the use of the math works model-based simulink design environment for FPGA design. The proposed hardware architecture requires less execution time and less number of FPGA resources. To make effective use of SBR2P architecture in real-time applications, hardware implementation of the polynomial matrix multiplication is required. For this we can use efficient, Highly pipelined, and partly systolic FPGA architecture for matrix-vector and matrix-matrix PMM operations. The architecture for computing the PMM will implemented on virtex-5. Design is developed using the Xilinx system generator tool which was synthesized, mapped, placed and routed by Xilinx ISE 14.5 tool.

KEYWORDS: Field programmable gate array (FPGA), Xilinx system generator, polynomial matrix multiplication.

I. INTRODUCTION

Polynomial matrix is a matrix whose elements are multivariate or univariate polynomials. In the area of control, polynomial matrices have been used. They play an important role in the realization of multi-variable transfers functions associated with multiple-input multiple-output systems. Applications of polynomial matrix techniques include broadband sensor array signal processing, biomedical engineering, multiple-input multiple-output communications and coding. Polynomial matrix eigen value decomposition gives output consisting of a diagonal polynomial matrix that is pre and post multiplied by paraunitary polynomial matrices. At every frequency polynomial matrix saves the total power signal power. Here PMM is used as a tool for polynomial eigenvalue decomposition.

II. LITERATURE SURVEY

An eigenvalue decomposition algorithm amounts to diagonalizing the polynomial matrix by means of a paraunitary transformation. The algorithm makes use of elementary paraunitary transformations and constitutes a generalization of the classical Jacobi algorithm for conventional Hermitian matrix diagonalization. Second order sequential best rotation algorithm gives an extension of the EVD to Para-Hermitian polynomial matrices. It was developed for the purpose of generating a finite impulse response PU matrix to diagonalize the para-Hermitian polynomial matrix of signals received by a broadband sensor array. Signals that give rise to a diagonalized para-Hermitian matrix have the strong decorrelation property. In the case of broadband sensor array, the sensor outputs will generally be correlated with one another. However, they can no longer be decorrelated using the eigenvalue decomposition, which only measure and remove instantaneous spatial correlation, i.e. correlation between pairs of signals sampled at the same instant in time. For convolutive mixing, it is necessary to decorrelate signals not just at the same time instant for all signals, but over a suitably chosen range of relative time delays. This is nothing but strong decorrelation or total decorrelation, and a matrix of suitably chosen filters is required to achieve it. Strong decorrelation for broadband sensor array is implemented using a paraunitary polynomial matrix. A paraunitary polynomial matrix represents a multichannel all-pass filter and accordingly it preserves the total signal power at every frequency. In order to achieve strong decorrelation, para-Hermitian polynomial matrix is achieved by means of second order sequential best rotation algorithm.

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Another approach to decorrelate broadband signals is to reduce the problem to narrowband form, using a DFT to split the data into narrower frequency bands. Conventional singular value decomposition is used to decorrelate the sensor signals within each band. Computing an independent single value decomposition for each frequency band ignores the relatively small but important correlations that may exist between different bands. This independent frequency band approach limits the degree of strong decorrelation. This also lead to a lack of phase coherence across the bands. The singular value decomposition is a very important tool for narrowband adaptive sensor array processing. It finds application in areas as diverse as high resolution direction finding. The SVD decorrelates the signals received from an array of sensors by applying a unitary matrix of complex scalars which serves to modify the signals in phase and amplitude.

Polynomial matrices are useful in finding out foetal heart condition. The foetal ECG is an electric signal that can be measured in a non-invasive manner by applying electrodes to the abdomen of an expected mother. This practice leads to a contamination of the recorded signals with interference mainly from the maternal heartbeat. Much research effort has been devoted to the detection and extraction of foetal ECG using techniques such as neural networks, fuzzy logic, IIR adaptive filtering combined with genetic algorithms. For that they use principal component analysis which generates uncorrelated sequences. Then higher order statistics are used in order to complete the separation process. If the total power of the FECG signal across all the channels is significantly different from the interferers, then the PCA carries out most of the separation. This is totally based on the singular-value decomposition or eigenvalue decomposition. Drawback of the basic SVD-based technique is that signal separation performance is dependent on the position of the electrodes. Previously eigenvalue decomposition algorithm is realized by using field programmable gate array hardware. For that parallelized version of the second-order sequential best rotation is used. Hardware implementation of the algorithm is achieved via a highly pipelined, nonsystolic FPGA architecture, the architecture has been designed using Xilinx system generator tool.

III. FIELD PROGRAMMABLE GATE ARRAY

A field programmable gate array is an field programmable device featuring a general structure that allows very high logic capacity, FPGA offer more narrow logic resources. FPGA also offer a higher ratio of flip-flops to logic resources. FPGA's comprise an array of uncommitted circuit elements, called logic blocks, and interconnect resources, but FPGA configuration is performed through programming by the end user. The design process of FPGA is similar to that for CPLDs, but additional tools are needed to support the increased complexity of the chips. The major difference in the "device fitter" step that comes after logic optimization and before simulation, where FPGA require three steps: a technology mapper to map from basic logic gates into the FPGA's logic blocks, placement to choose which specific blocks to use in the FPGA, and router to allocate the wire segments in the FPGA to interconnect the logic blocks. With this added complexity, the CAD tools might require a fairly long period of time to complete their tasks. FPGA is nothing but logic blocks placed in an interconnect framework, interconnect framework comprises of wire segments and switches; provide a means to interconnect logic blocks. Any data can be stored in FPGA using block RAM. Block RAM has different types as single port RAM, single port ROM, True dual port RAM, True dual port ROM and simple dual port RAM. FPGA is systolic array, a systolic array is an arrangement of processors in an array where data flows synchronously across the array between neighbors, usually with different data flowing in different directions. Each processor at each step takes in data from one or more neighbors, processes it and, in the next step, outputs results in the opposite direction. Each systolic unit is an independent processor, every processor has some registers and an ALU. The cells share information with their neighbors, after performing the needed operations on the data.

IV. SBR2 ALGORITHM

To make effective use of SBR2P architecture in real-time applications, hardware implementation of the polynomial matrix multiplication is required. For this we can use efficient, Highly pipelined, and partly systolic FPGA architecture for matrix-vector and matrix-matrix PMM operations. The proposed architecture gives low execution times while utilizing limited FPGA resources. It gives good approximation to the polynomial matrix computation provided by its counterpart running in MATLAB for both real and complex valued data. The architecture has been developed using the Xilinx system generator for DSP tool. The SBR2 algorithm was originally developed for the purpose of generating a lossless filter bank to decorrelate the signals received by a broadband sensor array.

SBR2 adopt different formula for generating the paraunitary matrices

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$$\mathbf{H}(z) = \mathbf{Q}_L \Lambda^{dL} \ldots\ldots \mathbf{Q}_1 \Lambda^{d1}$$

Where the integer parameters di can be negative or positive It can be seen that any polynomial matrix generated by is paraunitary since each stage is paraunitary. Each step of the algorithm applies a single elementary paraunitary matrix, chosen to maximize an instantaneous measure of decorrelation evaluated at that stage. This might not appear to be a sensible strategy since the successive elementary paraunitary matrices do not commute and applying a rotation doesn't just affect the current state but also the potential future gains of the algorithm. Unlike the narrowband case, applying a poorly chosen rotation is likely to make the problem more difficult by increasing the order of the mixing polynomial for no good reason. However, the freedom to choose an optimum delay for each stage makes the process much more meaningful.

The SBR2 algorithm for two signals may be summarized as follows:

1. Apply a relative delay between the two signals so that the instantaneous correlation between them is maximized.
2. Rotate the signals through an angle θ which drives the instantaneous correlation to zero.
3. Repeat steps 1 and 2 until the value of N_1 achieves its maximum value to within a specified tolerance.

V. XILINX SYSTEM GENERATOR TOOL

System Generator is a DSP design tool from Xilinx that enables the use of the MathWorks model-based Simulink design environment for FPGA design. Previous experience with Xilinx FPGAs or RTL design methodologies are not required when using System generator tool. Designs are captured in the DSP friendly Simulink modeling environment using a Xilinx specific blockset. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file. System Generator includes a FIR Compiler block that targets the dedicated DSP48 hardware resources in the Virtex-4 and Virtex-5 devices to create highly optimized implementations that can run in excess of 500 Mhz. System Generator is an MCode block that allows the use of non-algorithmic MATLAB for the modeling and implementation of simple control operations. System Generator provides a Resource Estimator block that quickly estimates the area of a design prior to place and route. This can be a valuable aid in the hardware / software partitioning process by helping system designers take full advantage of the FPGA resources which include up to 640 multiply/accumulate (or DSP) blocks in the Virtex-5 devices. System Generator provides a system integration platform for the design of DSP FPGAs that allows the RTL, Simulink, MATLAB and C/C++ components of a DSP system to come together in a single simulation and implementation environment. System Generator supports a black box block that allows RTL to be imported into Simulink and co-simulated with either ModelSim or Xilinx-ISE Simulator. System Generator also supports the inclusion of a MicroBlaze embedded processor running C/C++ programs. System Generator does not support UNC (Universal Naming Convention) paths. For example System Generator cannot operate on a design that is located on a shared network drive without mapping to the drive first. System generator is a system level modeling tool that facilitates
FPGA hardware design. It extends simulink in many ways to provide a modeling environment that is well suited to hardware design. The tool provides high-level abstractions that are automatically compiled into an FPGA at the push of a button. The tool also provides access to underlying FPGA resources through low level abstraction, allowing the construction of highly efficient FPGA designs. The simulink environment uses a “double” to represent numbers in simulation. A double is a 64-bit twos complement floating point number. The Xilinx blockset uses n-bit fixed point numbers. Thus, a conversion is required when Xilinx blocks communicate with simulink blocks.

VI. CONCLUSION

FFT is used to design a novel FPGA architecture for the implementation of an algorithm for computing polynomial matrix multiplication. The proposed architecture uses limited FPGA resources and has a little dependency on the order of the input polynomial matrices.

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