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High Speed 16 Bit Digital Multiplier Architecture Using Urdhwa Tiryakbhyam and Compressors

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ABSTRACT: With the growing technology in field of Communication and VLSI a very high Speed processing power and low area is area is required. Multiplier unit is the central part of digital signal processor as well as general purpose processors that substantially decide the performance of the same. Due to this a high speed multiplier architecture become the need of the day. This paper introduce the 16 bit high speed digital multiplier architecture based on ancient Vedic mathematics. For further increasing the speed of multiplication, addition of partial products generated by multiplication has been implemented by 4:2 and 7:2 compressor. Upon comparison the compressor based Vedic multiplier is 1.5 times faster than normal Vedic multiplier and almost 2 times faster than conventional multiplier. The architecture has been implemented using Verilog language and the tool used for simulation is Xilinx ISE 14.2.

KEYWORDS: FPGA, Multiplier, VLSI, Vedic Mathematics, 4:2 compressor, 7:2 compressor

I.INTRODUCTION

Various arithmetic operations such as multiplication addition, subtraction are important part of digital circuit to speed up the computation speed of processor. However the speed of processor greatly depends on multiplier unit of the processor. This in turn increase the demand of high speed multiplier architecture in ALU and in various digital signal processors. Several new multiplier architecture have been introduced over the past few decades. Booth's multiplier [7] and modified booth's [12] multiplier are very popular in modern VLSI design but they have their own set of disadvantages. In these multiplier before arriving the final answer several intermediate steps are required that slows the speed of processor. These intermediate steps includes several shifting operations, comparison and subtraction which reduce the speed of processor exponentially as the number of bits present in multiplier and multiplicand increases. Since Speed is major concern in developing processors now a days, so new architecture have to be introduced which are faster than above mentioned multiplier.

To address the above mentioned disadvantage of conventional multiplier booth's multiplier and modified booth's multiplier a new architecture based on Vedic mathematics is explored. Vedic mathematics is ancient system of mathematics that was reintroduced by Bharati Krishna Tirthaji Maharaj [3]. "Vedic mathematics" was the name given byhim. Bharati Krishna who was the scholar of Sanskrit, mathematics, and philosophy, introduced simple methods to solve complex mathematical problem that are very complex in conventional mathematics. He bifurcated Vedic mathematics into 16 simple sutras and 13 sub sutras. These sutras have been proved very efficient in solving complex problems in a simple way. All Sutras deals with Trigonometry, Algebra, Geometry and has various applications in signal processing, control engineering and in VLSI.

The Vedic mathematics multiplier can generate partial products before the actual product has started because of its Urdhwa Tiryakbhyam method [7]. Vedic mathematics multiplier is the fastest available multiplier. However most of the delay in Vedic mathematics multiplier is due to addition of partial products using half adder, full adder and carry propagation delay. In this paper compressor based method for 8 bit multiplication has been proposed [1]. Compressors are digital circuit that are capable in adding more than three bits simultaneously removing the disadvantage of full adder

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that is capable in adding only three bits at a time [2]. For further increasing the speed of 16 bit multiplier reconfigurable multiplier method [13] has been used in addition to 8 bit compressor based multiplier.

II.VEDIC MATHEMATICS

Vedic mathematics is part of four Vedas. It is part of Sthapatya Veda which is an up Veda of Atharwa Veda. Vedic Mathematics is divided in 16 sutras and 13 up sutras by bhakti Krishna Tirthji Maharaj [3]. These covers the explanation of various parts of mathematics including Geometry, Trigonometry, and Algebra. Among these 16 sutras Urdhwa Tiryakbhyam sutra is very efficient and highly preferred algorithm for multiplication. Urdhwa Tiryakbhyam sutra appears like magic for multiplication but this sutra is purely logical and very simplified method for multiplication which eliminates complex steps of multiplication.

"Urdhwa Tiryakbhyam" sutra is integration of two Sanskrit words Urdhwa and Tiryakbhyam which means "vertically" and "crosswise" respectively [3]. The main advantage of utilizing this algorithm in comparison with other existing multiplication methods, is fact that it requires only AND gate, half adder and full adder to complete multiplication. Also the partial product are generated in parallel that save a lot of time and makes multiplication processes very fast. All sixteen sutras are given below-

1. Ekadhikena Purvena
2. Nikhilam navatascaramam Dasatah
3. Urdhva - tiryagbhyam
4. Paravartya Yojayet
5. Sunyam Samya Samuccaye
6. Anurupye - Sunyamanyat
7. Sankalana - Vyavakalanabhyam
8. Puranapuranabhyam
9. Calana - Kalanabhyam
10. Ekanyunena Purvena
11. Anurupyena
12. Adyamadyenantya - mantyena
13. Yavadunam Tavadunikrtya Varganca Yojayet
14. Antyayor Dasakepi
15. Antyayoreva
16. Gunita Samuccayah.

III.VEDIC MATHEMATICS MULTIPLIER

This multiplier is based on Urdhwa Tiryakbhyam sutra. Using this method to multiply two binary number "vertically crosswise" multiplication is calculated for individual bits [14].

Let us consider there are two 8 bit binary number X_7-X_0 and Y_7-Y_0 where X_7 Y_7 are MSB and X_0, Y_0 are LSB. The product of these two 8 bit binary number is 16 bit number that is represented by P_{15}-P_0.

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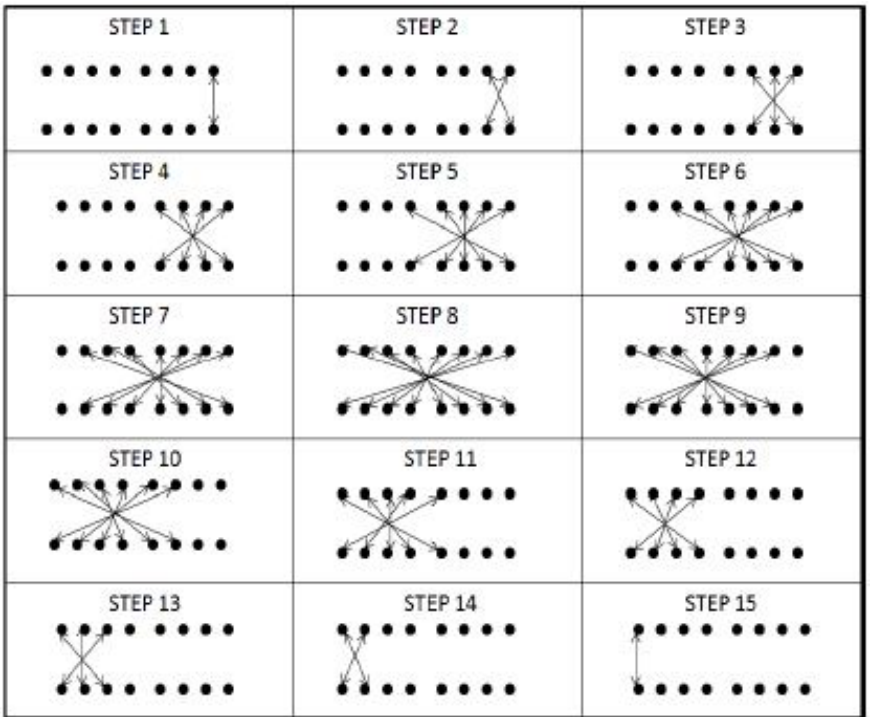

Fig. 1. Multiplication using Urdhwa Tiryakbhyam sutra [1]

All partial products can be calculated using above mentioned method. The final product P15 – P0 can be calculated using full adder, half adder. The following equation clearly explain the procedure for calculation of final product.

$$P_0 = X_0Y_0 \quad (1)$$

$$P_1 = X_0Y_1+X_1Y_0+C_1 \quad (2)$$

$$P_2 = X_2Y_0+X_0Y_2+ X_1Y_1+C_2 \quad (3)$$

$$P_3 = X_3Y_0+ X_0Y_3+ X_2Y_1+ X_1Y_2+C_3+ C_4 \quad (4)$$

$$P_4 = X_4Y_0+ X_0Y_4+ X_3Y_1+ X_1Y_3+ X_2Y_2+C_5+C_6 \quad (5)$$

$$P_5 = X_5Y_0+ X_0Y_5+ X_4Y_1+ X_1Y_4+X_3Y_2+ X_2Y_3+C_7+ C_8+ C_9 \quad (6)$$

$$P_6 = X_6Y_0+ X_0Y_6+ X_5Y_1+ X_1Y_5+ X_4Y_2+ X_2Y_4+ X_3Y_3+C_{10}+C_{11}+ C_{12} \quad (7)$$

$$P_7 = X_7Y_0+ X_0Y_7+ X_6Y_1+ X_1Y_6+ X_5Y_2+ X_2Y_5+ X_3Y_4+X_4Y_3+C_{13}+C_{14}+C_{15}+C_{16} \quad (8)$$

$$P_8 = X_7Y_1+ X_1Y_7+ X_6Y_2+ X_2Y_6+ X_5Y_3+ X_3Y_5+ X_4Y_4+C_{17}+C_{18}+C_{19}+C_{20} \quad (9)$$

$$P_9 = X_7Y_2+ X_2Y_7+ X_6Y_3+ X_3Y_6+ X_4Y_5+ X_5Y_4+C_{21}+C_{22}+C_{23}+C_{24} \quad (10)$$

$$P_{10} = X_7Y_3+ X_3Y_7+ X_6Y_4+ X_4Y_6+ X_5Y_5+ C_{25}+ C_{26}+ C_{27}+ C_{28} \quad (11)$$

$$P_{11} = X_7Y_4+ X_4Y_7+ X_6Y_5+ X_5Y_6+ C_{29}+ C_{30}+ C_{31} \quad (12)$$

$$P_{12} = X_7Y_5+ X_5Y_7+ X_6Y_6+ C_{32}+ C_{33}+ C_{34} \quad (13)$$

$$P_{13} = X_7Y_6+ X_6Y_7+ C_{35}+ C_{36} \quad (14)$$

$$P_{14} = X_7Y_7+ C_{37}+ C_{38} \quad (15)$$

$$P_{15} = X_7Y_7$$

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The carry bits generated during the calculation of final product are represented from C-1 to C¬38. The dots in Fig 1 represent LSB to MSB from right to left respectively. Arrow gives indication for the bits to be multiplied. From equation (1) to (15) it can be seen that number of bits are increasing this require additional number of stages of half adder and full adder that proportionally increases delay for final product.

The 16 bit multiplier can be implemented using 2n-bit reconfigurable method that has been given in equation (17). In this method let us consider that X and Y are two 16 bit multiplier and multiplicand respectively and we assume X and Y as 2n bit wide binary numbers where value of n is 8. X_H,Y_H represents MSB 8 bits of X and Y, X_L and Y_L represents LSB 8 bits of X and Y respectively.

$$P = (X_H * Y_H)\, 2^{2n} + (X_H * Y_L + X_L * Y_H) 2^n + X_L * Y_L \text{ [13]} \qquad (17)$$

To overcome disadvantage of Vedic multiplier 4:2 and 7:2 compressor have been proposed [1]. These compressor are able to add 4 bits and 7 bits simultaneously which reduces the number of stage for calculation of final product and multiplier gives better result compared to Vedic multiplier. For further improvement in 16 bit multiplier in addition to compressor reconfigurable multiplier architecture [13] has been used.

IV.COMPRESSOR

Compressor is the logical circuit that is capable in adding more than 3 binary bits. Due to its property to reduce larger number of bits into smaller one it is called compressor. Compressor can replace large number of full adder and half adder.

A. 4:2 COMPRESSOR

4:2 compressor consist of 4 input bits, 3 output bits and it can be implemented with two stages of full adder connected in series as shown in fig 2. 4:2 compressor using full adder has been shown in fig. 2, it has 4 input bits X_1-X_4 and one carry C_{in}. One sum bit S and two carry C and C_{out} are the outputs of 4:2 compressor. C_{out} will be propagated to next 4:2 compressor as carry input bits.

Nevertheless the same 4:2 compressor can be implemented using more efficient method used in [2]. The architecture of this compressor is shown in fig. 3. Fig. 3 clearly shows that all

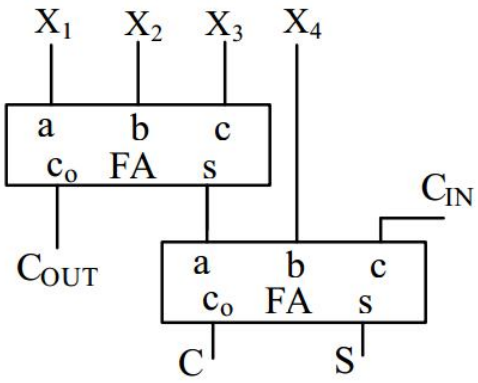

Fig. 2. 4:2 compressor using two full adder [2]

It is made up of multiplexer and XOR gate and it can be clearly seen that the critical path of this compressor is less in comparison with full adder based compressor. Let us assume that delay of gate is tp than full adder based compressor would require 4tp time and due to only 3 gates in series in presented 4:2 compressor the delay will be tp. That clearly show the performance improvement over previous 4:2 compressor

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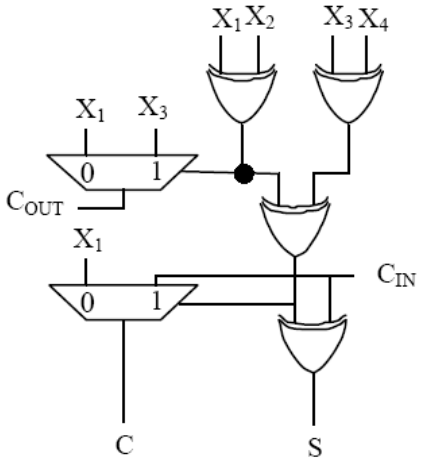

Fig. 3 Mux and XOR based 4:2 compressor architecture [2]

In fig 3 it has been shown that 4:2 compressor can be implemented using XOR gate and Multiplexer, all 5 bits (one carry and 4 input bits) given to mux and XOR and 3 output bits has been generated. This is very efficient method to implement 4:2 compressor as compared to full adder based compressor method.

B. 7:2 COMPRESSOR ARCHITECTURE

The 7:2 compressor consist of 7 inputs and 2 carries from previous stage. It has 3 outputs consisting one sum and two carries.

7:2 compressor can be implemented using two 4:2 compressor, one half adder and two full adder. This compressor has great improvement over compressor based on only full adder and half adder for adding 9 bits at a time.

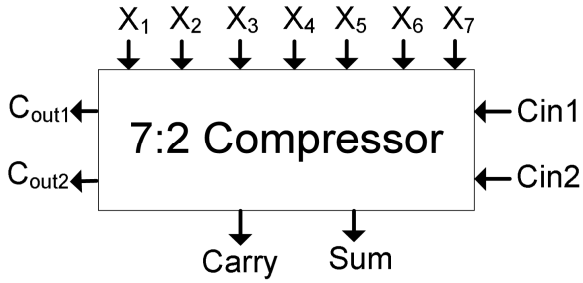

Fig. 4. 7:2 compressor

The general architecture of 7:2 compressor has shown in fig 4 and fig 5 shows the architecture of 7:2 compressor using 4:2 compressor, half adder and full adder.

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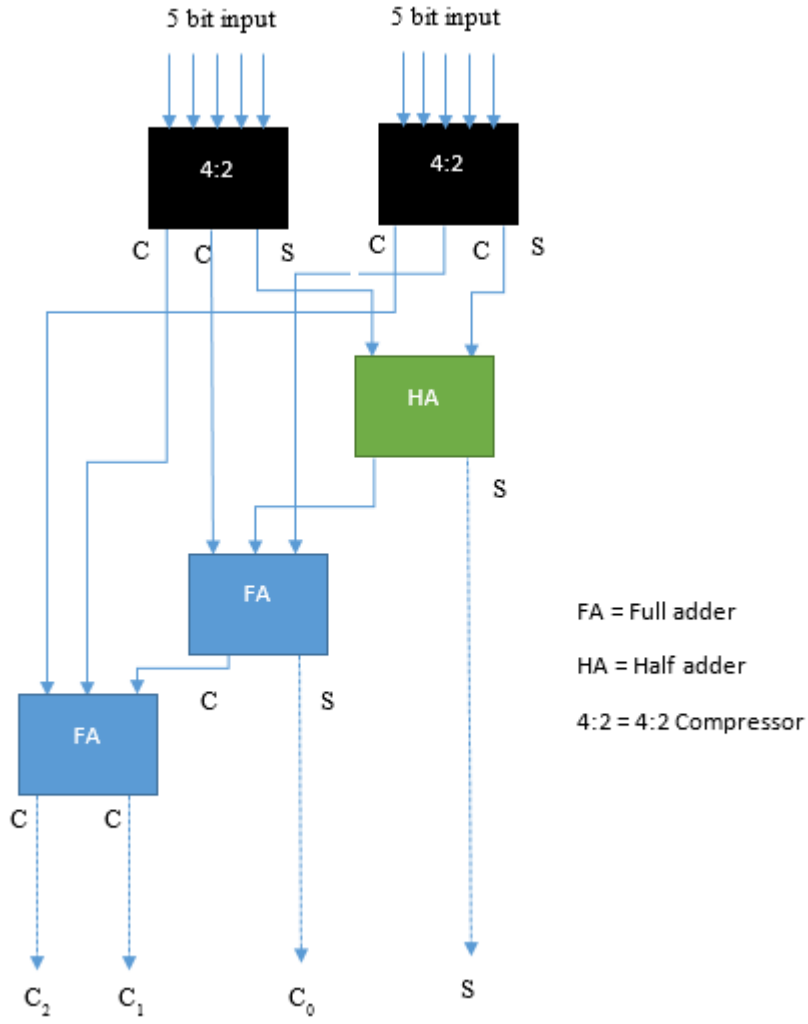

Fig. 5. 7:2 compressor using 4:2 compressor, half adder and full adder [1]

Fig. 5 explains the implementation method of 7:2 compressor. It can be clearly seen in fig. 5 two full adder, one half adder and previously explained 4:2 compressor has been used. The implementation of 7:2 compressor has been tested on Xilinx ISE 14.2 and it has been seen that this compressor is 1.05 times faster than the conventional approach.

V.16 BIT MULTIPLIER BASED ON URDHWA TRIYAKBHYAM, COMPRESSOR ADDER AND RECONFIGURABLE MULTIPLIER

This paper proposed the architecture for 16 bit multiplier. First 8 bit multiplier has been implemented using Urdhwa Tiryakbhyam sutra as it is known that this is the fast available multiplier but requires a lot of full adder and half adder for addition of partial products that substantially increase the delay for multiplication. It can be known from previous section that compressor adder are much efficient over conventional adder. In proposed design of multiplier compressor (4:2 and 7:2) for addition of more than 3 bits has been used that significantly increased the speed of Vedic multiplier.

For further increase the speed of 16 bit multiplication 8 bit Vedic multiplier and reconfigurable multiplier has been used that is very well organized approach for making low power and high speed multiplication. Addition of this method to Vedic multiplier has shown significant improvement.

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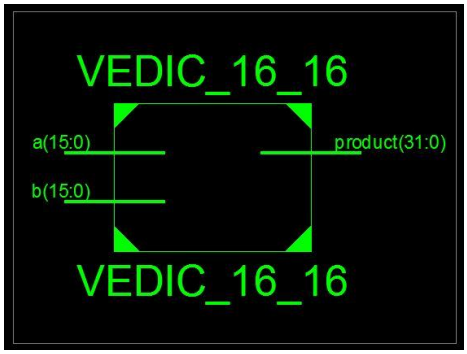

Fig. 6. 16 bit Vedic multiplier block

Fig. 6 shows the RTL architecture of 16 bit proposed high speed Vedic multiplier. It has two 16 bit input multiplier and multiplicand, 32 bit output is produced by multiplication.

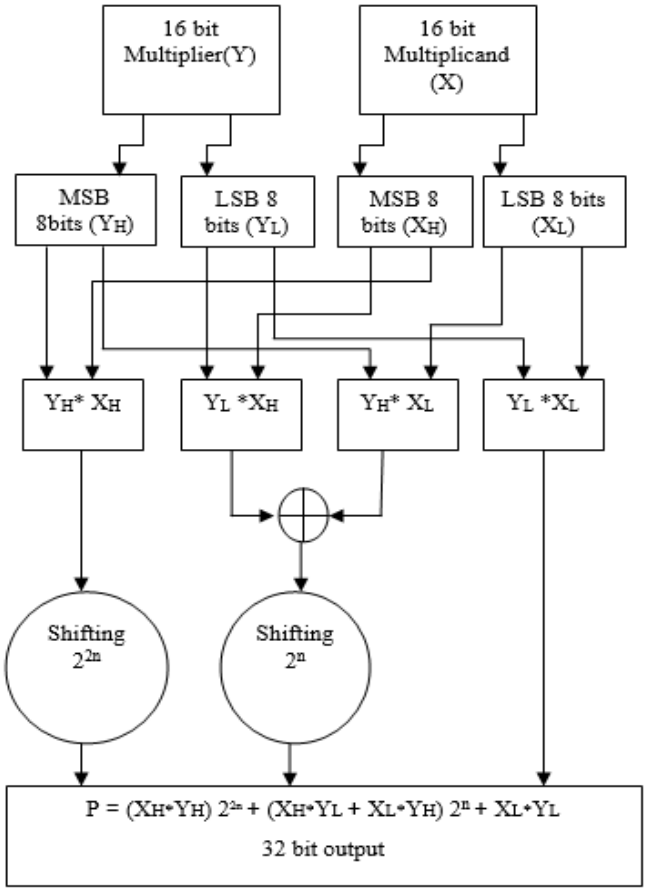

Fig. 7. 16 bit Vedic multiplier architecture

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Fig 7 shows the architecture of 16 bit multiplier. 16 bit multiplier and multiplicand have been splitted in to LSB and MSB 8 bits respectively these 8 bits have been represented by Y_H, X_H, Y_L, X_L where subscript L represents lower and H represents higher 8 bits. The 8 bit multiplication has been done by compressor based 8 bit vedic multiplier. Final product has been calculated by following formula.

$$P = (X_H * Y_H)2^{2n} + (X_H * Y_L + X_L * Y_H)2^n + X_L * Y_L$$

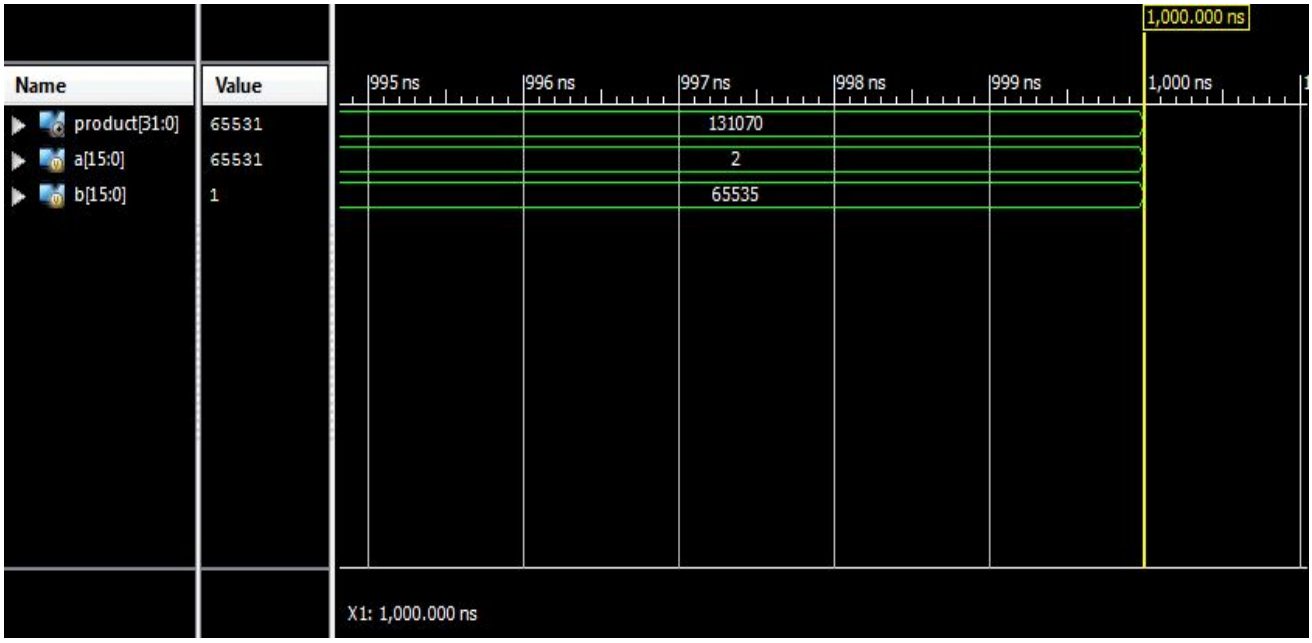

Fig. 8. Simulation result of 16 bit multiplier

Simulation results have been shown in figure 8. Multiplier presented in this paper is almost 1.5 times faster than conventional Vedic multiplier and 2 times faster than booth's multiplier.

VI.RESULTS

Well liked multiplier such as booth's multiplier and Vedic multiplier has been synthesized and simulated on Xilinx ISE 14.2. Upon comparison with proposed 16 bit multiplier speed grade table has been created that clearly shows the significance of proposed multiplier.

TABLE 1 COMPARISON OF VARIOUS MULTIPLIER ARCHITECTURE

ARCHITECTURE	Number of Bits	DELAY (ns)	FREQUENCY (MHz)
BOOTH MULTIPLIER	16	65.72	15.21
VEDIC MULTIPLIER	16	48.506	20.61
PROPOSED MULTIPLIER	16	30.132	33.18

The speed and frequency of various multiplier architecture such as Booth's multiplier, Vedic multiplier and proposed multiplier for 16 bit multiplication is given in Table I. Table 1 clearly represents that proposed multiplier is almost 2 times faster than booth's multiplier and 1.5 times faster than the existing Vedic multiplier.

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VII.CONCLUSION

In this paper a high speed multiplier architecture for 16 bit multiplication has been proposed. This architecture is combination of various researched architecture available for multiplication and addition such as Vedic multiplier, reconfigurable multiplier and compressor. Upon comparison with other existing multiplier it can be concluded that proposed multiplier is best in speed. For future work multiplier can be implemented and tested in ALU to increase the performance of processor.

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