



Efficient Bridgeless SEPIC Converter for BLDC Motor with Improved Power Factor

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ABSTRACT: An universal line approaches a modified version of the bridgeless single-ended primary inductance converter (BL-SEPIC) as preferred to achieve unity power factor by varying the speed of BLDC motor is presented in this paper using ANFIS controller. Two semiconductor switches are conducted during each switching cycles resulting in less conduction losses, switching losses and THD. Voltage Source Inverter (VSI) and variable DC link capacitor controls the wide range of speed controls with a single voltage sensor and applicable for low-power application. The performance of the system was analyzed through a MATLAB/Simulink model during discontinuous inductor current mode (DICM).

KEYWORDS: ANFIS controller, BLDC Motor, Bridgeless single-ended Primary inductance converter (BL-SEPIC), power factor, voltage source inverter.

I. INTRODUCTION

Brushless DC motor drives have improved in the last decade due to the quality of power is increased that have also resulted in comprehensive good performance compared with other conventional drives. The advantages of motor with the absence of brushes are compact size, high efficiency, high power density, high ruggedness, low electro-magnetic interference (EMI) problems. From the ranging of low- and medium-power applications BLDC motor are suited like household appliance; medical equipment; air-conditioning; and transportation. The BLDC motors are similar as synchronous motor having permanent magnet on the rotor and three phase winding on the stator. By the absence of brushes and using the electronic commutation performance which eliminates the problems such as sparking, noise and EMI. A conventional BLDC motor drive proposed using front-end diode bridge rectifier (DBR) with the high value of DC link capacitor causes current has highly distorted leads disturbance in the source named harmonics are increased and very low power factor of the order of 0.72.

The use of low-switch voltage topologies achieve higher static gain and torque ripple reduction can improve the efficiency operates at low input voltage done by different converters. Boost converter uses voltage multiplier technique to improve the static gain with reduced switching losses. But the output voltage from the boost converter is doublers which is not suitable for universal input voltage. Buck-Boost converter can improve the static gain with higher switch voltage. A classical single-ended primary inductance converter (SEPIC) approaches the integration of a voltage multiplier cell in order to analyzed high step-up and low step-up static gain for the relevant input voltage operation, but it cannot reduce the torque ripple causes disturbance on the source side voltage. Using of ANFIS controller will reduce the torque ripple at the load and achieve the unity power factor at the ac mains.

II. LITERATURE REVIEW

In Bridgeless converters, the absence of an input diode bridge and the presence of only two semiconductor switches in the current flowing path during each switching cycle result in less conduction losses and improved thermal management compared to the conventional Sepic and Cuk PFC converters. Sepic and Cuk converters offer several advantages in PFC applications, such as easy implementation of transformer isolation, inherent inrush current limitation during start-up and overload conditions, lower input current ripple, and less electromagnetic interference (EMI). [1] The NFC serves as the speed controller of the drive Mamdani type FLC is designed and incorporated to optimize the developed torque ripple by online adaptation of the hysteresis band limits of the PWM current controller. A



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performance comparison of the proposed NFCFLC based IPMSM drive with conventional proportional integral (PI) controller based IPMSM drive having fixed hysteresis band limits is provided. Using this paper as a reference for torque ripple reduction and advantages of both ANFIS and FLC controlling technique [2]

It consists of C-type passive filter in parallel with a shunt active filter that is controlled by an adaptive neuro-fuzzy inference system (ANFIS) controller. The C-type passive filters have several features of low current rating, easier protection, and no resonance possibility with source and load. This work has taken the approach of the first configuration, with control scheme of ANFIS to enhance its tracking and estimation of the harmonics, boosting the overall system performance [3] An adaptive network-based fuzzy inference system (ANFIS) for speed and position estimation of PMSG, where an ANFIS-based model reference adaptive system is continuously tuned with actual PMSG to neutralize the effect of parameter variations such as stator resistance, inductance, and torque constant was presented. This ANFIS-tuned estimator is able to estimate the rotor position and speed accurately over a wide speed range with a great immunity against parameter variation. It has also been demonstrated that the grid-side inverter can perform all the duties of shunt APF while maintaining the smooth bidirectional power flow simultaneously. [4]

A new bridgeless single-phase ac–dc converter with a natural power factor correction (PFC) was proposed. Compared with existing single-phase bridgeless topologies, the bridgeless PFC topology has the merits of less component counts. Other advantages include: simple structure, soft switching, common ground, electrical isolation, and simple control circuitry. The absence of an input diode bridge and the presence of only one diode in the current path during each stage of the switching cycle result in higher power density and less conduction losses; hence, improved thermal management compared to existing PFC rectifiers is obtained. [5] Solid-state switch mode AC-DC converters having high-frequency transformer isolation are developed in buck, boost, and buck-boost configurations with improved power quality in terms of reduced total harmonic distortion (THD) of input current; power-factor correction (PFC) at AC mains and precisely regulated and isolated DC output voltage feeding to loads was presented. These AC-DC converters provide a high level of power quality at AC mains and well regulated, ripple free isolated DC outputs. Moreover, these converters have been found to operate very satisfactorily with very wide AC mains voltage and frequency variations. Using this paper as a reference for improving power quality in terms of total harmonic distortion [6]

A bridgeless buck power factor correction rectifier that substantially improves efficiency at low line of the universal line range is introduced. By eliminating input bridge diodes, the bridgeless rectifier's efficiency is further improved. A bridgeless buck PFC rectifier that further improves the low-line (115 V) efficiency of the buck front-end by reducing the conduction loss through minimization of the number of simultaneously conducting semiconductor components is introduced. The bridgeless buck rectifier also works as a voltage doubler; it can be designed to meet harmonic limit specifications with an output voltage shows better hold-up time performance. Although the output voltage is doubled, the switching losses of the primary switches of the downstream dc/dc output stage are still significantly lower. [7]

A Cuk dc–dc converter as a single-stage power-factor-correction converter for a permanent magnet (PM) brushless dc motor (PMBLDCM) fed through a diode bridge rectifier from a single-phase ac mains was dealt in this paper. The voltage speed control scheme which is based on the control of the dc link voltage reference as an equivalent to the reference speed. The PFC control scheme uses a current multiplier approach with a current control loop inside the speed control loop for continuous-conduction-mode operation of the converter. The control of current to PMBLDCM through VSI during the step change of the reference voltage due to the change in the reference speed, a rate limiter is introduced, which limits the stator current of the PMBLDCM within the specified value which is considered as double the rated current. [8]

III. PROPOSED SYSTEM

The proposed system consists of bridgeless converter replacing conventional SEPIC converter. In the Brushless Direct Current Motor (BLDC) single voltage sensor is used. This feature of BLDC motor reduces the cost and also improves the performance. The SEPIC rectifier is a high step-up AC-DC converter which is placed between the AC source and the motor. The change over of the motor speed will not disturb the AC source and maintain power quality.

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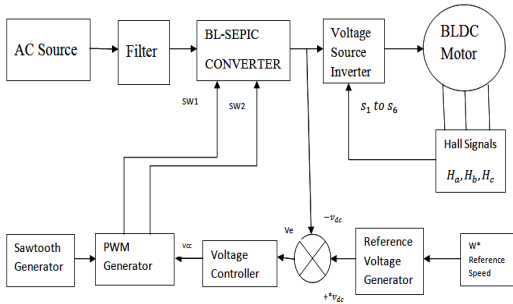


FIGURE 1(a)

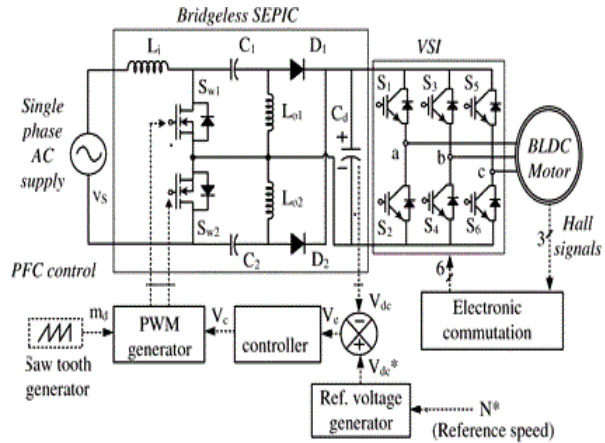
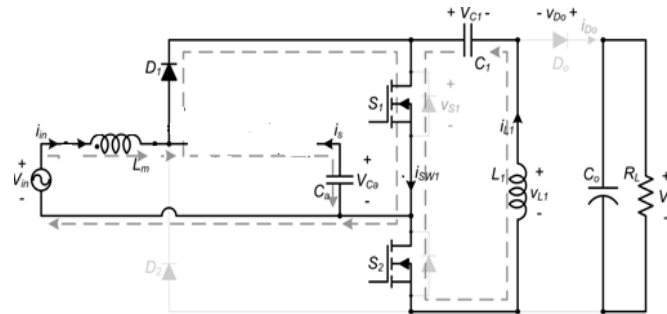


FIGURE 1(b)

Figure 1(a) Block diagram of the proposed model

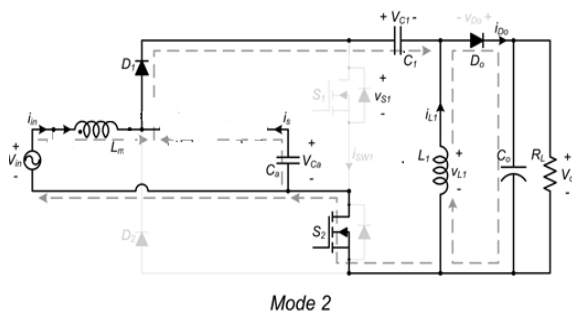
Figure 1(b) Circuit diagram of the proposed model

Figure 1.a. shows the block diagram of the efficient bridgeless SEPIC converter for BLDC motor with improve power factor by using ANFIS Controller. Figure 1.b. shows the circuit diagram for the efficient bridgeless SEPIC converter for BLDC motor with improve power factor.



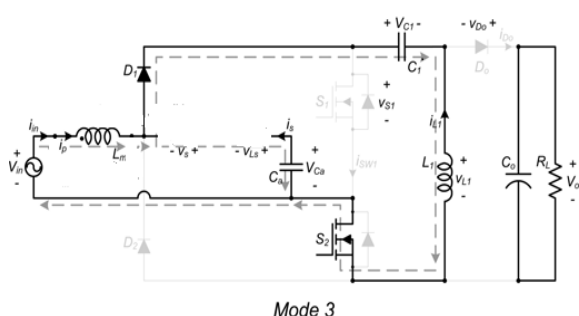
Mode 1

FIGURE. 2 (a)



Mode 2

FIGURE 2(c)



Mode 3

FIGURE 2(d)

FIGURE 2 MODES OF OPERATION



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Figure 2. shows the proposed BL SEPIC converter-based VSI –fed BLDC motor drive. The parameters obtained in the BL SEPIC converter are designed for the operation in discontinues inductor current mode (DICM) to obtained nearly unity power factor corrected phases at AC mains. Presence of variable DC link voltage control of VSI controls the speed is obtained using a BL-SEPIC converter.

MODES OF OPERATION

MODE 1: Switch S_2 is turned ON with switch S_2 is still conducting, so the voltage V_P across L_m as V_{in} .

MODE 2: Switch S_2 is turned OFF and the switch S_2 and diode D_0 is still conducting. So the voltage V_P across L_m is $-V_0$.

MODE 3: Switch S_1 and D_0 is turned OFF, Switch S_2 is switch conducting. Since the voltage across L_m is zero.

The output voltage is typically of the same polarity of the input, and can be lower or higher than the input. Such a non-inverting buck-boost converter may use a single inductor which is used for both the buck inductor and the boost inductor; it may use multiple inductors but only a single switch as in the SEPIC topologies. The two operating states of a SEPIC converter: When the switch is turned-on, the input voltage source supplies current to the inductor, and the capacitor supplies current to the resistor (output load). When the switch is opened, the inductor discharges current to the load via the diode D. The operation of SEPIC converter during discontinuous conduction mode is to provide current to reach zero for some time. But the power factor at source could not disturb due to the effective controller to control the switch and PFC stage presence. The voltage gain is given as the ratio of input voltage and product of inductor and current. During the discontinuous operation, the values of input voltage, output current and the duty cycle determine the output voltage.

a. Discontinuous Mode

The BL-SEPIC converter is designed to operate at discontinuous inductor current mode (DICM) such that the current flowing through inductors L_m and L_f are discontinuous but the voltage across the capacitor C_a and C_1 remains continuous in a switching period. The firing angle is calculated through the source voltage and diode to the output voltage. By varying the firing angle from zero to one, the output voltage is varied from source voltage to infinity. Thus the power is controlled and also the power factor is maintained at unity leading to improved power quality.

$$\delta = \frac{V_i D}{V_o}$$

Firing angle is given by the ratio of product of voltage gain and time. The load current I_0 equal to the average diode current (I_D). Therefore, the output current can be written as:

$$I_o = \bar{I}_D = \frac{I_{Lmax}}{2} \delta$$

Therefore, the output voltage gain can be written as:

$$\frac{V_o}{V_i} = - \frac{V_i D^2}{2LI_o}$$

a. ANFIS Controller

Fuzzy system theory can easily perform when the process is complicated compared with differential equation. It is obtained due to systematic procedure to transfer the desire human thought into a non-linear mapping. But the tuning of fuzzy system parameters (e.g., parameters of the membership function) is problem due to often it requires a relatively long time. ANFIS is a combination of fuzzy logic controller and neural network and hence named as a hybrid controller. It combines the advantages of both and hence used in complicated circuits.

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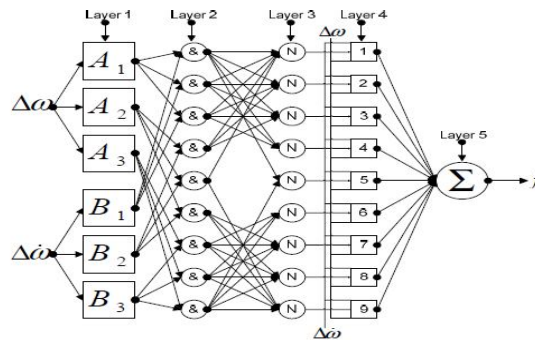


Figure 3 ANFIS structure with two-input sugeno fuzzy model

Table 1

Layer	Name of operation	Expression
1	Fuzzification	$o_{i,1} = \mu_{A_i}(\Delta\omega)$ $o_{i,1} = \mu_{B_i}(\Delta\omega)$
2	Ruled	$o_{i,2} = \omega_i$ $= \mu_{A_i}(\Delta\omega)\mu_{B_j}(\Delta\omega)$
3	Normalisation	$o_{i,3} = \bar{\omega}_i = \frac{\omega_i}{\sum \omega_j}$
4	Defuzzification	$o_{i,4} = \bar{\omega}_i f_i$
5	Summation	$o_{i,5} = \sum \bar{\omega}_i f_i$

Analysis of ANFIS controller layers & expressions

Figure 3 shows the five-layered structure of the ANFIS with first-order sugeno fuzzy model to obtain optimized efficiency and transparency. ANFIS constructs a fuzzy inference system whose parameters used training datas are tuned using combination of recursive least square algorithm and back propagation algorithm. Using this hybrid learning technique, the learning process speeds up compared to the gradient alone, which gives way to be trapped in local minima. Using of these membership function parameters and the controller controls the speed over the wide range without any ripples in the torque at load. Hence the power factor is improved at AC mains using the above technique and it is maintained nearer to unity. Table 1 shows the analysis of the ANFIS controller layers and expression for the operation of those layers.

IV. SIMULATION MODELS

Simulation model of bridgeless SEPIC converter is implemented in MATLAB/Simulink environment and simulation results are verified. The bridgeless configuration reduces the number of switches leading to better efficiency. Moreover, the conduction losses are reduced and better performance is achieved. The torque ripples are eliminated and the power quality is improved especially the power factor is maintained at unity.

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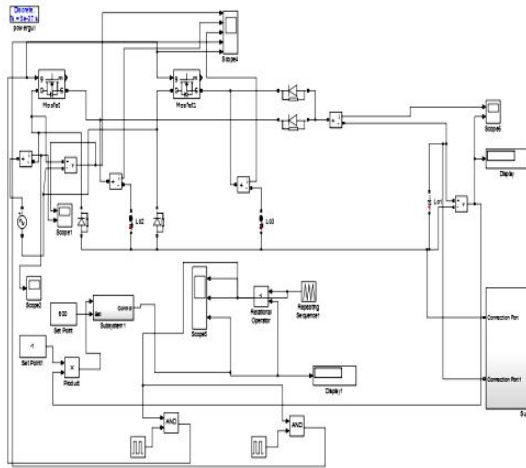


Figure 4(a)

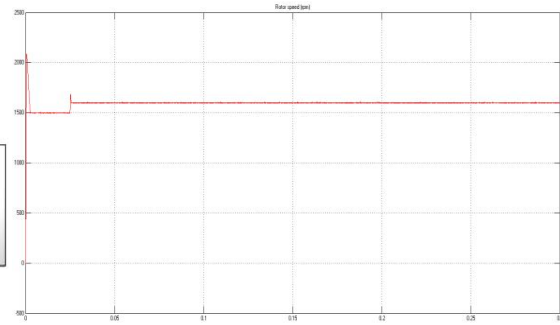


Figure 4(b)

Figure 4a. Simulation circuit for SEPIC converter

Figure 4b. Output waveform of speed performance in BLDC motor

Figure 4a. shows the bridgeless SEPIC rectifier with variable DC bus voltage consisting of IGBT Switch and some components like inductors, capacitors and diodes. The output from the DC bus voltage could be same polarity. Figure 4b. shows the simulation diagram for the BLDC motor along with the VSI and the ANFIS controller block to control the switch by firing gate pulse through the set speed and actual speed from the motor.

V.SIMULATION RESULTS

This chapter will investigate the results of the proposed model. Simulated results of the project are shown and discussed. It also ensures the proper working of the model. The output waveforms of various devices are shown.

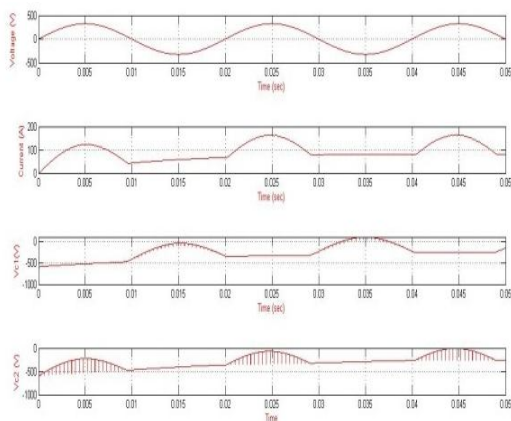


Figure 5(a)

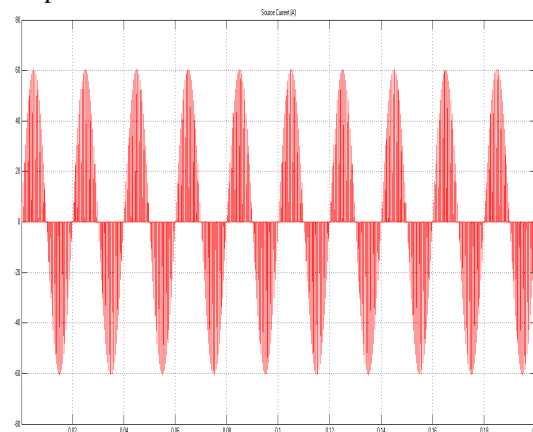


Figure 5(b)

Figure 5a. Waveforms for positive and negative half cycles of supply voltage, current through inductor and voltage through capacitors.

Figure 5b. Distortion less source current.

Figure 5a Shows the source voltages and currents taken from the positive and negative half cycles of the switches and Figure 5b shows the distortion less source current and THD of the source current is less than 2%.

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Here the simulation result for various modules are shown below which includes the simulation of interleaved Buck-Boost converters source voltage and current. Simulation of speed performance in BLDC motor under ANFIS controller technique. Simulation of ripple less torque waveform for PI and ANFIS controller in BLDC motor.

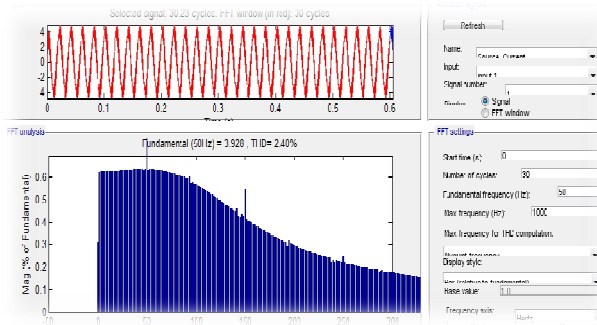


Figure 6(a)

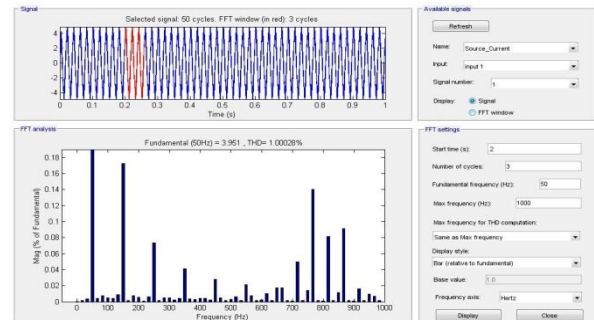


Figure 6(b)

Figure 6a. THD measurements in source current using PI

Figure 6b. THD measurements in source current using ANFIS

Figure 12 and 13 shows the THD in output voltage. THD of a signal is measurement of harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. The THD is usually expressed in percent as distortion factor or in dB relative to the fundamental as distortion attenuation. It should be within 3-5%. And in the output voltage the THD is about 2.40% which shows a very low distortion.

VII.CONCLUSION

Enhancing the performance of BLDC motor by improving the power quality in AC mains using Adaptive Fuzzy Logic Scheme has been studied. The system is attempted to design and develop an Advanced Driver system for a BLDC Motor fed by a “Power Factor Corrected” Bridgeless Rectifier Unit. The rectifier stage consists of SEPIC converter configuration. Reduction in the source current harmonics average current control technique is implemented by adopting fuzzy logic scheme. The proposed scheme of control is expected to offer reduced torque ripple and increased power quality on the source side. The proposed topology uses single stage PFC converter which reduces component count leading to a compact design with reduced cost.

REFERENCES

- [1]. Siriki.S.M.Ravi kumar, T. Srinivasa rao, K.durga rao “New efficient bridgeless cuk rectifiers for PFC application on D.C machine” IEEE transactions on power electronics, vol 9, Issue 1, pp. 15-21 Nov 2013
- [2]. K. Bett1, N. Nderu, K. Hinga “Adaptive neuro-fuzzy inference system based control of three-phase hybrid power filter for harmonic mitigation” IEEE transactions on industrial electronics volume 2, issue 8, Aug 2012
- [3]. A. Fardoun, H. Ismail, J. Sabzali and A. Al-saffar, “New efficient bridgeless cuk rectifiers for PFC applications”, IEEE trans. Power electron., vol. 27, no. 7, pp. 3292–3301, Jul. 2012.
- [4]. Sanjeev singh, “A voltage-controlled pfc cuk converter-based pmbldcm drive for air-conditioners” IEEE transactions on industry applications, vol. 48, no. 2, Mar/Apr. 2012
- [5]. B.Singh, Singh, Chandra, and Al-haddad, “Comprehensive study of single-phase ac-dc power factor corrected converters with high-frequency isolation,” IEEE Trans. Ind. Informat., vol. 7, no. 4, pp. 540–556, Nov. 2011.
- [6]. J. Sabzali, H. Ismail, A. Al-saffar, and A. Fardoun, “New bridgeless dem sepic and cuk PFC rectifiers with low conduction and switching losses,” IEEE trans. Ind. Appl., vol. 47, no. 2, pp. 873–881, Mar./Apr. 2011.
- [7]. Jang and M. Jovanovi c, Bridgeless high-power-factor buck converter,” IEEE trans. Power electron., vol. 26, no. 2, pp. 602–611, Feb. 2011.
- [8]. Singh, N. Singh, Chandra, Al-haddad, Pandey, and P. Kothari, “A review of single-phase improved power quality ac dc converters,” IEEE Trans. Ind. Electron., vol. 50, no. 5, pp. 962–981, Oct. 2003.